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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	25 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	8
Number of Gates	-
Number of I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	24-DIP (0.300", 7.62mm)
Supplier Device Package	24-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/gal20v8b-25lpi

GAL20V8

High Performance E²CMOS PLD Generic Array Logic™

Lead-Free Package Options Available!

ALL DEVICES DISCONTINUED

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 5 ns Maximum Propagation Delay
  - Fmax = 166 MHz
  - 4 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- 50% to 75% REDUCTION IN POWER FROM BIPOLAR
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- ACTIVE PULL-UPS ON ALL PINS
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 24-pin PAL® Devices with Full Function/ Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

Functional Block Diagram

Description

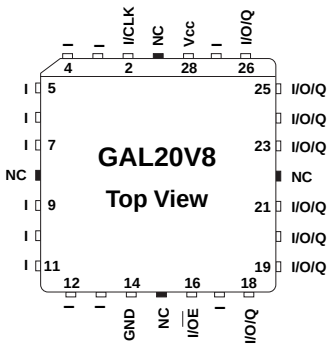
The GAL20V8C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8 are the PAL architectures listed in the table of the macrocell description section. GAL20V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

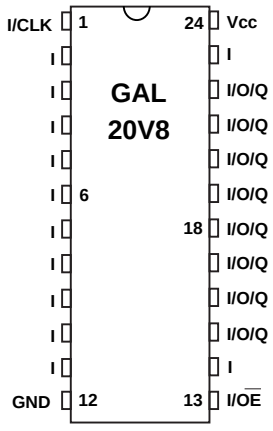
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



DIP



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August 2006

GAL20V8 Ordering Information

Conventional Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJ[1]	28-Lead PLCC
7.5	7	5	115	GAL20V8C-7LJ	28-Lead PLCC
			115	GAL20V8B-7LP[1]	24-Pin Plastic DIP
10	10	7	115	GAL20V8C-10LJ	28-Lead PLCC
			115	GAL20V8B-10LP	24-Pin Plastic DIP
15	12	10	55	GAL20V8B-15QP	24-Pin Plastic DIP
			55	GAL20V8B-15QJ	28-Lead PLCC
			90	GAL20V8B-15LP	24-Pin Plastic DIP
			90	GAL20V8B-15LJ	28-Lead PLCC
25	15	12	55	GAL20V8B-25QP	24-Pin Plastic DIP
			55	GAL20V8B-25QJ	28-Lead PLCC
			90	GAL20V8B-25LP	24-Pin Plastic DIP
			90	GAL20V8B-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8C-10LJI	28-Lead PLCC
			130	GAL20V8B-10LPI[1]	24-Pin Plastic DIP
			130	GAL20V8B-10LJI	28-Lead PLCC
15	12	10	130	GAL20V8B-15LPI	24-Pin Plastic DIP
			130	GAL20V8B-15LJI	28-Lead PLCC
20	13	11	65	GAL20V8B-20QPI	24-Pin Plastic DIP
			65	GAL20V8B-20QJI	28-Lead PLCC
25	15	12	65	GAL20V8B-25QPI	24-Pin Plastic DIP
			65	GAL20V8B-25QJI	28-Lead PLCC
			130	GAL20V8B-25LPI	24-Pin Plastic DIP
			130	GAL20V8B-25LJI	28-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

ALL DEVICES DISCONTINUED

Lead-Free Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJN[1]	Lead-Free 28-Lead PLCC
7.5	7	5	115	GAL20V8C-7LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-7LPN[1]	Lead-Free 24-Pin Plastic DIP
10	10	7	115	GAL20V8C-10LJN	Lead-Free 28-Lead PLCC
			115	GAL20V8B-10LPN	Lead-Free 24-Pin Plastic DIP
15	12	10	55	GAL20V8B-15QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-15QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-15LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-15LPN	Lead-Free 24-Pin Plastic DIP
25	15	12	55	GAL20V8B-25QJN	Lead-Free 28-Lead PLCC
			55	GAL20V8B-25QPN	Lead-Free 24-Pin Plastic DIP
			90	GAL20V8B-25LJN	Lead-Free 28-Lead PLCC
			90	GAL20V8B-25LPN	Lead-Free 24-Pin Plastic DIP

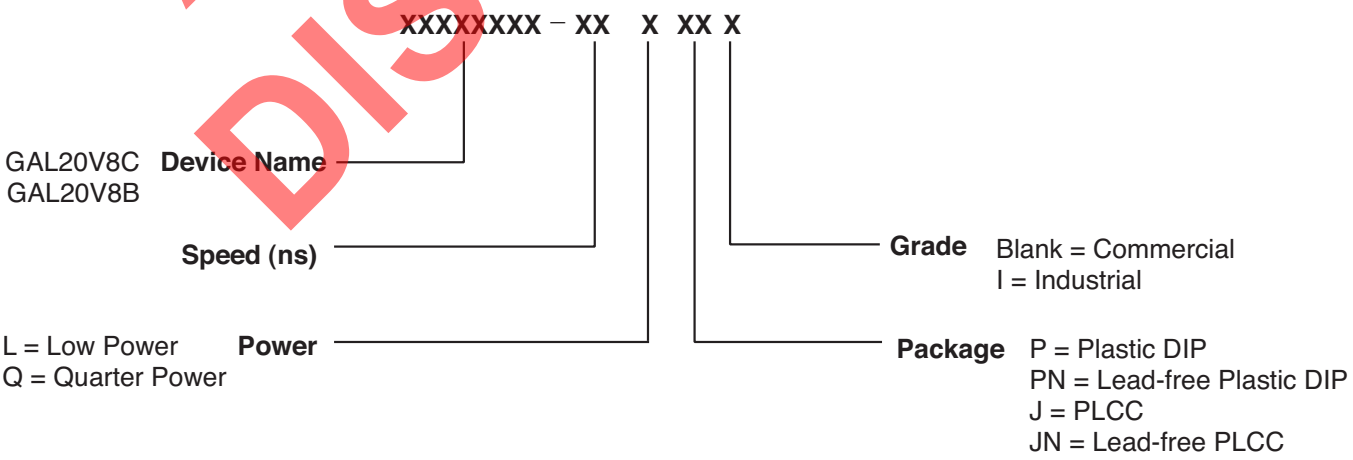
Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8C-10LJNI	Lead-Free 28-Pin Plastic DIP
			130	GAL20V8B-10LPNI[1]	Lead-Free 24-Pin Plastic DIP
15	12	10	130	GAL20V8B-15LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-15LPNI	Lead-Free 24-Pin Plastic DIP
20	13	11	65	GAL20V8B-20QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-20QPNI	Lead-Free 24-Pin Plastic DIP
25	15	12	65	GAL20V8B-25QJNI	Lead-Free 28-Lead PLCC
			65	GAL20V8B-25QPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL20V8B-25LJNI	Lead-Free 28-Lead PLCC
			130	GAL20V8B-25LPNI	Lead-Free 24-Pin Plastic DIP

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

ALL DEVICES DISCONTINUED

Part Number Description



Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8 . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20V8 can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20V8	GAL20V8 Global OLMC Mode
20R8	Registered
20R6	Registered
20R4	Registered
20RP8	Registered
20RP6	Registered
20RP4	Registered
20L8	Complex
20H8	Complex
20P8	Complex
14L8	Simple
16L6	Simple
18L4	Simple
20L2	Simple
14H8	Simple
16H6	Simple
18H4	Simple
20H2	Simple
14P8	Simple
16P6	Simple
18P4	Simple
20P2	Simple

ALL DEVICES DISCONTINUED

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 13 (DIP pinout) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 22 and pin 15 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18 and 19) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL20V8A
PLDesigner	P20V8R[2]	P20V8C[2]	P20V8C[2]	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS[3]	G20V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

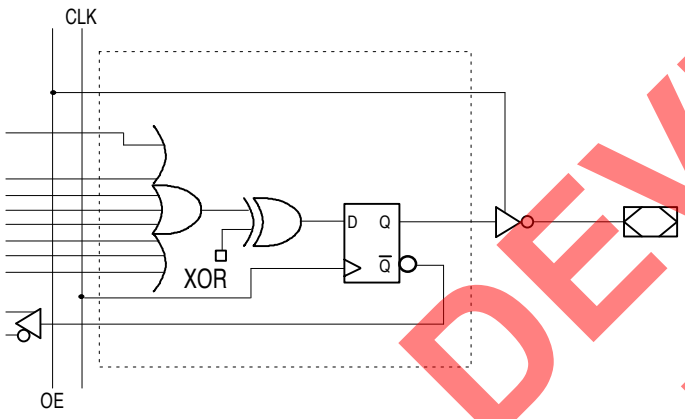
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode.

Dedicated input or output functions can be implemented as subsets of the I/O function.

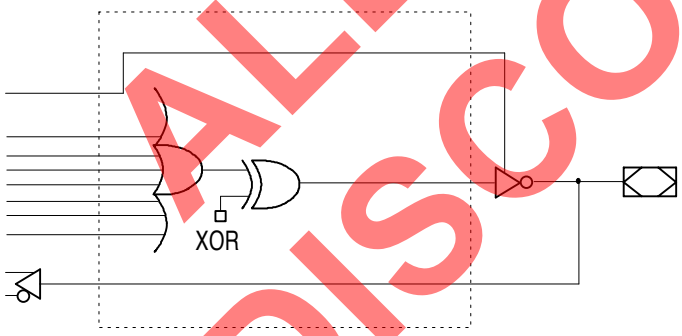
Registered outputs have eight product terms per output. I/Os have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 13 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



Combinatorial Configuration for Registered Mode

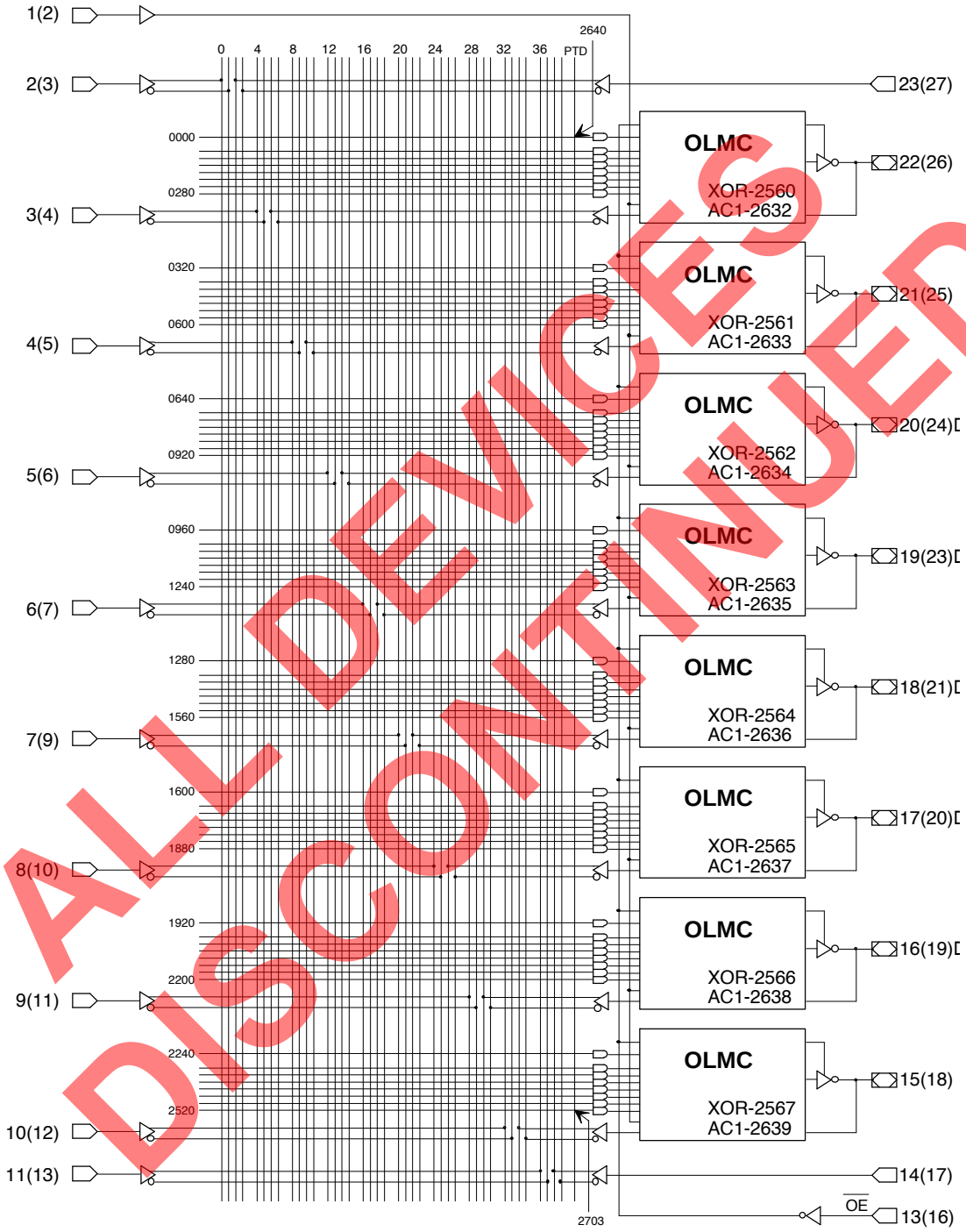
- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$ for registered output configuration..

ALL DEVICES DISCONTINUED

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2704
AC0-2705

ALL DEVICES DISCONTINUED

Complex Mode

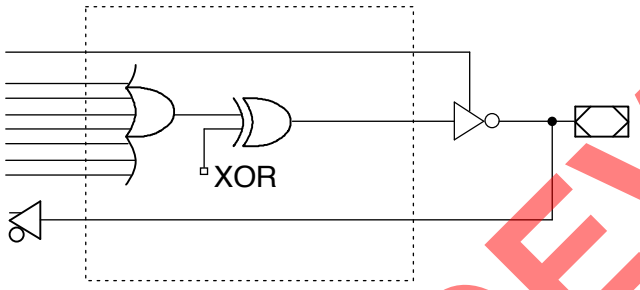
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

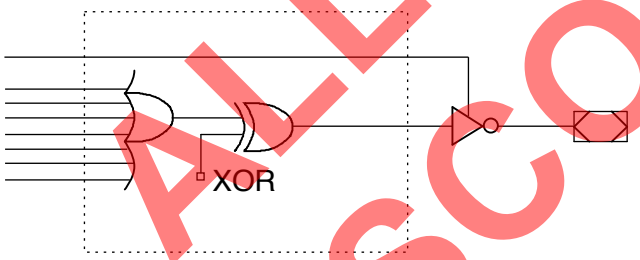
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 16 through Pin 21 are configured to this function.



Combinatorial Output Configuration for Complex Mode

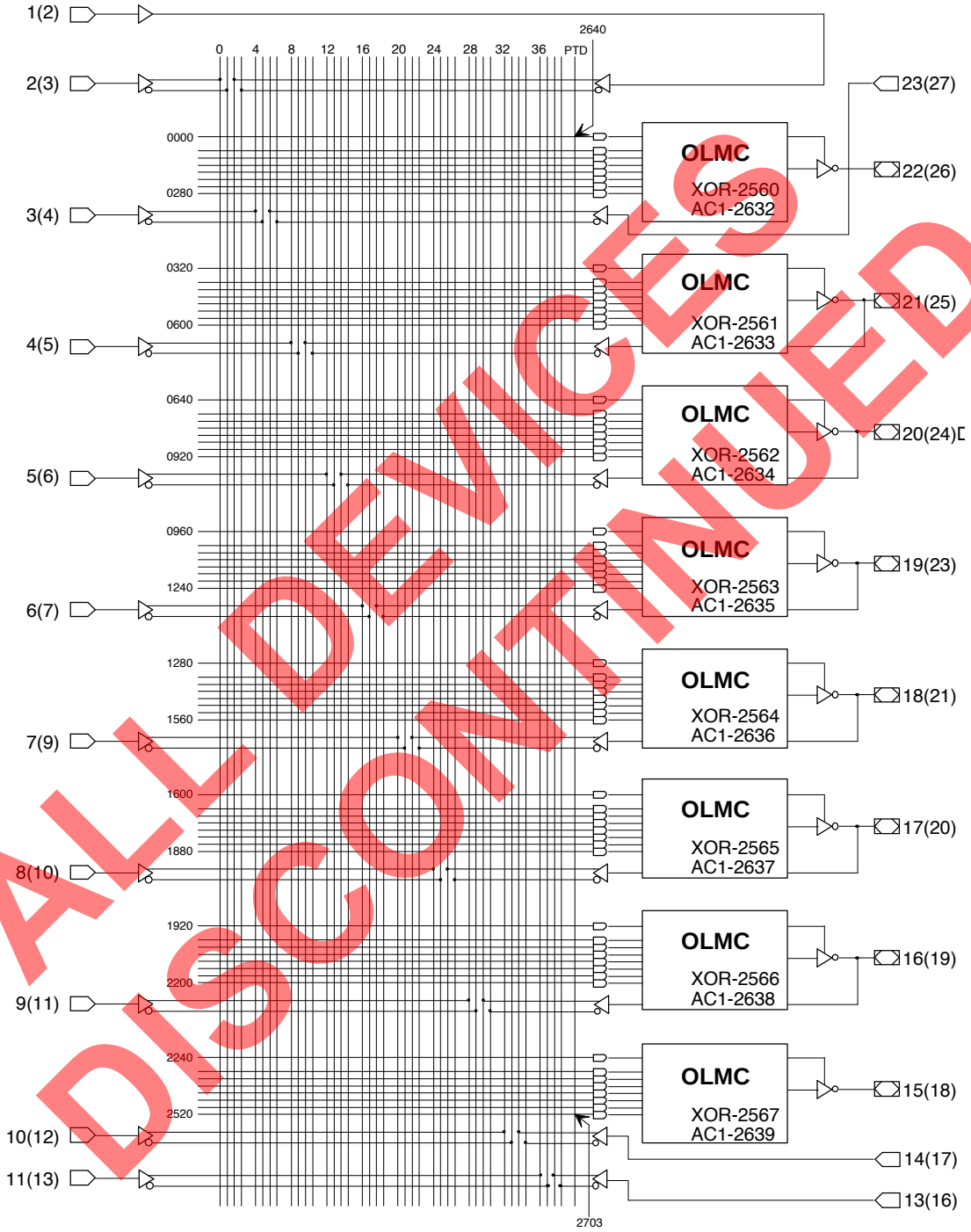
- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 15 and Pin 22 are configured to this function.

ALL DEVICES DISCONTINUED

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...			.... 2630, 2631
Byte 7	Byte 6	.... Byte 1	Byte 0

MSB LSB

SYN-2704
AC0-2705

ALL DEVICES DISCONTINUED

Simple Mode

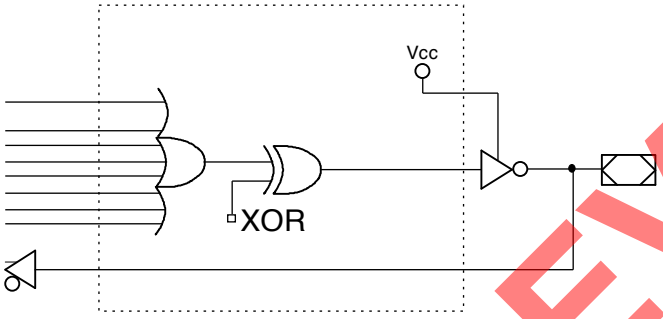
In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

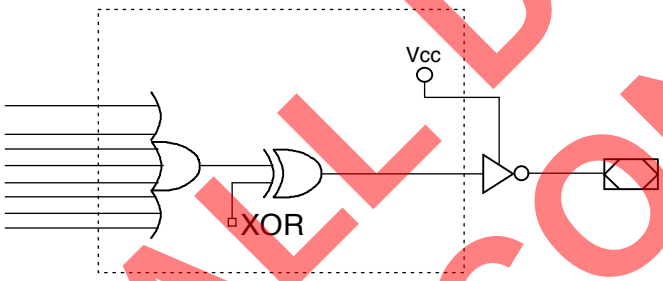
Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 18 and 19) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



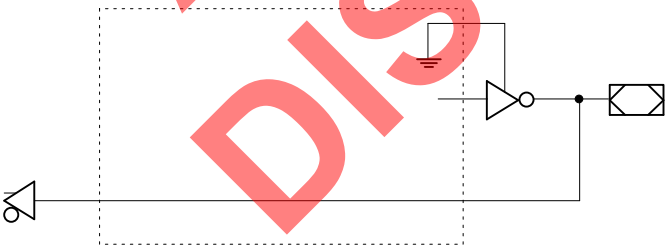
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 18 & 19 are permanently configured to this function.



Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.

ALL DEVICES DISCONTINUED

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.