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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc931a1fdh-512

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC9301FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC931A1FDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC9301FDH	4 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC931A1FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P2.2/MOSI	13	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	15	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	16	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6	27	I/O	**P2.6 —** Port 2 bit 6.
P2.7	28	I/O	**P2.7 —** Port 2 bit 7.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 10 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	9	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	8	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	7	I	**Ground:** 0 V reference.
V_{DD}	21	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[1]	x000 0000
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	PI2C	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[1]	
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD	TXD	[1]	
	Bit address		**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
P2*	Port 2	A0H	-	-	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	-	-	[1]	
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[1]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[1]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high-impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC9301/931A1 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

Table 5. Extended special function registers[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	-	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

7.2 Enhanced CPU

The P89LPC9301/931A1 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC9301/931A1 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 4) and can also be optionally divided to a slower frequency (see Section 7.11 “CCLK modification: DIVM register”).

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC9301/931A1 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

7.4 Crystal oscillator option

The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK and RTC. Low speed oscillator option can be the clock source of WDT.

7.4.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.4.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.4.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

7.16 I/O ports

The P89LPC9301/931A1 has four I/O ports: Port 0, Port 1, Port 2 and Port 3. Ports 0, 1, and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 7.

Table 7. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported	23

7.16.1 Port configurations

All but three I/O port pins on the P89LPC9301/931A1 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

7.16.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC9301/931A1 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit. The P89LPC9301/931A1 device has high current source on eight pins in push-pull mode. See Table 9 “Limiting values”.

7.16.2 Port 0 analog functions

The P89LPC9301/931A1 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

7.16.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC9301/931A1 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 10 “Static characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.17 Power monitoring functions

The P89LPC9301/931A1 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC9301/931A1 User manual*). Otherwise, instructions will be fetched from address 0000H.

7.20 Timers/counters 0 and 1

The P89LPC9301/931A1 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (Modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.20.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.20.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.20.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.20.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.20.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.20.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.24 SPI

The P89LPC9301/931A1 provides another high-speed serial communication interface: the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master mode or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

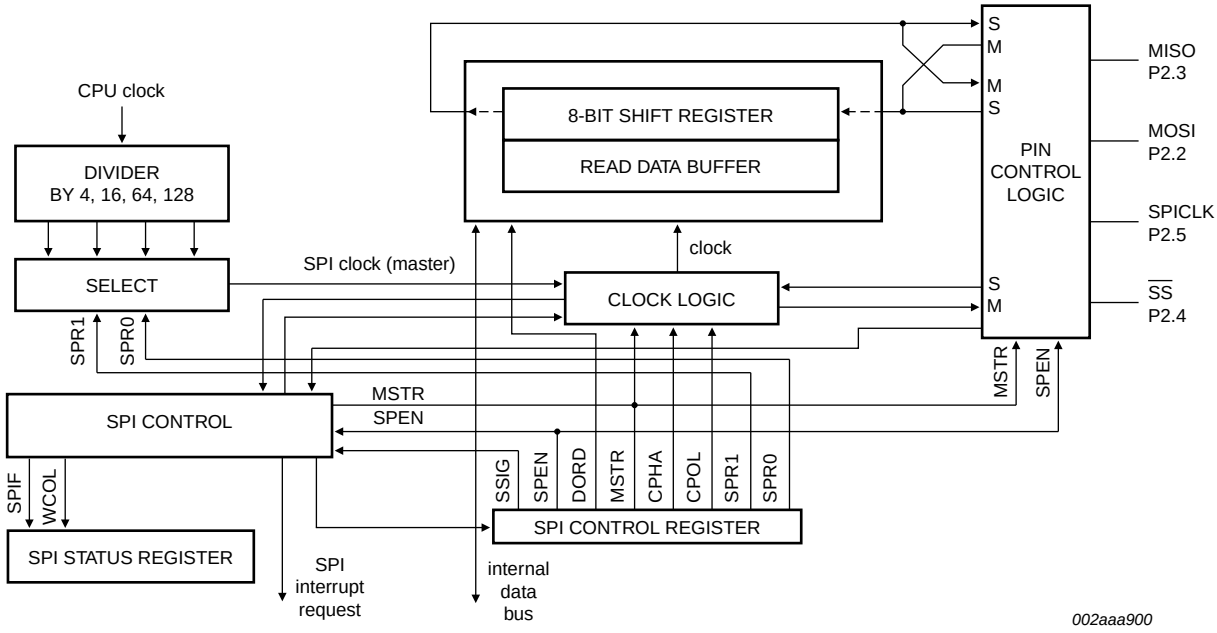


Fig 9. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the Master mode and is input in the Slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 10 through Figure 12.

7.24.1 Typical SPI configurations

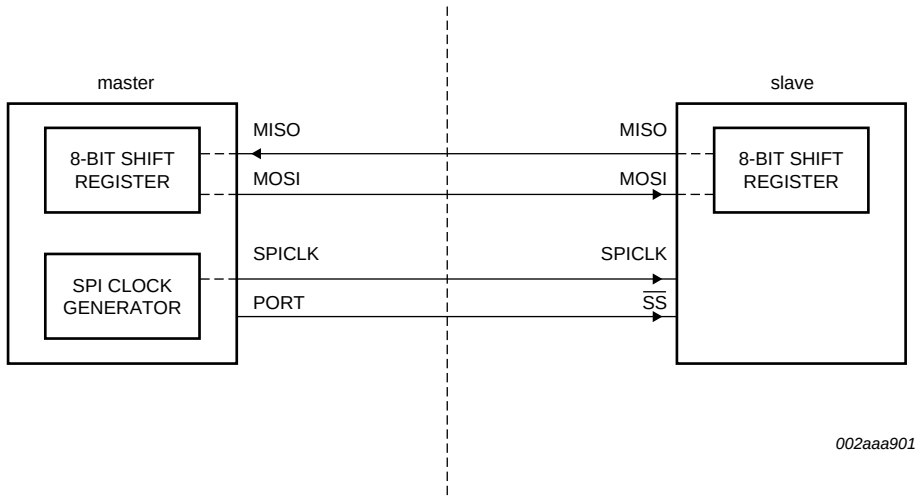


Fig 10. SPI single master single slave configuration

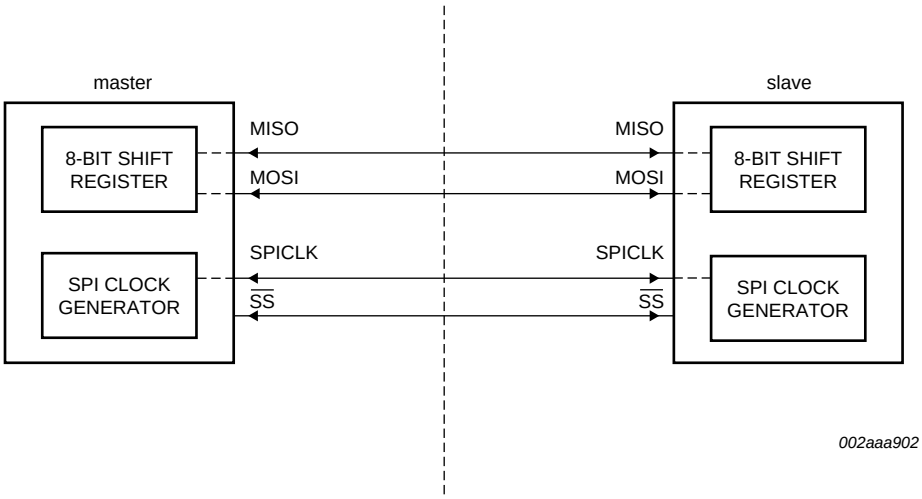
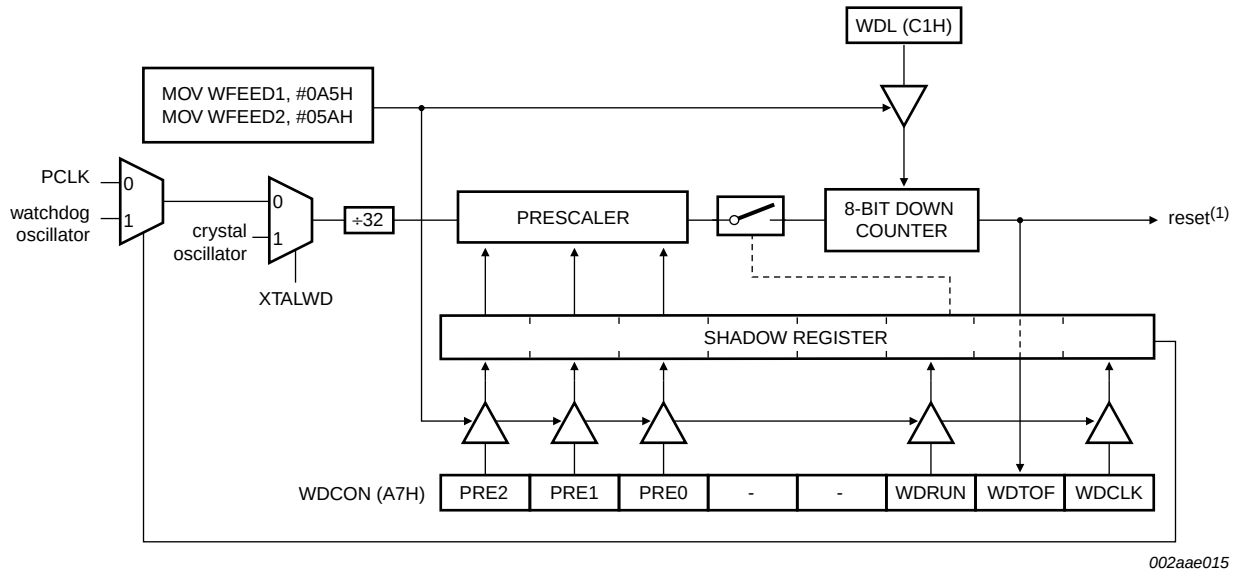


Fig 11. SPI dual device configuration, where either can be a master or a slave



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 14. Watchdog timer in Watchdog mode (WDTE = 1)

7.28 Additional features

7.28.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.28.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.29 Flash program memory

7.29.1 General description

The P89LPC9301/931A1 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9301/931A1 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to

Remark: Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this bootloader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom bootloader can be written with the Boot Vector set to the custom bootloader, if desired.

Table 8. Default boot vector values and ISP entry points

Device	Default boot vector	Default bootloader entry point	Default bootloader code range	1 kB sector range
P89LPC9301	0FH	0F00H	0E00H to 0FFFH	0C00H to 0FFFH
P89LPC931A1	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.29.10 Hardware activation of the bootloader

The bootloader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC9301/931A1 User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector is changed, it will no longer point to the factory pre-programmed ISP bootloader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.30 User configuration bytes

Some user-configurable features of the P89LPC9301/931A1 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the *P89LPC9301/931A1 User manual* for additional details.

7.31 User sector security bytes

There are four/eight User Sector Security Bytes on the P89LPC9301/931A1. Each byte corresponds to one sector. Please see the *P89LPC9301/931A1 User manual* for additional details.

8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature			−55	+125	°C
T_{stg}	storage temperature			−65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin			-	20	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin			-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current			-	100	mA
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pin to V_{SS}		-	V_{DD} + 0.5	V
V_n	voltage on any other pin	except XTAL1, XTAL2 to V_{SS}		−0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[2]	−3000	+3000	V
		charged device model; all pins		−700	+700	V

[1] The following applies to Table 9:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

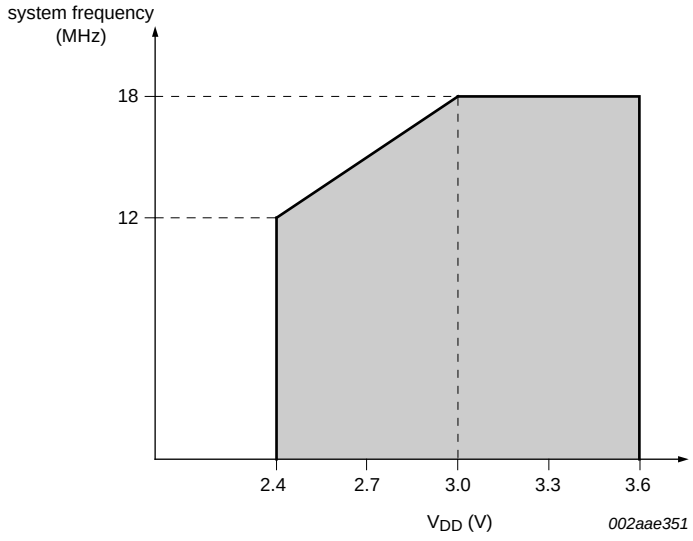
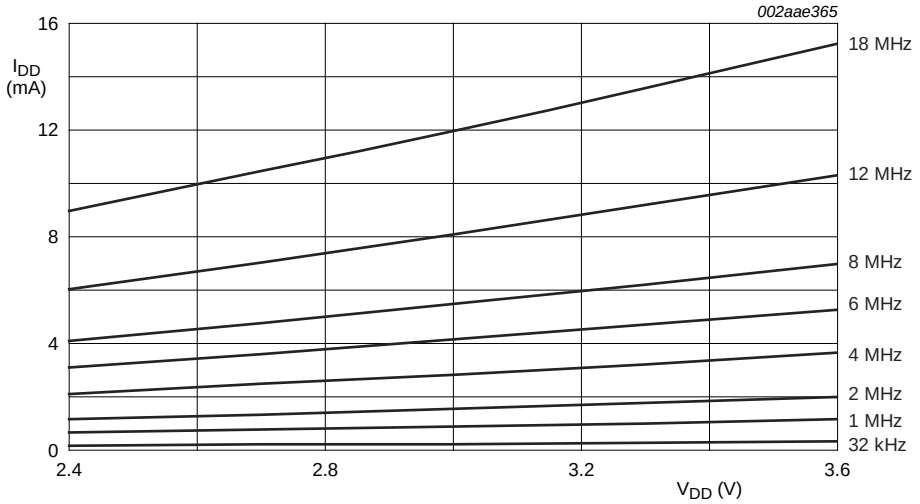
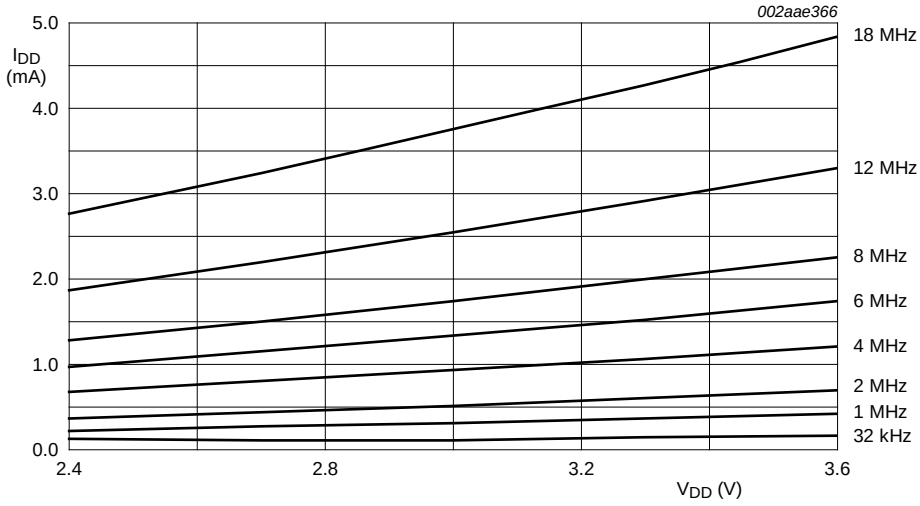


Fig 15. Frequency vs. supply voltage



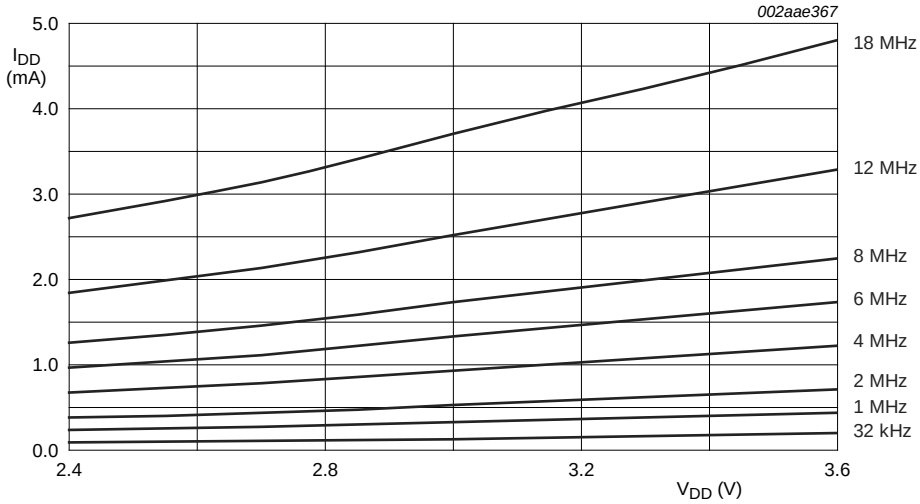
Test conditions: normal mode, code while(1) {} executed from on-chip flash; using an external clock.

Fig 18. $I_{DD(oper)}$ vs. frequency at +85 °C



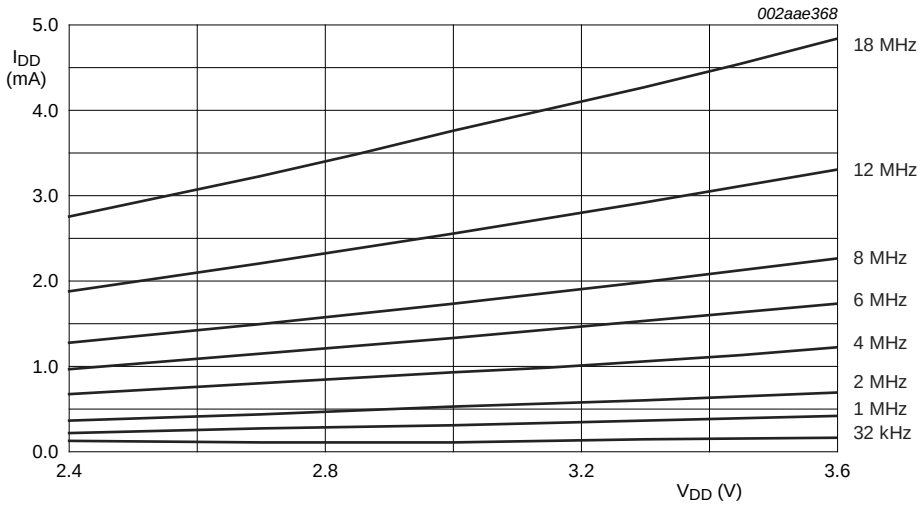
Test conditions: Idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

Fig 19. $I_{DD(idle)}$ vs. frequency at +25 °C



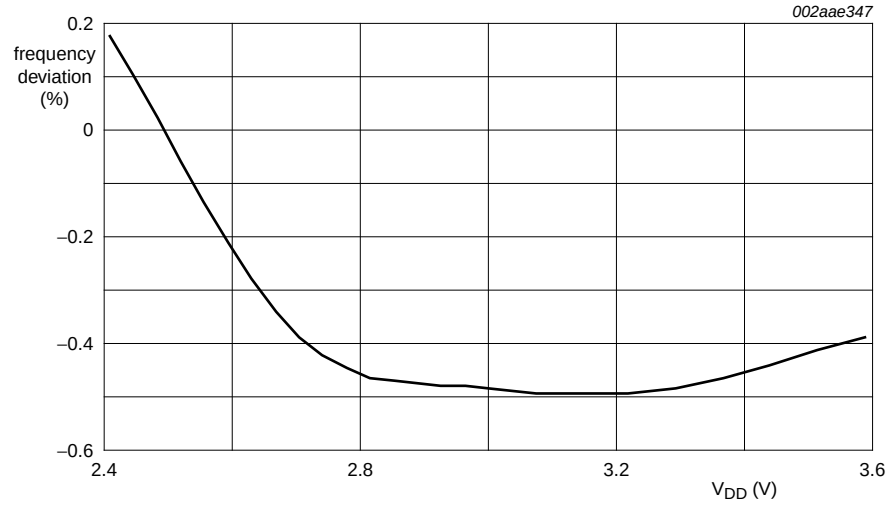
Test conditions: Idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

Fig 20. $I_{DD(idle)}$ vs. frequency at –40 °C



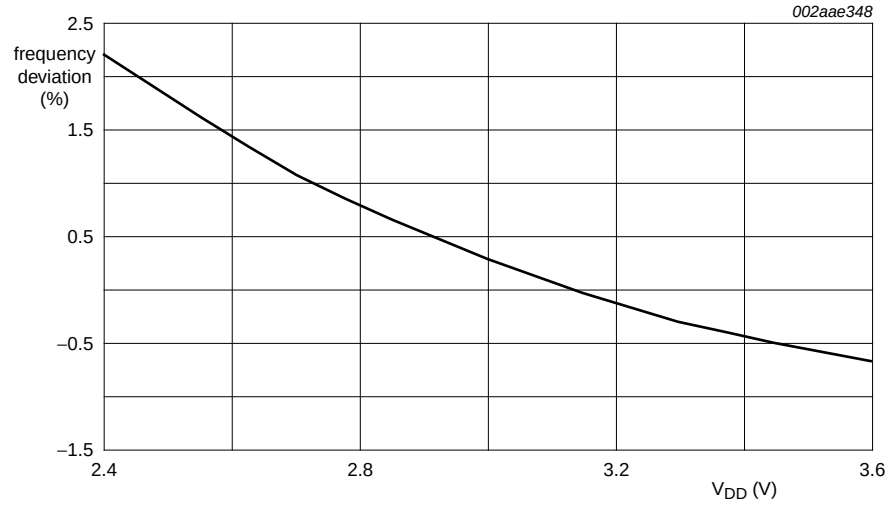
Test conditions: Idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

Fig 21. $I_{DD(idle)}$ vs. frequency at +85 °C



Central frequency of internal RC oscillator = 7.3728 MHz

Fig 26. Average internal RC oscillator frequency vs. V_{DD} at +85 °C



Central frequency of watchdog oscillator = 400 kHz

Fig 27. Average watchdog oscillator frequency vs. V_{DD} at +25 °C

10. Dynamic characteristics

Table 12. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON, V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	T_{amb} = 25 °C	380	420	380	420	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 32	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{\text{RST}}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 32	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 32	33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 32	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 32	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 31	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 31	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 31	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 31	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 31	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	2.0	MHz
	master		-	$^{CCLK}/_{4}$	-	3.0	MHz

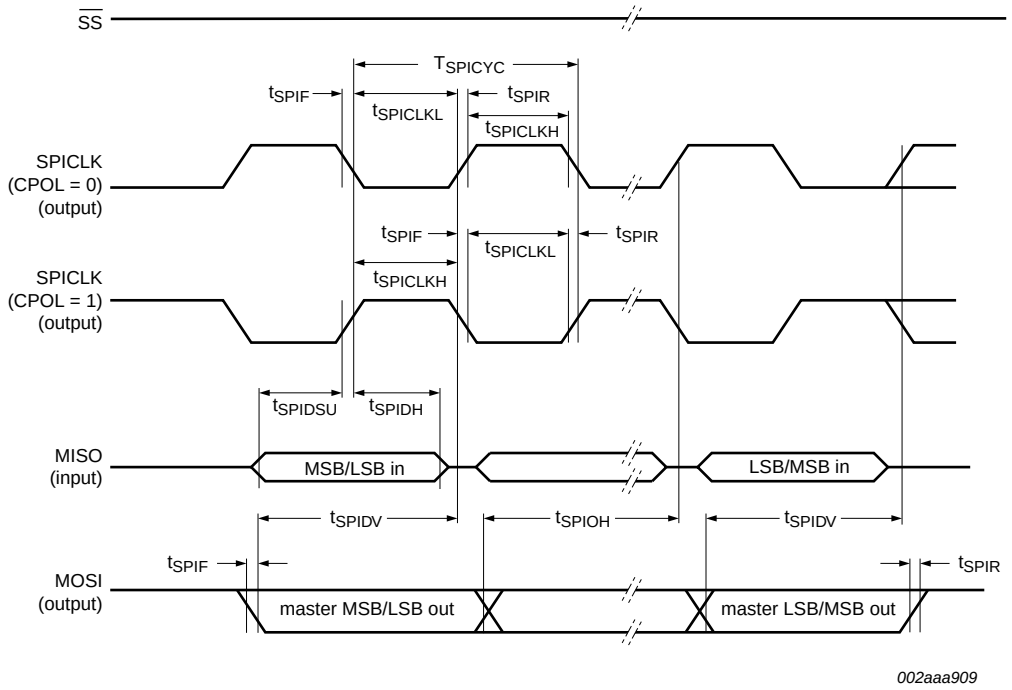


Fig 34. SPI master timing (CPHA = 1)

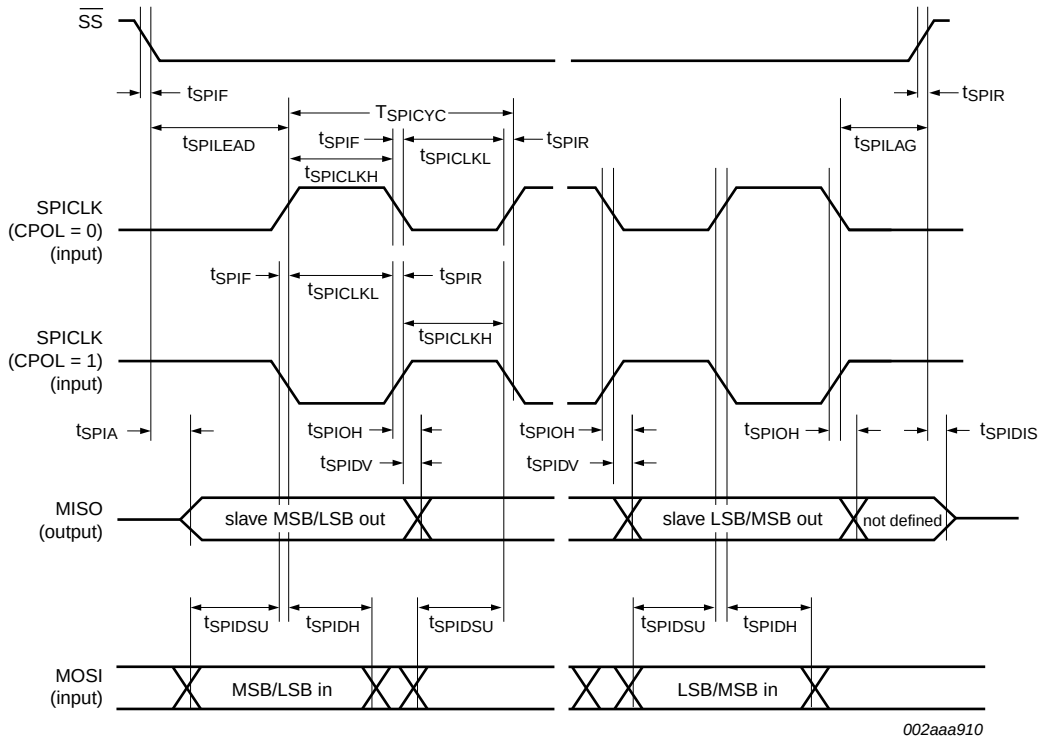


Fig 35. SPI slave timing (CPHA = 0)

17. Contents

continued >>