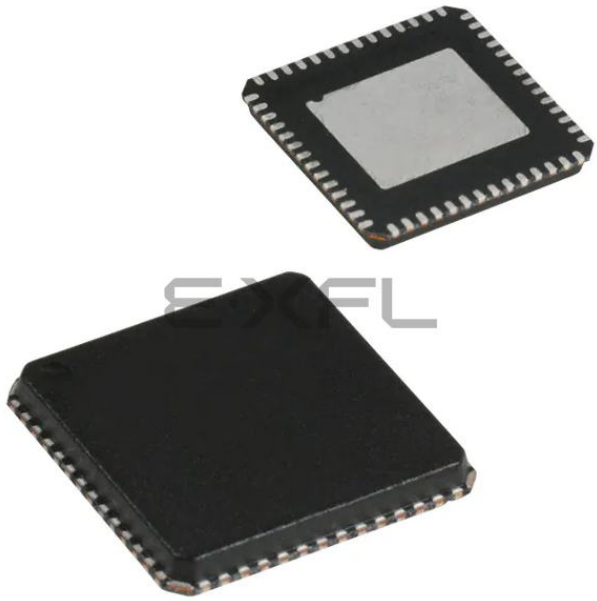

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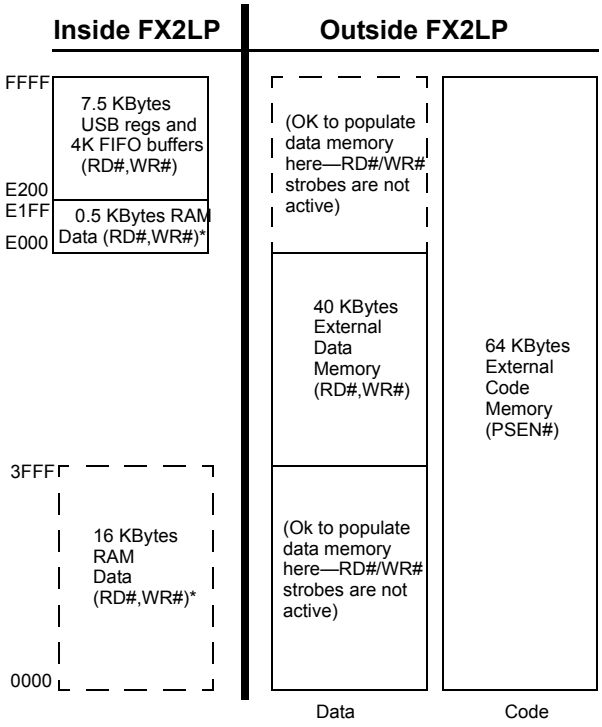
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	26
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68015a-56lfxc

Figure 4. External Code Memory, EA = 1



*SUDPTR, USB upload/download, I^2C interface boot access

3.11 Register Addresses

FFFF F000	4 KBytes EP2-EP8 buffers (8 x 512)
EFFF E800	2 KBytes RESERVED
E7FF E7C0	64 Bytes EP1IN
E7BF E780	64 Bytes EP1OUT
E77F E740	64 Bytes EP0 IN/OUT
E73F E700	64 Bytes RESERVED
E6FF E500	8051 Addressable Registers (512)
E4FF E480	Reserved (128)
E47F E400	128 bytes GPIF Waveforms
E3FF E200	Reserved (512)
E1FF E000	512 bytes 8051 xdata RAM

3.12 Endpoint RAM

3.12.1 Size

- 3× 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

3.12.2 Organization

- EP0
- Bidirectional endpoint zero, 64 byte buffer
- EP1IN, EP1OUT
- 64 byte buffers, bulk or interrupt
- EP2, 4, 6, 8
- Eight 512 byte buffers, bulk, interrupt, or isochronous. EP4 and EP8 can be double buffered; EP2 and 6 can be either double, triple, or quad buffered. For high speed endpoint configuration options, see Figure 5.

3.12.3 Setup Data Buffer

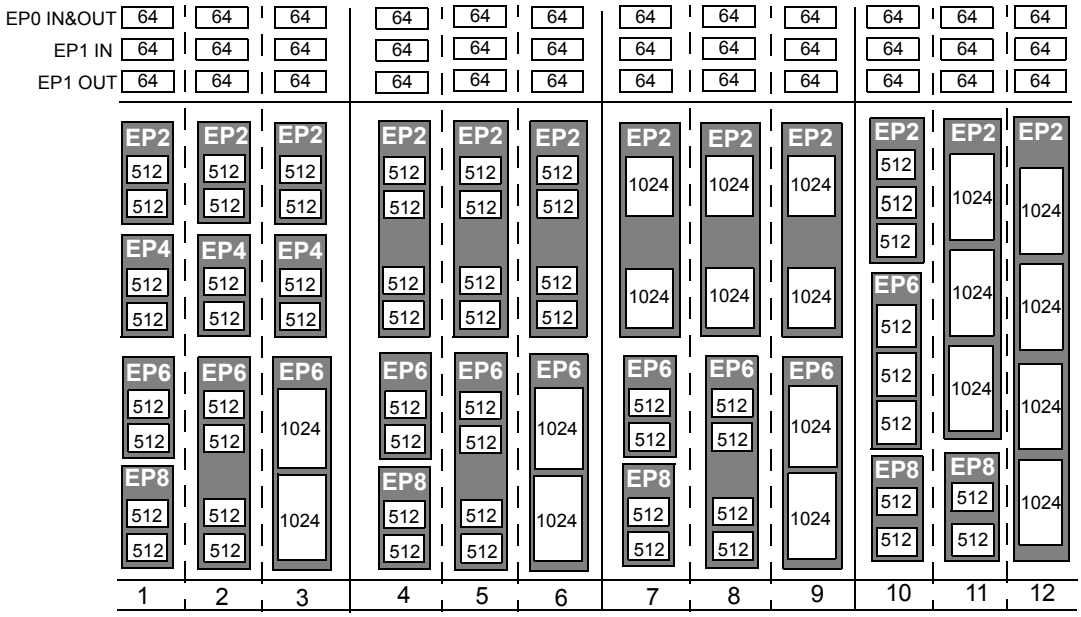
A separate 8 byte buffer at 0xE6B8-0xE6BF holds the setup data from a CONTROL transfer.

3.12.4 Endpoint Configurations (High Speed Mode)

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT.

The endpoint buffers can be configured in any 1 of the 12 configurations shown in the vertical columns. When operating in the full speed BULK mode only the first 64 bytes of each buffer are used. For example, in high speed, the max packet size is 512 bytes but in full speed it is 64 bytes. Even though a buffer is configured to a 512 byte buffer, in full speed only the first 64 bytes are used. The unused endpoint buffer space is not available for other operations. An example endpoint configuration is the EP2–1024 double buffered; EP6–512 quad buffered (column 8).

Figure 5. Endpoint Configuration



3.20 CY7C68013A/14A and CY7C68015A/16A Differences

CY7C68013A is identical to CY7C68014A in form, fit, and functionality. CY7C68015A is identical to CY7C68016A in form, fit, and functionality. CY7C68014A and CY7C68016A have a lower suspend current than CY7C68013A and CY7C68015A respectively and are ideal for power sensitive battery applications.

CY7C68015A and CY7C68016A are available in 56-pin QFN package only. Two additional GPIO signals are available on the CY7C68015A and CY7C68016A to provide more flexibility when neither IFCLK or CLKOUT are needed in the 56-pin package.

USB developers wanting to convert their FX2 56-pin application to a bus-powered system directly benefit from these additional signals. The two GPIOs give developers the signals they need for the power control circuitry of their bus-powered application without pushing them to a high pincount version of FX2LP.

The CY7C68015A is only available in the 56-pin QFN package

Table 10. CY7C68013A/14A and CY7C68015A/16A Pin Differences

CY7C68013A/CY7C68014A	CY7C68015A/CY7C68016A
IFCLK	PE0
CLKOUT	PE1

4. Pin Assignments

Figure 6 on page 15 identifies all signals for the five package types. The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 128-pin, 100-pin, and 56-pin packages.

The signals on the left edge of the 56-pin package in Figure 6 on page 15 are common to all versions in the FX2LP family with the noted differences between the CY7C68013A/14A and the CY7C68015A/16A.

Three modes are available in all package versions: Port, GPIF master, and Slave FIFO. These modes define the signals on the right edge of the diagram. The 8051 selects the interface mode using the IFCONFIG[1:0] register bits. Port mode is the power on default configuration.

The 100-pin package adds functionality to the 56-pin package by adding these pins:

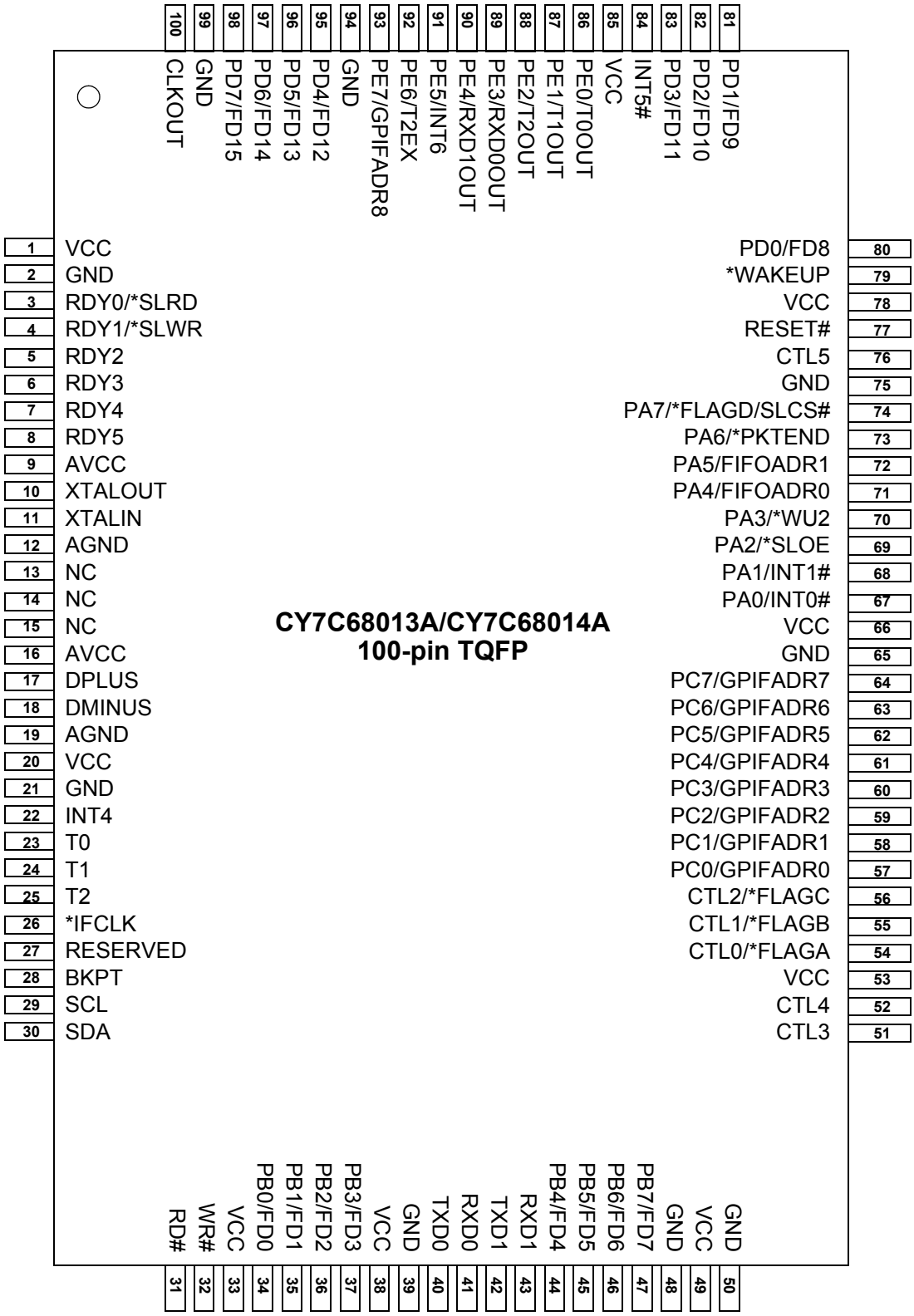
- PORTC or alternate GPIFADR[7:0] address signals
- PORTE or alternate GPIFADR[8] address signal and seven additional 8051 signals
- Three GPIF Control signals
- Four GPIF Ready signals
- Nine 8051 signals (two USARTs, three timer inputs, INT4,and INT5#)
- BKPT, RD#, WR#.

The 128-pin package adds the 8051 address and data buses plus control signals. Note that two of the required signals, RD# and WR#, are present in the 100-pin version.

In the 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from/writes to PORTC. This feature is enabled by setting PORTCSTB bit in CPUCS register.

Section 10.5 displays the timing diagram of the read and write strobing function on accessing PORTC.

Figure 8. CY7C68013A/CY7C68014A 100-pin TQFP Pin Assignment



* denotes programmable polarity

Table 11. FX2LP Pin Descriptions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VF-BGA	Name	Type	Default	Description
70	55	37	30	7G	CTL1 or FLAGB	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL1** is a GPIF control output. **FLAGB** is a programmable slave-FIFO output status flag signal. Defaults to FULL for the FIFO selected by the FIFOADR[1:0] pins.
71	56	38	31	8H	CTL2 or FLAGC	O/Z	H	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **CTL2** is a GPIF control output. **FLAGC** is a programmable slave-FIFO output status flag signal. Defaults to EMPTY for the FIFO selected by the FIFOADR[1:0] pins.
66	51				CTL3	O/Z	H	**CTL3** is a GPIF control output.
67	52				CTL4	Output	H	**CTL4** is a GPIF control output.
98	76				CTL5	Output	H	**CTL5** is a GPIF control output.
32	26	20	13	2G	IFCLK on CY7C68013A and CY7C68014A --- PE0 on CY7C68015A and CY7C68016A	I/O/Z --- I/O/Z	Z --- I	Interface Clock, used for synchronously clocking data into or out of the slave FIFOs. IFCLK also serves as a timing reference for all slave FIFO control signals and GPIF. When internal clocking is used (IFCONFIG.7 = 1) the IFCLK pin can be configured to output 30/48 MHz by bits IFCONFIG.5 and IFCONFIG.6. IFCLK may be inverted, whether internally or externally sourced, by setting the bit IFCONFIG.4 =1. --- **PE0** is a bidirectional I/O port pin.
28	22				INT4	Input	N/A	**INT4** is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH.
106	84				INT5#	Input	N/A	**INT5#** is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW.
31	25				T2	Input	N/A	**T2** is the active-HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2 = 1. When C/T2 = 0, Timer2 does not use this pin.
30	24				T1	Input	N/A	**T1** is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit.
29	23				T0	Input	N/A	**T0** is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit.
53	43				RXD1	Input	N/A	**RXD1**is an active-HIGH input signal for 8051 UART1, which provides data to the UART in all modes.
52	42				TXD1	Output	H	**TXD1**is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode.
51	41				RXD0	Input	N/A	**RXD0** is the active-HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes.

Table 11. FX2LP Pin Descriptions (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VF-BGA	Name	Type	Default	Description
50	40				TXD0	Output	H	**TXD0** is the active-HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode.
42					CS#	Output	H	**CS#** is the active-LOW chip select for external memory.
41	32				WR#	Output	H	**WR#** is the active-LOW write strobe output for external memory.
40	31				RD#	Output	H	**RD#** is the active-LOW read strobe output for external memory.
38					OE#	Output	H	**OE#** is the active-LOW output enable for external memory.
33	27	21	14	2H	Reserved	Input	N/A	**Reserved**. Connect to ground.
101	79	51	44	7B	WAKEUP	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB® chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	15	3F	SCL	OD	Z	**Clock** for the I^2C interface. Connect to VCC with a 2.2K resistor, even if no I^2C peripheral is attached.
37	30	23	16	3G	SDA	OD	Z	**Data** for **I^2C-compatible interface**. Connect to VCC with a 2.2K resistor, **even if no I^2C-compatible peripheral is attached**.
2	1	6	55	5A	VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
26	20	18	11	1G	VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
43	33	24	17	7E	VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
48	38				VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
64	49	34	27	8E	VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
68	53				VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
81	66	39	32	5C	VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
100	78	50	43	5B	VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
107	85				VCC	Power	N/A	**VCC**. Connect to 3.3V power source.
3	2	7	56	4B	GND	Ground	N/A	**Ground**.
27	21	19	12	1H	GND	Ground	N/A	**Ground**.
49	39				GND	Ground	N/A	**Ground**.
58	48	33	26	7D	GND	Ground	N/A	**Ground**.
65	50	35	28	8D	GND	Ground	N/A	**Ground**.
80	65				GND	Ground	N/A	**Ground**.
93	75	48	41	4C	GND	Ground	N/A	**Ground**.
116	94				GND	Ground	N/A	**Ground**.
125	99	4	53	4A	GND	Ground	N/A	**Ground**.
14	13				NC	N/A	N/A	**No Connect**. This pin must be left open.
15	14				NC	N/A	N/A	**No Connect**. This pin must be left open.
16	15				NC	N/A	N/A	**No Connect**. This pin must be left open.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E65D	1	USBIRQ[12]	USB Interrupt Requests	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	0xxxxxxx	rbbbbbbb
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E65F	1	EPIRQ[12]	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	0	RW
E660	1	GPIFIE[11]	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW
E661	1	GPIFIRQ[11]	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	000000xx	RW
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E663	1	USBERRIRQ[12]	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	0000000x	bbbbrrrb
E664	1	ERRCNTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	xxxx0100	rrrrbbbb
E665	1	CLRERRCNT	Clear Error Counter EC3:0	x	x	x	x	x	x	x	x	xxxxxxxx	W
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	I2V4	I2V3	I2V2	I2V1	I2V0	0	0	00000000	R
E667	1	INT4IVEC	Interrupt 4 (slave FIFO & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	10000000	R
E668	1	INTSET-UP	Interrupt 2&4 setup	0	0	0	0	AV2EN	0	INT4SRC	AV4EN	00000000	RW
E669	7	reserved											
		INPUT / OUTPUT											
E670	1	PORTACFG	I/O PORTA Alternate Configuration	FLAGD	SLCS	0	0	0	0	INT1	INT0	00000000	RW
E671	1	PORTCCFG	I/O PORTC Alternate Configuration	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
E672	1	PORTECFG	I/O PORTE Alternate Configuration	GPIFA8	T2EX	INT6	RXD1OUT	RXD0OUT	T2OUT	T1OUT	T0OUT	00000000	RW
E673	4	reserved											
E677	1	reserved											
E678	1	I^2CS	I²C Bus Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbrrrrr
E679	1	I2DAT	I²C Bus Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW
E67A	1	I^2CTL	I²C Bus Control	0	0	0	0	0	0	STOPIE	400KHZ	00000000	RW
E67B	1	XAUTODAT1	Autoptr1 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E67C	1	XAUTODAT2	Autoptr2 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
		UDMA CRC											
E67D	1	UDMACRCH[11]	UDMA CRC MSB	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	01001010	RW
E67E	1	UDMACRCL[11]	UDMA CRC LSB	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	10111010	RW
E67F	1	UDMACRC-QUALIFIER	UDMA CRC Qualifier	QENABLE	0	0	0	QSTATE	QSIGNAL2	QSIGNAL1	QSIGNAL0	00000000	brrrbbbb
		USB CONTROL											
E680	1	USBCS	USB Control & Status	HSM	0	0	0	DISCON	NOSYNSOF	RENUM	SIGRSUME	x0000000	rrrrbbbb
E681	1	SUSPEND	Put chip into suspend	x	x	x	x	x	x	x	x	xxxxxxxx	W
E682	1	WAKEUPCS	Wakeup Control & Status	WU2	WU	WU2POL	WUPOL	0	DPEN	WU2EN	WUEN	xx000101	bbbbrbbb
E683	1	TOGCTL	Toggle Control	Q	S	R	I/O	EP3	EP2	EP1	EP0	x0000000	rrrbbbbb
E684	1	USBFRAMEH	USB Frame count H	0	0	0	0	0	FC10	FC9	FC8	00000xxx	R
E685	1	USBFRAMEL	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxxx	R
E686	1	MICROFRAME	Microframe count, 0-7	0	0	0	0	0	MF2	MF1	MF0	00000xxx	R
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	0xxxxxxx	R
E688	2	reserved											
		ENDPOINTS											
E68A	1	EP0BCH[11]	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxxx	RW
E68B	1	EP0BCL[11]	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E68C	1	reserved											
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E68E	1	reserved											
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E690	1	EP2BCH[11]	Endpoint 2 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E691	1	EP2BCL[11]	Endpoint 2 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E692	2	reserved											
E694	1	EP4BCH[11]	Endpoint 4 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW
E695	1	EP4BCL[11]	Endpoint 4 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E696	2	reserved											
E698	1	EP6BCH[11]	Endpoint 6 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E699	1	EP6BCL[11]	Endpoint 6 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69A	2	reserved											
E69C	1	EP8BCH[11]	Endpoint 8 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E6CB	1	FLOWSTB	Flowstate Strobe Configuration	SLAVE	RDYASYNC	CTLTOGL	SUSTAIN	0	MSTB2	MSTB1	MSTB0	00100000	RW
E6CC	1	FLOWSTBEDGE	Flowstate Rising/Falling Edge Configuration	0	0	0	0	0	0	FALLING	RISING	00000001	rrrrrrbb
E6CD	1	FLOWSTBPERIOD	Master-Strobe Half-Period	D7	D6	D5	D4	D3	D2	D1	D0	00000010	RW
E6CE	1	GPIFTCB3[11]	GPIF Transaction Count Byte 3	TC31	TC30	TC29	TC28	TC27	TC26	TC25	TC24	00000000	RW
E6CF	1	GPIFTCB2[11]	GPIF Transaction Count Byte 2	TC23	TC22	TC21	TC20	TC19	TC18	TC17	TC16	00000000	RW
E6D0	1	GPIFTCB1[11]	GPIF Transaction Count Byte 1	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW
E6D1	1	GPIFTCB0[11]	GPIF Transaction Count Byte 0	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000001	RW
	2	reserved										00000000	RW
		reserved											
		reserved											
E6D2	1	EP2GPIFFLGSEL[11]	Endpoint 2 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6D3	1	EP2GPIFPFSTOP	Endpoint 2 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO2FLAG	00000000	RW
E6D4	1	EP2GPIFTRIG[11]	Endpoint 2 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6DA	1	EP4GPIFFLGSEL[11]	Endpoint 4 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6DB	1	EP4GPIFPFSTOP	Endpoint 4 GPIF stop transaction on GPIF Flag	0	0	0	0	0	0	0	FIFO4FLAG	00000000	RW
E6DC	1	EP4GPIFTRIG[11]	Endpoint 4 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6E2	1	EP6GPIFFLGSEL[11]	Endpoint 6 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6E3	1	EP6GPIFPFSTOP	Endpoint 6 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO6FLAG	00000000	RW
E6E4	1	EP6GPIFTRIG[11]	Endpoint 6 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6EA	1	EP8GPIFFLGSEL[11]	Endpoint 8 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6EB	1	EP8GPIFPFSTOP	Endpoint 8 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO8FLAG	00000000	RW
E6EC	1	EP8GPIFTRIG[11]	Endpoint 8 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
E6F0	1	XGPIFSGLDATH	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW
E6F1	1	XGPIFSGLDATLX	Read/Write GPIF Data L & trigger transaction	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E6F2	1	XGPIFSGLDATL-NOX	Read GPIF Data L, no transaction trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
E6F3	1	GPIFREADYCFG	Internal RDY, Sync/Async, RDY pin states	INTRDY	SAS	TCXRDY5	0	0	0	0	0	00000000	bbbrrrrr
E6F4	1	GPIFREADYSTAT	GPIF Ready Status	0	0	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	00xxxxxx	R
E6F5	1	GPIFABORT	Abort GPIF Waveforms	x	x	x	x	x	x	x	x	xxxxxxxx	W
E6F6	2	reserved											
		ENDPOINT BUFFERS											
E740	64	EP0BUF	EP0-IN/-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E780	64	EP10UTBUF	EP1-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E7C0	64	EP1INBUF	EP1-IN buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E800	2048	reserved											RW
F000	1024	EP2FIFOBUF	512/1024 byte EP 2 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F400	512	EP4FIFOBUF	512 byte EP 4 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F600	512	reserved											
F800	1024	EP6FIFOBUF	512/1024 byte EP 6 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
FC00	512	EP8FIFOBUF	512 byte EP 8 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
FE00	512	reserved											

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
xxxx		I²C Configuration Byte		0	DISCON	0	0	0	0	0	400KHZ	xxxxxxxx [14]	n/a
		Special Function Registers (SFRs)											
80	1	IOA[13]	Port A (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
81	1	SP	Stack Pointer	D7	D6	D5	D4	D3	D2	D1	D0	00000111	RW
82	1	DPL0	Data Pointer 0 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
83	1	DPH0	Data Pointer 0 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
84	1	DPL1[13]	Data Pointer 1 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
85	1	DPH1[13]	Data Pointer 1 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
86	1	DPS[13]	Data Pointer 0/1 select	0	0	0	0	0	0	0	SEL	00000000	RW
87	1	PCON	Power Control	SMOD0	x	1	1	x	x	x	IDLE	00110000	RW
88	1	TCON	Timer/Counter Control (bit addressable)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000	RW
89	1	TMOD	Timer/Counter Mode Control	GATE	CT	M1	M0	GATE	CT	M1	M0	00000000	RW
8A	1	TL0	Timer 0 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
8B	1	TL1	Timer 1 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
8C	1	TH0	Timer 0 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
8D	1	TH1	Timer 1 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
8E	1	CKCON[13]	Clock Control	x	x	T2M	T1M	T0M	MD2	MD1	MD0	00000001	RW
8F	1	reserved											
90	1	IOB[13]	Port B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
91	1	EXIF[13]	External Interrupt Flag(s)	IE5	IE4	I²CINT	USBNT	1	0	0	0	00001000	RW
92	1	MPAGE[13]	Upper Addr Byte of MOVX using @R0 / @R1	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
93	5	reserved											
98	1	SCON0	Serial Port 0 Control (bit addressable)	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00000000	RW
99	1	SBUF0	Serial Port 0 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
9A	1	AUTOPTRH1[13]	Autopointer 1 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
9B	1	AUTOPTRL1[13]	Autopointer 1 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
9C	1	reserved											
9D	1	AUTOPTRH2[13]	Autopointer 2 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
9E	1	AUTOPTRL2[13]	Autopointer 2 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
9F	1	reserved											
A0	1	IOC[13]	Port C (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
A1	1	INT2CLR[13]	Interrupt 2 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W
A2	1	INT4CLR[13]	Interrupt 4 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W
A3	5	reserved											
A8	1	IE	Interrupt Enable (bit addressable)	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00000000	RW
A9	1	reserved											
AA	1	EP2468STAT[13]	Endpoint 2,4,6,8 status flags	EP8F	EP8E	EP6F	EP6E	EP4F	EP4E	EP2F	EP2E	01011010	R
AB	1	EP24FIFOFLGS [13]	Endpoint 2,4 slave FIFO status flags	0	EP4PF	EP4EF	EP4FF	0	EP2PF	EP2EF	EP2FF	00100010	R
AC	1	EP68FIFOFLGS [13]	Endpoint 6,8 slave FIFO status flags	0	EP8PF	EP8EF	EP8FF	0	EP6PF	EP6EF	EP6FF	01100110	R
AD	2	reserved											
AF	1	AUTOPTRSETUP[13]	Autopointer 1&2 setup	0	0	0	0	0	APTR2INC	APTR1INC	APTREN	00000110	RW
B0	1	IOD[13]	Port D (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B1	1	IOE[13]	Port E (NOT bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B2	1	OEA[13]	Port A Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B3	1	OEB[13]	Port B Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B4	1	OEC[13]	Port C Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B5	1	OED[13]	Port D Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B6	1	OEE[13]	Port E Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B7	1	reserved											
B8	1	IP	Interrupt Priority (bit addressable)	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	10000000	RW
B9	1	reserved											
BA	1	EP01STAT[13]	Endpoint 0&1 Status	0	0	0	0	0	EP1INBSY	EP1OUTBSY	EP0BSY	00000000	R
BB	1	GPIFTRIG[13, 11]	Endpoint 2,4,6,8 GPIF slave FIFO Trigger	DONE	0	0	0	0	RW	EP1	EP0	10000xxx	brrrrbbb
BC	1	reserved											
BD	1	GPIFSGLDATH[13]	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW

Note
13. SFRs not part of the standard 8051 architecture.
14. If no EEPROM is detected by the SIE then the default is 00000000.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
BE	1	GPIFSGLDATLX[13]	GPIF Data L w/ Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
BF	1	GPIFSGLDATL-NOX[13]	GPIF Data L w/ No Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
C0	1	SCON1[13]	Serial Port 1 Control (bit addressable)	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00000000	RW
C1	1	SBUF1[13]	Serial Port 1 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
C2	6	reserved											
C8	1	T2CON	Timer/Counter 2 Control (bit addressable)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00000000	RW
C9	1	reserved											
CA	1	RCAP2L	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CB	1	RCAP2H	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CC	1	TL2	Timer 2 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CD	1	TH2	Timer 2 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
CE	2	reserved											
D0	1	PSW	Program Status Word (bit addressable)	CY	AC	F0	RS1	RS0	OV	F1	P	00000000	RW
D1	7	reserved											
D8	1	EICON[13]	External Interrupt Control	SMOD1	1	ERESI	RESI	INT6	0	0	0	01000000	RW
D9	7	reserved											
E0	1	ACC	Accumulator (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
E1	7	reserved											
E8	1	EIE[13]	External Interrupt Enable(s)	1	1	1	EX6	EX5	EX4	EI²C	EUSB	11100000	RW
E9	7	reserved											
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
F1	7	reserved											
F8	1	EIP[13]	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	PI²C	PUSB	11100000	RW
F9	7	reserved											

R = all bits read-only
W = all bits write-only
r = read-only bit
w = write-only bit
b = both read/write bit

9. DC Characteristics

Table 14. DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
VCC	Supply Voltage		3.00	3.3	3.60	V
VCC Ramp Up	0 to 3.3V		200			µs
V_{IH}	Input HIGH Voltage		2		5.25	V
V_{IL}	Input LOW Voltage		–0.5		0.8	V
V_{IH_X}	Crystal Input HIGH Voltage		2		5.25	V
V_{IL_X}	Crystal Input LOW Voltage		–0.5		0.8	V
I_I	Input Leakage Current	0< V_{IN} < VCC			±10	µA
V_{OH}	Output Voltage HIGH	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current HIGH				4	mA
I_{OL}	Output Current LOW				4	mA
C_{IN}	Input Pin Capacitance	Except D+/D–			10	pF
		D+/D–			15	pF
I_{SUSP}	Suspend Current CY7C68014/CY7C68016	Connected		300	380[16]	µA
		Disconnected		100	150[16]	µA
	Suspend Current CY7C68013/CY7C68015	Connected		0.5	1.2[16]	mA
		Disconnected		0.3	1.0[16]	mA
I_{CC}	Supply Current	8051 running, connected to USB HS		50	85	mA
		8051 running, connected to USB FS		35	65	mA
T_{RESET}	Reset Time after Valid Power	VCC min = 3.0V	5.0			mS
	Pin Reset after powered on		200			µS

9.1 USB Transceiver

USB 2.0 compliant in full speed and high speed modes.

10. AC Electrical Characteristics

10.1 USB Transceiver

USB 2.0 compliant in full speed and high speed modes.

Note
16. Measured at Max VCC, 25°C.

10.3 Data Memory Read

Figure 13. Data Memory Read Timing Diagram

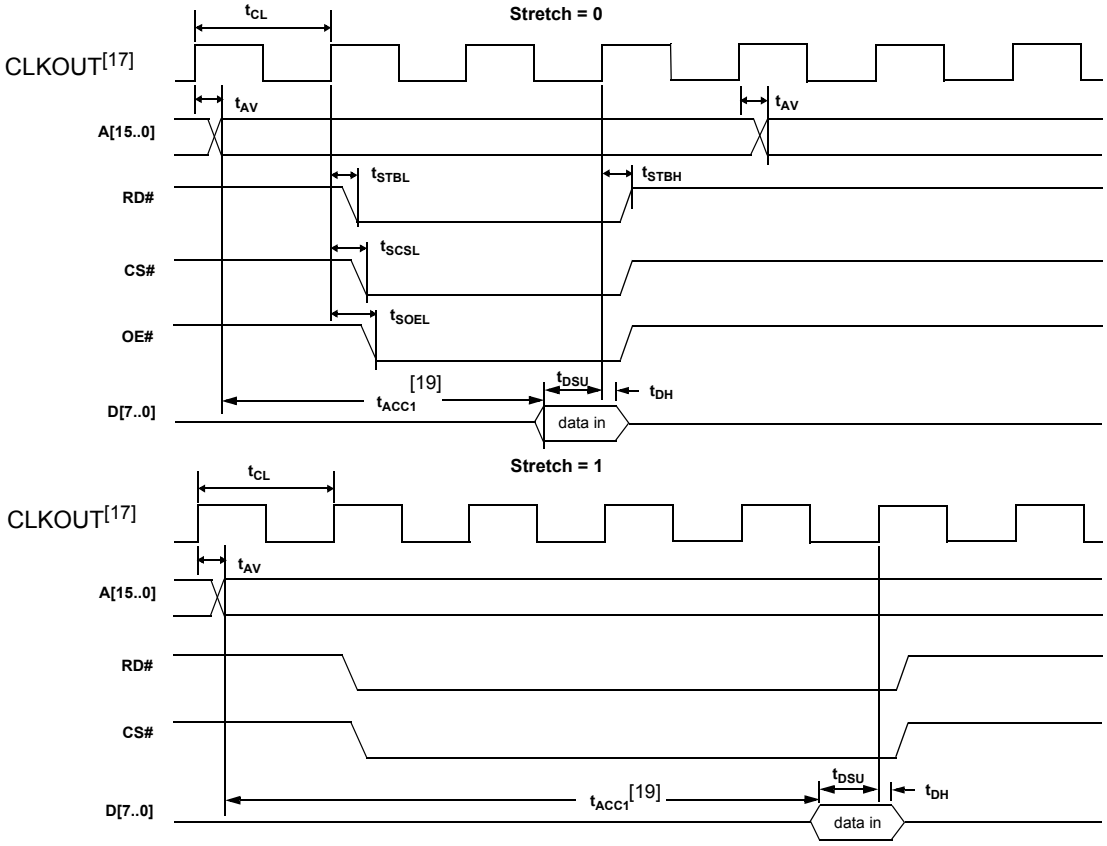


Table 16. Data Memory Read Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
t_{CL}	1/CLKOUT Frequency		20.83		ns	48 MHz
			41.66		ns	24 MHz
			83.2		ns	12 MHz
t_{AV}	Delay from Clock to Valid Address			10.7	ns	
t_{STBL}	Clock to RD LOW			11	ns	
t_{STBH}	Clock to RD HIGH			11	ns	
t_{SCSL}	Clock to CS LOW			13	ns	
t_{SOEL}	Clock to OE LOW			11.1	ns	
t_{DSU}	Data Setup to Clock	9.6			ns	
t_{DH}	Data Hold Time	0			ns	

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the above address valid time for which is based on the stretch value

Note

19. t_{ACC2} and t_{ACC3} are computed from the above parameters as follows:
t_{ACC2}(24 MHz) = 3*t_{CL} – t_{AV} –t_{DSU} = 106 ns
t_{ACC2}(48 MHz) = 3*t_{CL} – t_{AV} – t_{DSU} = 43 ns
t_{ACC3}(24 MHz) = 5*t_{CL} – t_{AV} –t_{DSU} = 190 ns
t_{ACC3}(48 MHz) = 5*t_{CL} – t_{AV} – t_{DSU} = 86 ns.

10.4 Data Memory Write

Figure 14. Data Memory Write Timing Diagram

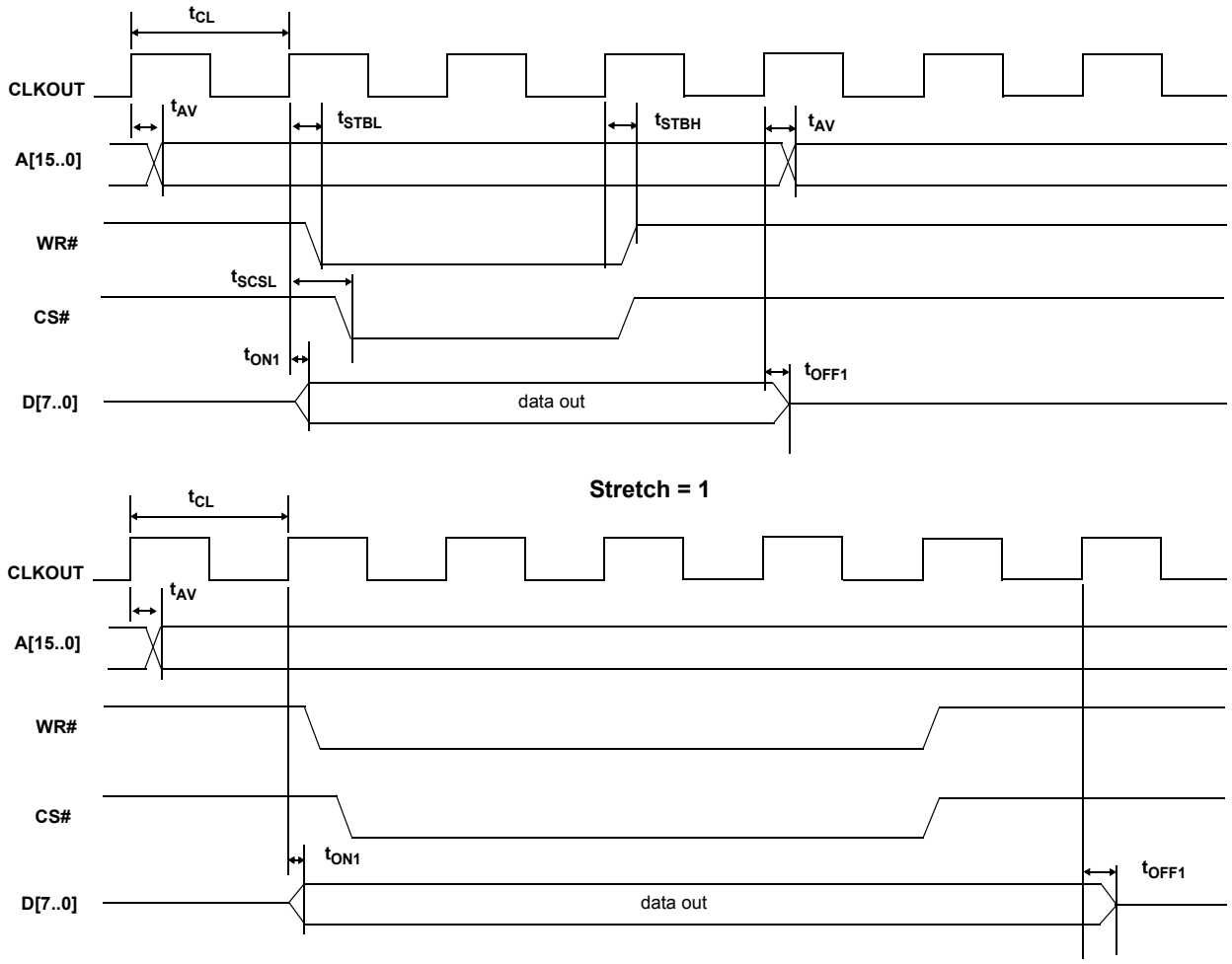


Table 17. Data Memory Write Parameters

Parameter	Description	Min	Max	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	10.7	ns	
t_{STBL}	Clock to WR Pulse LOW	0	11.2	ns	
t_{STBH}	Clock to WR Pulse HIGH	0	11.2	ns	
t_{SCSL}	Clock to CS Pulse LOW		13.0	ns	
t_{ON1}	Clock to Data Turn-on	0	13.1	ns	
t_{OFF1}	Clock to Data Hold Time	0	13.1	ns	

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the above address valid time for which is based on the stretch value.

10.6 GPIF Synchronous Signals

Figure 17. GPIF Synchronous Signals Timing Diagram[20]

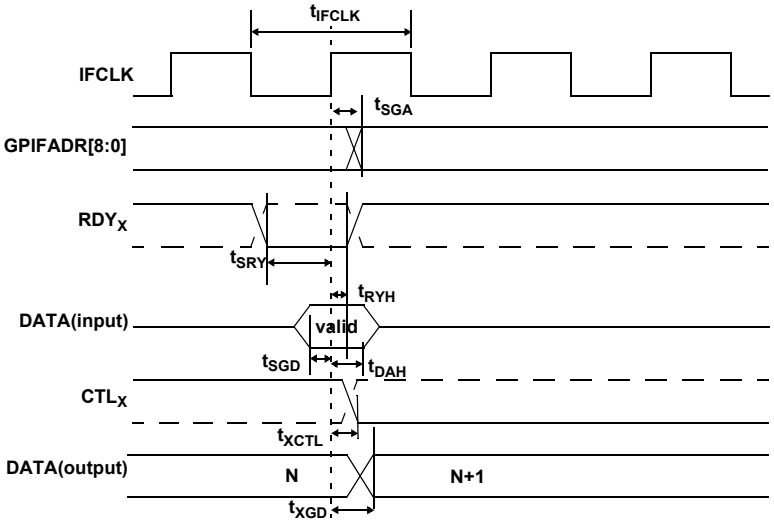


Table 18. GPIF Synchronous Signals Parameters with Internally Sourced IFCLK[20, 21]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83		ns
t_{SRY}	RDY_X to Clock Setup Time	8.9		ns
t_{RYH}	Clock to RDY_X	0		ns
t_{SGD}	GPIF Data to Clock Setup Time	9.2		ns
t_{DAH}	GPIF Data Hold Time	0		ns
t_{SGA}	Clock to GPIF Address Propagation Delay		7.5	ns
t_{XGD}	Clock to GPIF Data Output Propagation Delay		11	ns
t_{XCTL}	Clock to CTL_X Output Propagation Delay		6.7	ns

Table 19. GPIF Synchronous Signals Parameters with Externally Sourced IFCLK[21]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period[22]	20.83	200	ns
t_{SRY}	RDY_X to Clock Setup Time	2.9		ns
t_{RYH}	Clock to RDY_X	3.7		ns
t_{SGD}	GPIF Data to Clock Setup Time	3.2		ns
t_{DAH}	GPIF Data Hold Time	4.5		ns
t_{SGA}	Clock to GPIF Address Propagation Delay		11.5	ns
t_{XGD}	Clock to GPIF Data Output Propagation Delay		15	ns
t_{XCTL}	Clock to CTL_X Output Propagation Delay		10.7	ns

Notes
20. Dashed lines denote signals with programmable polarity.
21. GPIF asynchronous RDY_x signals have a minimum Setup time of 50 ns when using internal 48-MHz IFCLK.
22. IFCLK must not exceed 48 MHz.

10.9 Slave FIFO Synchronous Write

Figure 20. Slave FIFO Synchronous Write Timing Diagram[20]

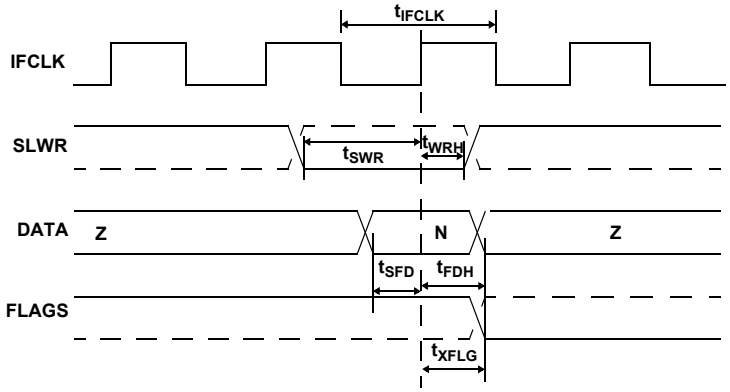


Table 23. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK[21]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83		ns
t_{SWR}	SLWR to Clock Setup Time	10.4		ns
t_{WRH}	Clock to SLWR Hold Time	0		ns
t_{SFD}	FIFO Data to Clock Setup Time	9.2		ns
t_{FDH}	Clock to FIFO Data Hold Time	0		ns
t_{XFLG}	Clock to FLAGS Output Propagation Time		9.5	ns

Table 24. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK[21]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SWR}	SLWR to Clock Setup Time	12.1		ns
t_{WRH}	Clock to SLWR Hold Time	3.6		ns
t_{SFD}	FIFO Data to Clock Setup Time	3.2		ns
t_{FDH}	Clock to FIFO Data Hold Time	4.5		ns
t_{XFLG}	Clock to FLAGS Output Propagation Time		13.5	ns

10.15 Slave FIFO Synchronous Address

Figure 27. Slave FIFO Synchronous Address Timing Diagram[20]

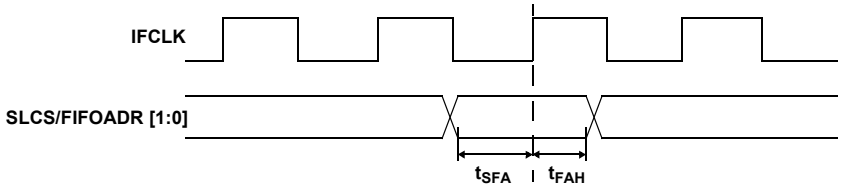


Table 31. Slave FIFO Synchronous Address Parameters [21]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	Interface Clock Period	20.83	200	ns
t_{SFA}	FIFOADR[1:0] to Clock Setup Time	25		ns
t_{FAH}	Clock to FIFOADR[1:0] Hold Time	10		ns

10.16 Slave FIFO Asynchronous Address

Figure 28. Slave FIFO Asynchronous Address Timing Diagram[20]

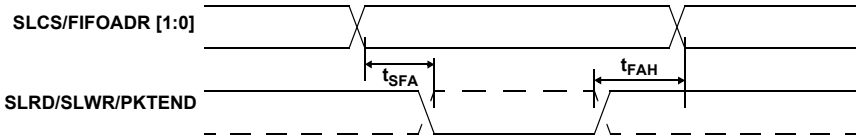


Table 32. Slave FIFO Asynchronous Address Parameters[23]

Parameter	Description	Min	Max	Unit
t_{SFA}	FIFOADR[1:0] to SLRD/SLWR/PKTEND Setup Time	10		ns
t_{FAH}	RD/WR/PKTEND to FIFOADR[1:0] Hold Time	10		ns

10.17.3 Sequence Diagram of a Single and Burst Asynchronous Read

Figure 32. Slave FIFO Asynchronous Read Sequence and Timing Diagram[20]

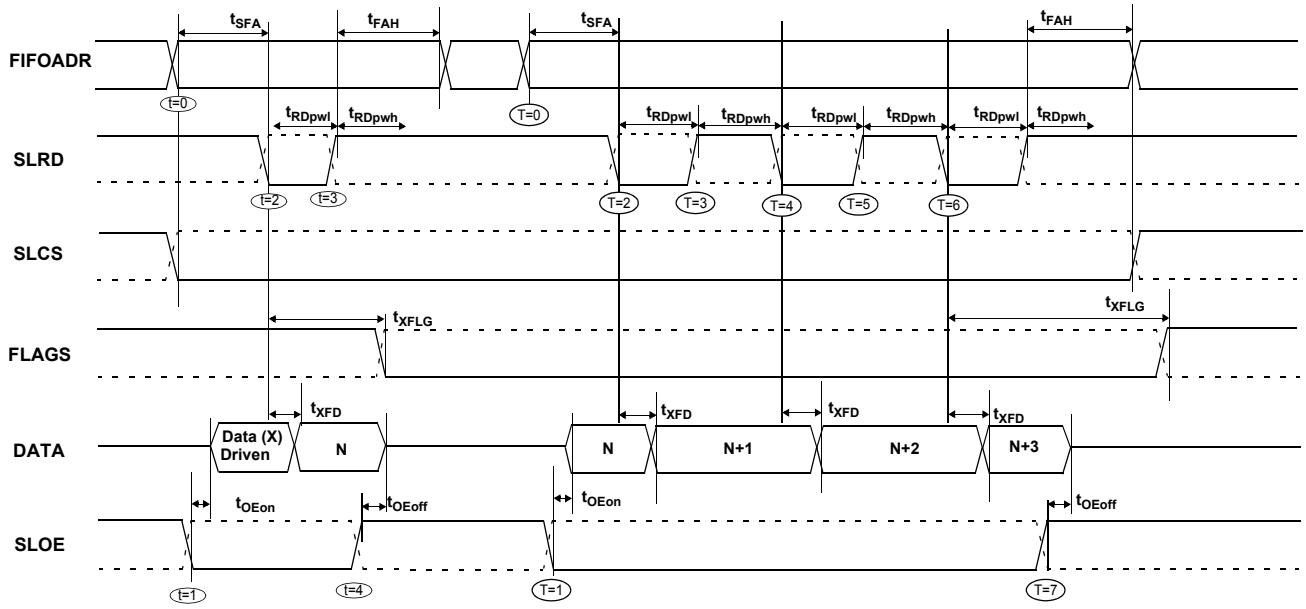


Figure 33. Slave FIFO Asynchronous Read Sequence of Events Diagram

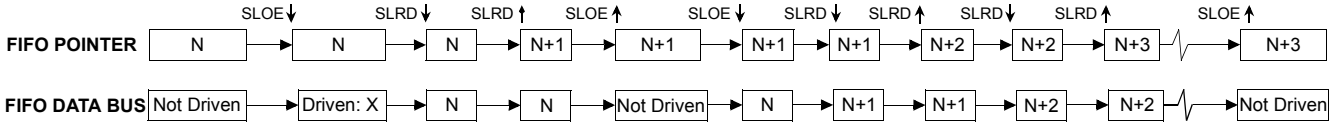


Figure 32 shows the timing relationship of the SLAVE FIFO signals during an asynchronous FIFO read. It shows a single read followed by a burst read.

- At t = 0 the FIFO address is stable and the SLCS signal is asserted.
- At t = 1, SLOE is asserted. This results in the data bus being driven. The data that is driven on to the bus is previous data, it data that was in the FIFO from a prior read cycle.
- At t = 2, SLRD is asserted. The SLRD must meet the minimum active pulse of t_{RDpwl} and minimum de-active pulse width of t_{RDpwh}. If SLCS is used then, SLCS must be asserted before SLRD is asserted (The SLCS and SLRD signals must both be asserted to start a valid read condition.)
- The data that is driven, after asserting SLRD, is the updated data from the FIFO. This data is valid after a propagation delay of t_{XFD} from the activating edge of SLRD. In Figure 32, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle (SLRD is asserted), SLOE must be in an asserted state. SLRD and SLOE can also be tied together.

The same sequence of events is also shown for a burst read marked with T = 0 through 5.

Note In burst read mode, during SLOE is assertion, the data bus is in a driven state and outputs the previous data. After SLRD is asserted, the data from the FIFO is driven on the data bus (SLOE must also be asserted) and then the FIFO pointer is incremented.

10.17.4 Sequence Diagram of a Single and Burst Asynchronous Write

Figure 34. Slave FIFO Asynchronous Write Sequence and Timing Diagram[20]

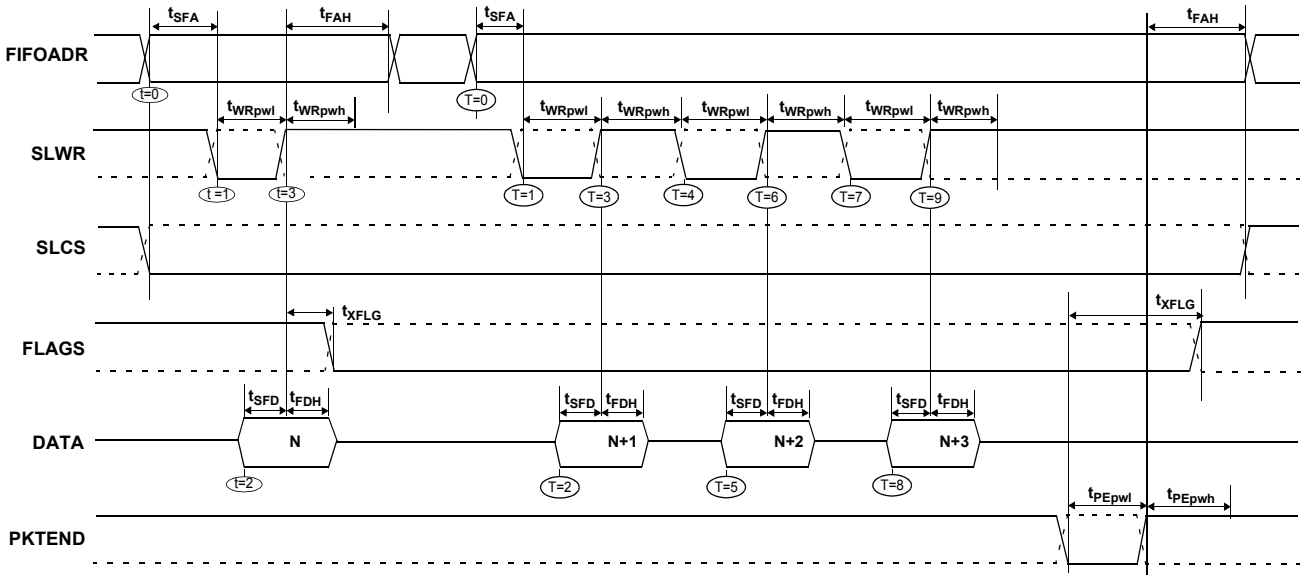


Figure 34 shows the timing relationship of the SLAVE FIFO write in an asynchronous mode. The diagram shows a single write followed by a burst write of 3 bytes and committing the 4 byte short packet using PKTEND.

- At t = 0 the FIFO address is applied, insuring that it meets the setup time of t_{SFA}. If SLCS is used, it must also be asserted (SLCS may be tied low in some applications).
- At t = 1 SLWR is asserted. SLWR must meet the minimum active pulse of t_{WRpwl} and minimum de-active pulse width of t_{WRpwh}. If the SLCS is used, it must be asserted with SLWR or before SLWR is asserted.
- At t = 2, data must be present on the bus t_{SFD} before the deasserting edge of SLWR.
- At t = 3, deasserting SLWR causes the data to be written from the data bus to the FIFO and then increments the FIFO pointer. The FIFO flag is also updated after t_{XFLG} from the deasserting edge of SLWR.

The same sequence of events are shown for a burst write and is indicated by the timing marks of T = 0 through 5.

Note In the burst write mode, after SLWR is deasserted, the data is written to the FIFO and then the FIFO pointer is incremented to the next byte in the FIFO. The FIFO pointer is post incremented.

In Figure 34 after the four bytes are written to the FIFO and SLWR is deasserted, the short 4 byte packet can be committed to the host using the PKTEND. The external device should be designed to not assert SLWR and the PKTEND signal at the same time. It should be designed to assert the PKTEND after SLWR is deasserted and met the minimum deasserted pulse width. The FIFOADDR lines have to held constant during the PKTEND assertion.

11. Ordering Information

Table 33. Ordering Information

Ordering Code	Package Type	RAM Size	# Prog I/Os	8051 Address /Data Busses
Ideal for battery powered applications				
CY7C68014A-128AXC	128 TQFP – Pb-Free	16K	40	16/8 bit
CY7C68014A-100AXC	100 TQFP – Pb-Free	16K	40	–
CY7C68014A-56PVXC	56 SSOP – Pb-Free	16K	24	–
CY7C68014A-56LFXC	56 QFN – Pb-Free	16K	24	–
CY7C68014A-56BAXC	56 VFBGA – Pb-Free	16K	24	–
CY7C68016A-56LFXC	56 QFN – Pb-Free	16K	26	–
Ideal for non-battery powered applications				
CY7C68013A-128AXC	128 TQFP – Pb-Free	16K	40	16/8 bit
CY7C68013A-128AXI	128 TQFP – Pb-Free (Industrial)	16K	40	16/8 bit
CY7C68013A-100AXC	100 TQFP – Pb-Free	16K	40	–
CY7C68013A-100AXI	100 TQFP – Pb-Free (Industrial)	16K	40	–
CY7C68013A-56PVXC	56 SSOP – Pb-Free	16K	24	–
CY7C68013A-56PVXI	56 SSOP – Pb-Free (Industrial)	16K	24	–
CY7C68013A-56LFXC	56 QFN – Pb-Free	16K	24	–
CY7C68013A-56LFXI	56 QFN – Pb-Free (Industrial)	16K	24	–
CY7C68015A-56LFXC	56 QFN – Pb-Free	16K	26	–
CY7C68013A-56BAXC	56 VFBGA – Pb-Free	16K	24	–
CY7C68013A-56LTXC	56 QFN	16K	24	–
CY7C68013A-56LTXCT	56 QFN	16K	24	–
CY7C68013A-56LTXI	56 QFN	16K	24	–
CY7C68014A-56LTXC	56 QFN	16K	24	–
CY7C68015A-56LTXC	56 QFN	16K	24	–
CY7C68016A-56LTXC	56 QFN	16K	24	–
CY7C68016A-56LTXCT	56 QFN	16K	24	–
Development Tool Kit				
CY3684	EZ-USB FX2LP Development Kit			
Reference Design Kit				
CY4611B	USB 2.0 to ATA/ATAPI Reference Design using EZ-USB FX2LP			

12. Package Diagrams

The FX2LP is available in five packages:

- 56-pin SSOP
- 56-pin QFN
- 100-pin TQFP
- 128-pin TQFP
- 56-ball VFBGA

Package Diagrams

Figure 35. 56-Pin Shrunk Small Outline Package O56 (51-85062)