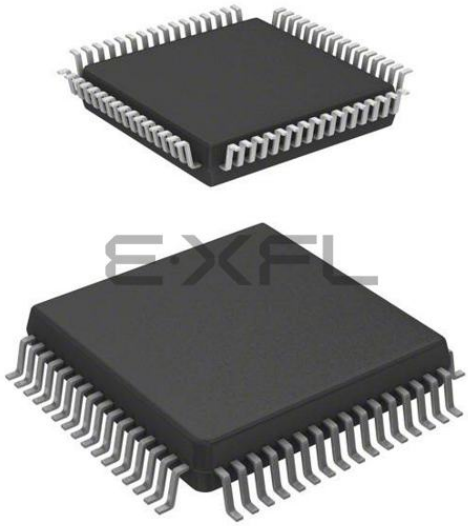

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | H8/300H |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | I²C, SCI |
| Peripherals | PWM, WDT |
| Number of I/O | 29 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | External |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-BQFP |
| Supplier Device Package | 64-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3664hv |

# Preface

The H8/3664 Group are single-chip microcomputers made up of the high-speed H8/300H CPU employing Renesas Technology original architecture as their cores, and the peripheral functions required to configure a system. The H8/300H CPU has an instruction set that is compatible with the H8/300 CPU.

Target Users: This manual was written for users who will be using the H8/3664 Group in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the H8/3664 Group to the target users.
Refer to the H8/300H Series Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the CPU's functions
  Read the H8/300H Series Software Manual.
- In order to understand the details of a register when its name is known
  Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bits, and initial values of the registers are summarized in section 19, List of Registers.
  Example: Bit order: The MSB is on the left and the LSB is on the right.

Notes:

When using the on-chip emulator (E7, E8) for H8/3664 program development and debugging, the following restrictions must be noted.

1. The $\overline{\text{NMI}}$ pin is reserved for the E7 or E8, and cannot be used.
2. Pins P85, P86, and P87 cannot be used. In order to use these pins, additional hardware must be provided on the user board.
3. Area H'7000 to H'7FFF is used by the E7 or E8, and is not available to the user.

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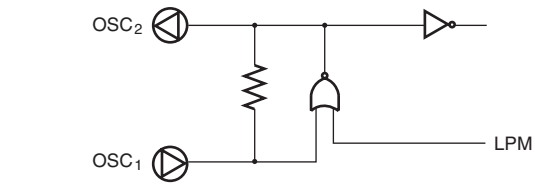
## 5.1 System Clock Generator

Clock pulses can be supplied to the system clock divider either by connecting a crystal or ceramic resonator, or by providing external clock input. Figure 5.2 shows a block diagram of the system clock generator.

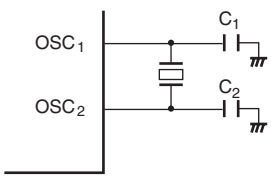



LPM: Lo -po er mode ( andb mode, bac i e mode, b leep mode)

**Figure 5.2 Block Diagram of System Clock Generator**

### 5.1.1 Connecting Crystal Resonator

Figure 5.3 shows a typical method of connecting a crystal resonator. An AT-cut parallel-resonance crystal resonator should be used. Figure 5.4 shows the equivalent circuit of a crystal resonator. A resonator having the characteristics given in table 5.1 should be used.




$C_1 = C_2 = 12$ pF 20%

No e: Capaci ance are reference al e .

**Figure 5.3 Typical Connection to Crystal Resonator**

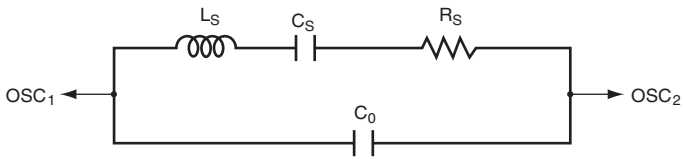



**Figure 5.4 Equivalent Circuit of Crystal Resonator**

### 6.1.2 System Control Register 2 (SYSCR2)

SYSCR2 controls the power-down modes, as well as SYSCR1.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | SMSEL | 0 | R/W | Sleep Mode Selec ion |
| 6 | LSON | 0 | R/W | Lo Speed on Flag |
| 5 | DTON | 0 | R/W | Direc Tran fer on Flag<br>The e bi elec he mode o ran i af er he e ec ion of a SLEEP in r c ion, a ell a bi SSBY of SYSCR1.<br>For de ail , ee able 6.2. |
| 4 | MA2 | 0 | R/W | Ac i e Mode Clock Selec 2 o 0 |
| 3 | MA1 | 0 | R/W | The e bi elec he opera ing clock freq enc in ac i e and leep mode . The opera ing clock freq enc change o he e freq enc af er he SLEEP in r c ion i e ec ed.<br>0XX: $\varphi_{osc}$<br>100: $\varphi_{osc}/8$<br>101: $\varphi_{osc}/16$<br>110: $\varphi_{osc}/32$<br>111: $\varphi_{osc}/64$ |
| 2 | MA0 | 0 | R/W | |
| 1 | SA1 | 0 | R/W | S bac i e Mode Clock Selec 1 and 0 |
| 0 | SA0 | 0 | R/W | The e bi elec he opera ing clock freq enc in bac i e and b leep mode . The opera ing clock freq enc change o he e freq enc af er he SLEEP in r c ion i e ec ed.<br>00: $\varphi_w/8$<br>01: $\varphi_w/4$<br>1X: $\varphi_w/2$ |

[Legend]

X: Don care.

**Table 6.2 Transition Mode after SLEEP Instruction Execution and Interrupt Handling**

| DTON | SSBY | SMSEL | LSON | Transition Mode after SLEEP Instruction Execution | Transition Mode due to Interrupt |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Sleep mode | Ac i e mode |
| | | | 1 | | S bac i e mode |
| | | 1 | 0 | S b leep mode | Ac i e mode |
| | | | 1 | | S bac i e mode |
| | 1 | X | X | S andb mode | Ac i e mode |
| 1 | X | 0* | 0 | Ac i e mode (direc ran i ion) | |
| | X | X | 1 | S bac i e mode (direc ran i ion) | |

[Legend]

X: Don care.

No e: * When a a e ran i ion i performed hile SMSEL i 1, imer V, SCI3, and he A/D con er er are re e , and all regi er are e o heir ini ial al e . To e he e f nc ion af er en ering ac i e mode, re e he regi er .

# Section 7 ROM

The features of the 32-kbyte flash memory built into the flash memory version are summarized below.

- Programming/erase methods

  The flash memory is programmed 128 bytes at a time. Erase is performed in single-block units. The flash memory is configured as follows: 1 kbyte ×4 blocks and 28 kbytes ×1 block. To erase the entire flash memory, each block must be erased in turn.
- Reprogramming capability

  The flash memory can be reprogrammed up to 1,000 times.
- On-board programming

  On-board programming/erasing can be done in boot mode, in which the boot program built into the chip is started to erase or program of the entire flash memory. In normal user program mode, individual blocks can be erased or programmed.
- Programmer mode

  Flash memory can be programmed/erased in programmer mode using a PROM programmer, as well as in on-board programming mode.
- Automatic bit rate adjustment

  For data transfer in boot mode, this LSI's bit rate can be automatically adjusted to match the transfer bit rate of the host.
- Programming/erasing protection

  Sets software protection against flash memory programming/erasing.
- Power-down mode

  Operation of the power supply circuit can be partly halted in subactive mode. As a result, flash memory can be read with low power consumption.

### 14.6.1 Multiprocessor Serial Data Transmission

Figure 14.16 shows a sample flowchart for multiprocessor serial data transmission. For an ID transmission cycle, set the MPBT bit in SSR to 1 before transmission. For a data transmission cycle, clear the MPBT bit in SSR to 0 before transmission. All other SCI3 operations are the same as those in asynchronous mode.

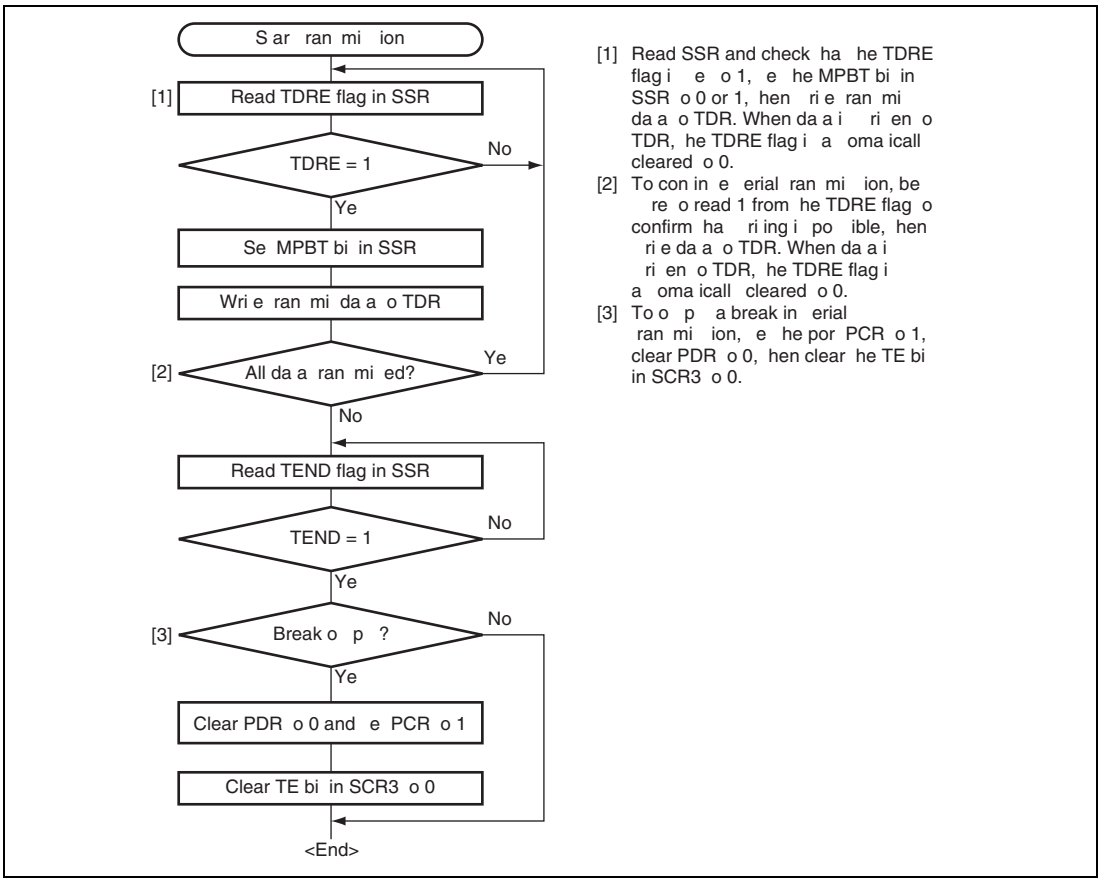



**Figure 14.16 Sample Multiprocessor Serial Transmission Flowchart**

5. Read ICDR and clear the IRIC flag in ICCR to 0. The RDRF flag is cleared to 0.

Receive operations can be performed continuously by repeating steps [4] and [5]. When SDA is changed from low to high when SCL is high, and the stop condition is detected, the BBSY flag in ICCR is cleared to 0.

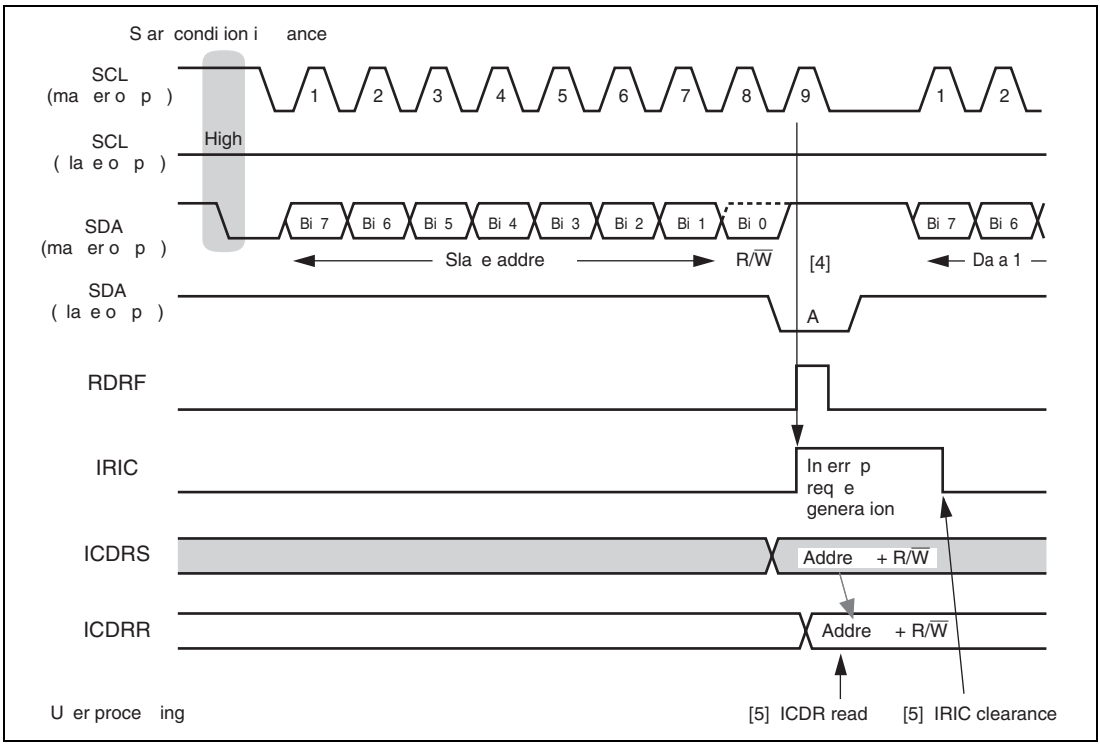



**Figure 15.7 Example of Slave Receive Mode Operation Timing (1)**
**(MLS = ACKB = 0)**

## Table 15.7 I²C Bus Timing (with Maximum Influence of $t_{sr}/t_{sf}$)

| | | | Time Indication (at Maximum Transfer Rate) [ns] | | | | | |
|---|---|---|---|---|---|---|---|---|
| Item | $t_{cyc}$ Indication | | $t_{sr}/t_{sf}$ Influence (Max.) | I²C Bus Specifi-cation (Min.) | φ= 5 MHz | φ= 8 MHz | φ= 10 MHz | φ= 16 MHz |
| SCLHO | 0.5 SCLO ( Sr) | S andard mode | 1000 | 4000 | 4000 | 4000 | 4000 | 4000 |
| | | High- peed mode | 300 | 600 | 950 | 950 | 950 | 950 |
| SCLLO | 0.5 SCLO ( Sf ) | S andard mode | 250 | 4700 | 4750 | 4750 | 4750 | 4750 |
| | | High- peed mode | 250 | 1300 | 1000*1 | 1000*1 | 1000*1 | 1000*1 |
| BUFO | 0.5 SCLO 1 c c ( Sr ) | S andard mode | 1000 | 4700 | 3800*1 | 3875*1 | 3900*1 | 3938*1 |
| | | High- peed mode | 300 | 1300 | 750*1 | 825*1 | 850*1 | 888*1 |
| STAHO | 0.5 SCLO 1 c c ( Sf ) | S andard mode | 250 | 4000 | 4550 | 4625 | 4650 | 4688 |
| | | High- peed mode | 250 | 600 | 800 | 875 | 900 | 938 |
| STASO | 1 SCLO ( Sr ) | S andard mode | 1000 | 4700 | 9000 | 9000 | 9000 | 9000 |
| | | High- peed mode | 300 | 600 | 2200 | 2200 | 2200 | 2200 |
| STOSO | 0.5 SCLO + 2 c c ( Sr ) | S andard mode | 1000 | 4000 | 4400 | 4250 | 4200 | 4125 |
| | | High- peed mode | 300 | 600 | 1350 | 1200 | 1150 | 1075 |
| SDASO (ma er) | 1 SCLLO*2 3 c c ( Sr ) | S andard mode | 1000 | 250 | 3100 | 3325 | 3400 | 3513 |
| | | High- peed mode | 300 | 100 | 400 | 625 | 700 | 813 |
| SDASO ( la e) | 1 SCLL*2 3 c c ( Sr ) | S andard mode | 1000 | 250 | 3100 | 3325 | 3400 | 3513 |
| | | High- peed mode | 300 | 100 | 400 | 625 | 700 | 813 |
| SDAHO | 3 c c | S andard mode | 0 | 0 | 600 | 375 | 300 | 188 |
| | | High- peed mode | 0 | 0 | 600 | 375 | 300 | 188 |

No e : 1. Doe no mee he I²C b in erface pecifica ion

2. Calc la ed ing he I²C b pecifica ion al e ( andard mode: 4700 n min.; high-peed mode: 1300 n min.).

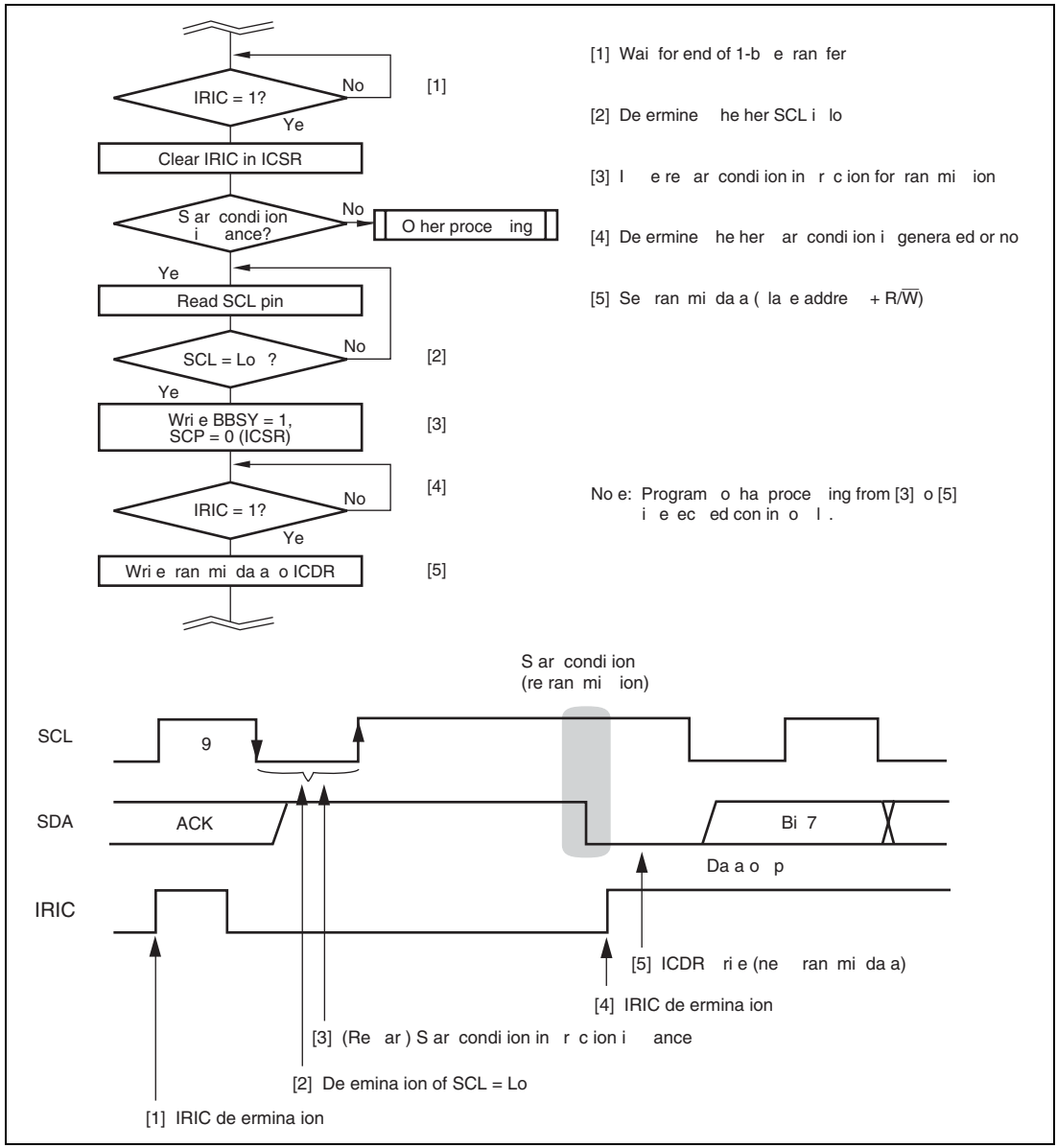



**Figure 15.17 Flowchart and Timing of Start Condition Instruction Issuance for Retransmission**

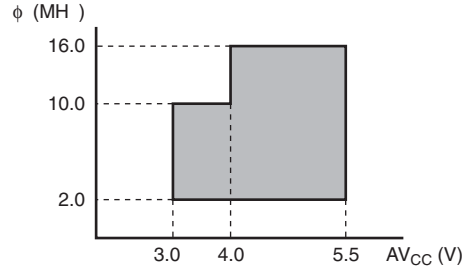
| Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Module Name |
|---|---|---|---|---|---|---|---|---|---|
| PDR7 | | P76 | P75 | P74 | | | | | I/O por |
| PDR8 | P87 | P86 | P85 | P84 | P83 | P82 | P81 | P80 | |
| PDRB | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 | |
| PMR1 | IRQ3 | IRQ2 | IRQ1 | IRQ0 | | | TXD | TMOW | |
| PMR5 | | | WKP5 | WKP4 | WKP3 | WKP2 | WKP1 | WKP0 | |
| PCR1 | PCR17 | PCR16 | PCR15 | PCR14 | | PCR12 | PCR11 | PCR10 | |
| PCR2 | | | | | | PCR22 | PCR21 | PCR20 | |
| PCR5 | PCR57*[2] | PCR56*[2] | PCR55 | PCR54 | PCR53 | PCR52 | PCR51 | PCR50 | |
| PCR7 | | PCR76 | PCR75 | PCR74 | | | | | |
| PCR8 | PCR87 | PCR86 | PCR85 | PCR84 | PCR83 | PCR82 | PCR81 | PCR80 | |
| SYSCR1 | SSBY | STS2 | STS1 | STS0 | NESEL | | | | Po er-do n |
| SYSCR2 | SMSEL | LSON | DTON | MA2 | MA1 | MA0 | SA1 | SA0 | |
| IEGR1 | NMIEG | | | | IEG3 | IEG2 | IEG1 | IEG0 | In err p |
| IEGR2 | | | WPEG5 | WPEG4 | WPEG3 | WPEG2 | WPEG1 | WPEG0 | |
| IENR1 | IENDT | IENTA | IENWP | | IEN3 | IEN2 | IEN1 | IEN0 | |
| IRR1 | IRRDT | IRRTA | | | IRRI3 | IRRI2 | IRRI1 | IRRI0 | |
| IWPR | | | IWPF5 | IWPF4 | IWPF3 | IWPF2 | IWPF1 | IWPF0 | |
| MSTCR1 | | MSTIIC | MSTS3 | MSTAD | MSTWD | MSTTW | MSTTV | MSTTA | Po er-do n |
| TSCR | | | | | | | IICRST | IICX | IIC |

No e : 1. WDT: Wa chdog imer
2. Thi bi i no incl ded in H8/3664N.

- EEPROM

| Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Module Name |
|---|---|---|---|---|---|---|---|---|---|
| EKR | EKR7 | EKR6 | EKR5 | EKR4 | EKR3 | EKR2 | EKR1 | EKR0 | EEPROM |

**Analog Power Supply Voltage and A/D Converter Accuracy Guarantee Range:**




### 20.3.2 DC Characteristics

**Table 20.10 DC Characteristics (1)**

$V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C unless otherwise indicated.

| Item | Symbol | Applicable Pins | Test Condition | Values Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Inp high ol age | $V_{IH}$ | RES, NMI, WKP0 o WKP5, IRQ0 o IRQ3, ADTRG, TMRIV, TMCIV, FTCI, FTIOA o FTIOD, SCK3, TRGV | $V_{CC}$ = 4.0 V o 5.5 V | $V_{CC}$ ×0.8 | | $V_{CC}$ + 0.3 | V | |
| | | | | $V_{CC}$ ×0.9 | | $V_{CC}$ + 0.3 | V | |
| | | RXD, SCL, SDA, P10 o P12, P14 o P17, P20 o P22, P50 o P57, P74 o P76, P80 o P87 | $V_{CC}$ = 4.0 V o 5.5 V | $V_{CC}$ ×0.7 | | $V_{CC}$ + 0.3 | V | |
| | | | | $V_{CC}$ ×0.8 | | $V_{CC}$ + 0.3 | V | |
| | | PB0 o PB7 | $V_{CC}$ = 4.0 V o 5.5 V | $V_{CC}$ ×0.7 | | $AV_{CC}$ + 0.3 | V | |
| | | | | $V_{CC}$ ×0.8 | | $AV_{CC}$ + 0.3 | V | |
| | | OSC1 | $V_{CC}$ = 4.0 V o 5.5 V | $V_{CC}$ 0.5 | | $V_{CC}$ + 0.3 | V | |
| | | | | $V_{CC}$ 0.3 | | $V_{CC}$ + 0.3 | V | |

## 20.5 Output Load Condition

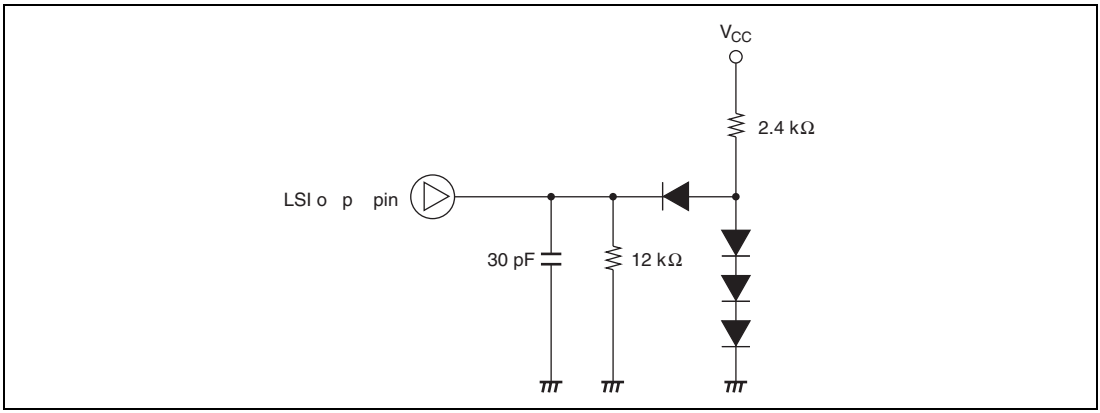



**Figure 20.8 Output Load Circuit**

## A.3 Number of Execution States

The status of execution for each instruction of the H8/300H CPU and the method of calculating the number of states required for instruction execution are shown below. Table A.4 shows the number of cycles of each type occurring in each instruction, such as instruction fetch and data read/write. Table A.3 shows the number of states required for each cycle. The total number of states required for execution of an instruction can be calculated by the following expression:

$$E\ ec\ \ ion\ \ a\ e\ \ = I\ \times S_I + J\ \times S_J + K\ \times S_K + L\ \times S_L + M\ \times S_M + N\ \times S_N$$

**Examples:** When instruction is fetched from on-chip ROM, and an on-chip RAM is accessed.

BSET #0, @FF00

From table A.4:
I = L = 2, J = K = M = N= 0

From table A.3:
$S_I = 2$, $S_L = 2$

Number of states required for execution = $2\ \times 2 + 2\ \times 2 = 8$

When instruction is fetched from on-chip ROM, branch address is read from on-chip ROM, and on-chip RAM is used for stack area.

JSR @@ 30

From table A.4:
I = 2, J = K = 1, L = M = N = 0

From table A.3:
$S_I = S_J = S_K = 2$

Number of states required for execution = $2\ \times 2 + 1\ \times 2 + 1\ \times 2 = 8$

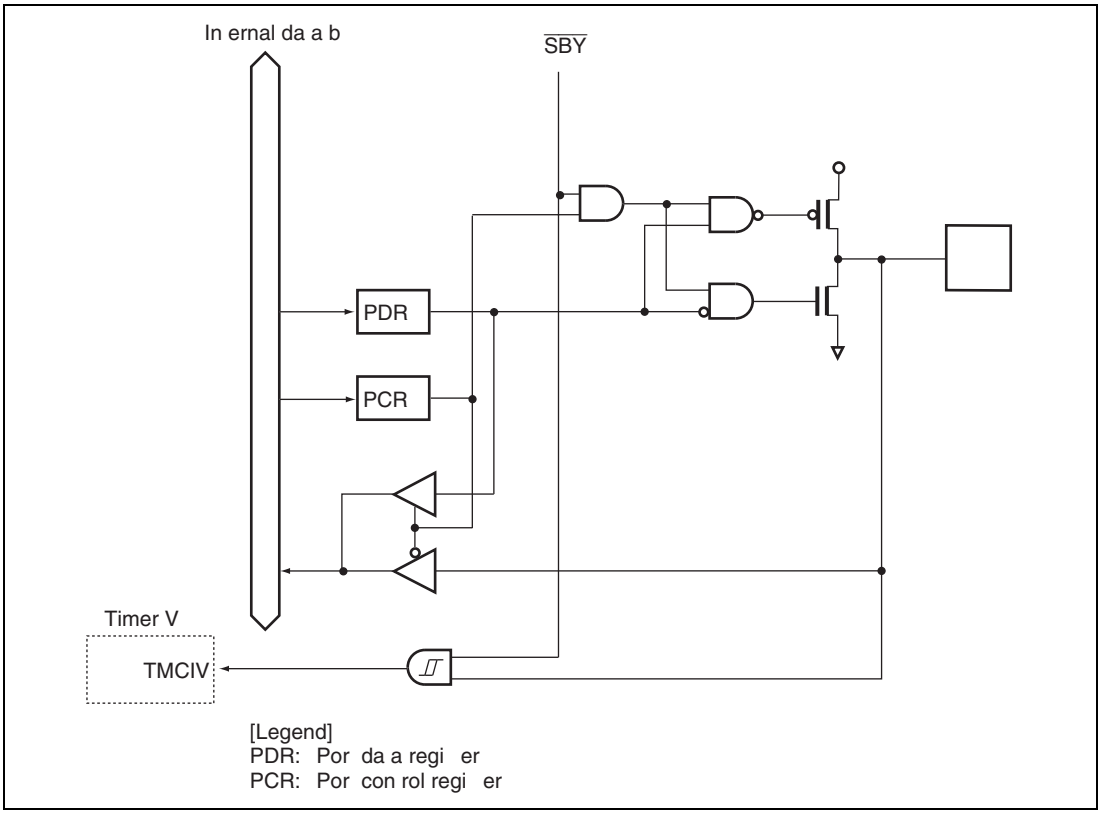



**Figure B.12 Port 7 Block Diagram (P75)**