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Details

Product Status	Last Time Buy
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Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Table 4.10. ADC0 Electrical Characteristics (Continued)

 V_{DD} = 1.8 to 3.6V V, VREF = 1.65 V (REFSL[1:0] = 11), -40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Тур	Max	Units
Analog Inputs	•				
ADC Input Voltage Range	Single Ended (AIN+ – GND)	0		VREF	V
Absolute Pin Voltage with respect to GND	Single Ended	0	_	V _{DD}	V
Sampling Capacitance (C8051F912/11/02/01)	1x Gain 0.5x Gain	—	28 26	—	pF
Input Multiplexer Impedance		—	5	—	kΩ
Power Specifications	•				
Power Supply Current (V _{DD} supplied to ADC0)	Conversion Mode (300 ksps) Tracking Mode (0 ksps)	_	720 680	_	μA
Power Supply Rejection	Internal High Speed VREF External VREF	_	67 74	_	dB
Notes:	<u>.</u>		•		

1. Blue indicates a feature only available on 'F912 and 'F902 devices.

2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.

3. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code.

4. Performance in 8-bit mode is similar to 10-bit mode.

Table 4.11. Temperature Sensor Electrical Characteristics

 V_{DD} = 1.8 to 3.6V V, -40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Тур	Max	Units
Linearity		_	±1	—	°C
Slope		_	3.40	_	mV/°C
Slope Error ¹		_	40	_	µV/°C
Offset	Temp = 25 °C	_	1025	_	mV
Offset Error ¹	Temp = 25 °C	_	18	_	mV
Temperature Sensor Settling	Initial Voltage=0 V	—	—	3.0	μs
Time ²	Initial Voltage=3.6 V			6.5	
Supply Current		_	35	—	μA

Notes:

1. Represents one standard deviation from the mean.

2. The temperature sensor settling time, resulting from an ADC mux change or enabling of the temperature sensor, varies with the voltage of the previously sampled channel and can be up to 6 µs if the previously sampled channel voltage was greater than 3 V. To minimize the temperature sensor settling time, the ADC mux can be momentarily set to ground before being set to the temperature sensor output. This ensures that the temperature sensor output will settle in 3 µs or less.



SFR Definition 5.2. ADC0CF: ADC0 Configuration

Bit	7 6 5 4 3 2 1							0
Name	•		AD0SC[4:0]			AD08BE	AD0TM	AMP0GN
Туре			R/W			R/W	R/W	R/W
Rese	t 1	1	1	1	1	0	0	0
SFR P	age = 0x0; SF	R Address =	= 0xBC					
Bit	Name				Function			
7:3	AD0SC[4:0]	ADC0 SAR Conversion Clock Divider. SAR Conversion clock is derived from FCLK by the following equation, where ADOSC refers to the 5-bit value held in bits ADOSC[4:0]. SAR Conversion clock requirements are given in Table 4.10. BURSTEN = 0: FCLK is the current system clock. BURSTEN = 1: FCLK is the 20 MHz low power oscillator, independent of the system clock. $ADOSC = \frac{FCLK}{CLK_{SAR}} - 1 *$ *Round the result up. or $CLK_{SAR} = \frac{FCLK}{AD0SC + 1}$					here h clock the system	
2	AD08BE	ADC0 8-Bit 0: ADC0 op 1: ADC0 op	ADC0 8-Bit Mode Enable. 0: ADC0 operates in 10-bit mode (normal operation). 1: ADC0 operates in 8-bit mode.					
1	AD0TM AMP0GN	 ADC0 Track Mode. Selects between Normal or Delayed Tracking Modes. 0: Normal Track Mode: When ADC0 is enabled, conversion begins immediately following the start-of-conversion signal. 1: Delayed Track Mode: When ADC0 is enabled, conversion begins 3 SAR clock cycles following the start-of-conversion signal. The ADC is allowed to track during this time. ADC0 Gain Control. 						
		0: The on-c 1: The on-c	hip PGA gai hip PGA gai	n is 0.5. n is 1.				



5.6.1. Window Detector In Single-Ended Mode

Figure 5.5 shows two example window comparisons for right-justified with data. ADC0LTH:ADC0LTL = 0x0080 (128d) and ADC0GTH:ADC0GTL = 0x0040 (64d). The input voltage can range from 0 to VREF x (1023/1024) with respect to GND, and is represented by a 10-bit unsigned integer value. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0040 < ADC0H:ADC0L < 0x0080). In the right example, and AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0040 or ADC0H:ADC0L > 0x0080). Figure 5.6 shows an example using leftjustified data with the same comparison values.



Figure 5.5. ADC Window Compare Example: Right-Justified Single-Ended Data



Figure 5.6. ADC Window Compare Example: Left-Justified Single-Ended Data

5.6.2. ADC0 Specifications

See "4. Electrical Characteristics" on page 36 for a detailed listing of ADC0 specifications.



7.5. Comparator Register Descriptions

The SFRs used to enable and configure the comparators are described in the following register descriptions. A Comparator must be enabled by setting the CPnEN bit to logic 1 before it can be used. From an enabled state, a comparator can be disabled and placed in a low power state by clearing the CPnEN bit to logic 0.

Important Note About Comparator Settings: False rising and falling edges can be detected by the Comparator while powering on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed. The Comparator Power Up Time is specified in Section "Table 4.14. Comparator Electrical Characteristics" on page 58.

SFR Definition 7.1. CPT0CN: Comparator 0 Control

Bit	7	6	5	4	3	2	1	0
Name	CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0H	YP[1:0]	CP0H	/N[1:0]
Туре	R/W	R	R/W	R/W	R/W		R/	W
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0x9B

Bit	Name	Function
7	CP0EN	Comparator0 Enable Bit.
		1: Comparator0 Disabled.
6	CP0OUT	Comparator0 Output State Flag.
		0: Voltage on CP0+ < CP0
		1: Voltage on CP0+ > CP0
5	CP0RIF	Comparator0 Rising-Edge Flag. Must be cleared by software.
		0: No Comparator0 Rising Edge has occurred since this flag was last cleared.
		1: Comparator0 Rising Edge has occurred.
4	CP0FIF	Comparator0 Falling-Edge Flag. Must be cleared by software.
		0: No Comparator0 Falling-Edge has occurred since this flag was last cleared.1: Comparator0 Falling-Edge has occurred.
3-2	CP0HYP[1:0]	Comparator0 Positive Hysteresis Control Bits.
		00: Positive Hysteresis Disabled.
		01: Positive Hysteresis = Hysteresis 1.
		10: Positive Hysteresis = Hysteresis 2.
		TT. Positive Hysteresis = Hysteresis 5 (Maximum).
1:0	CP0HYN[1:0]	Comparator0 Negative Hysteresis Control Bits.
		00: Negative Hysteresis Disabled.
		10. Negative Hysteresis = Π ysteresis 1. 10. Negative Hysteresis = Hysteresis 2
		11: Negative Hysteresis = Hysteresis 3 (Maximum).



Mnemonic	Description	Bytes	Clock Cycles
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	2	2/3
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4
	Program Branching		•
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

Table 8.1. CIP-51 Instruction Set Summary (Continued)



11. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the C8051F91x-C8051F90x's resources and peripherals. The CIP-51 controller core duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the C8051F91x-C8051F90x. This allows the addition of new functionality while retaining compatibility with the MCS-51[™] instruction set. Table 11.1 and Table 11.2 list the SFRs implemented in the C8051F91x-C8051F90x device family.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g., P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 11.3, for a detailed description of each register.

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
F0	В	P0MDIN	P1MDIN		SMB0ADR	SMB0ADM	EIP1	EIP2
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	FLWR	EIE1	EIE2
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	PCA0PWM
D0	PSW	REF0CN	PCA0CPL5	PCA0CPH5	P0SKIP	P1SKIP		P0MAT
C8	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	PCA0CPM5	P1MAT
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	P0MASK
B8	IP	IREF0CN	ADC0AC	ADC0MX	ADC0CF	ADC0L	ADC0H	P1MASK
B0	SPI1CN	OSCXCN	OSCICN	OSCICL		PMU0CF	FLSCL	FLKEY
A8	IE	CLKSEL	EMI0CN		RTC0ADR	RTC0DAT	RTC0KEY	
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	POMDOUT	P1MDOUT	P2MDOUT	SFRPAGE
98	SCON0	SBUF0	CPT1CN	CPT0CN	CPT1MD	CPT0MD	CPT1MX	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	DC0CF	DC0CN
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	SPI1CFG	SPI1CKR	SPI1DAT	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

Table 11.1. Special Function Register (SFR) Memory Map (Page 0x0)

(bit addressable)



12.6. External Interrupts INT0 and INT1

The INTO and INT1 external interrupt sources are configurable as active high or low, edge or level sensitive. The INOPL (INT0 Polarity) and IN1PL (INT1 Polarity) bits in the IT01CF register select active high or active low; the IT0 and IT1 bits in TCON (Section "25.1. Timer 0 and Timer 1" on page 272) select level or edge sensitive. The table below lists the possible configurations.

IT0	IN0PL	INT0 Interrupt		
1	0	Active low, edge sensitive		
1	1	Active high, edge sensitive		
0	0	Active low, level sensitive		
0	1	Active high, level sensitive		

IT1	IN1PL	INT1 Interrupt		
1	0	Active low, edge sensitive		
1	1	Active high, edge sensitive		
0	0	Active low, level sensitive		
0	1	Active high, level sensitive		

INT0 and INT1 are assigned to Port pins as defined in the IT01CF register (see SFR Definition 12.7). Note that INT0 and INT0 Port pin assignments are independent of any Crossbar assignments. INT0 and INT1 will monitor their assigned Port pins without disturbing the peripheral that was assigned the Port pin via the Crossbar. To assign a Port pin only to INT0 and/or INT1, configure the Crossbar to skip the selected pin(s). This is accomplished by setting the associated bit in register XBR0 (see Section "21.3. Priority Crossbar Decoder" on page 209 for complete details on configuring the Crossbar).

IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flags for the INT0 and INT1 external interrupts, respectively. If an INT0 or INT1 external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag remains logic 1 while the input is active as defined by the corresponding polarity bit (IN0PL or IN1PL); the flag remains logic 0 while the input is inactive. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.



13.5. Flash Write and Erase Guidelines

Any system which contains routines which write or erase Flash memory from software involves some risk that the write or erase routines will execute unintentionally if the CPU is operating outside its specified operating range of VDD, system clock frequency, or temperature. This accidental execution of Flash modifying code can result in alteration of Flash memory contents causing a system failure that is only recoverable by re-Flashing the code in the device.

To help prevent the accidental modification of Flash by firmware, the VDD Monitor must be enabled and enabled as a reset source on C8051F91x-C8051F90x devices for the Flash to be successfully modified. If either the VDD Monitor or the VDD Monitor reset source is not enabled, a Flash Error Device Reset will be generated when the firmware attempts to modify the Flash.

The following guidelines are recommended for any system that contains routines which write or erase Flash from code.

13.5.1. VDD Maintenance and the VDD Monitor

- 1. If the system power supply is subject to voltage or current "spikes," add sufficient transient protection devices to the power supply to ensure that the supply voltages listed in the Absolute Maximum Ratings table are not exceeded.
- 2. Make certain that the minimum VDD rise time specification of 1 ms is met. If the system cannot meet this rise time specification, then add an external VDD brownout circuit to the RST pin of the device that holds the device in reset until VDD reaches the minimum device operating voltage and re-asserts RST if VDD drops below the minimum device operating voltage.
- 3. Keep the on-chip VDD Monitor enabled and enable the VDD Monitor as a reset source as early in code as possible. This should be the first set of instructions executed after the Reset Vector. For C-based systems, this will involve modifying the startup code added by the C compiler. See your compiler documentation for more details. Make certain that there are no delays in software between enabling the VDD Monitor and enabling the VDD Monitor as a reset source. Code examples showing this can be found in "AN201: Writing to Flash from Firmware," available from the Silicon Laboratories website.

Note: On C8051F91x-C8051F90x devices, both the VDD Monitor and the VDD Monitor reset source must be enabled to write or erase Flash without generating a Flash Error Device Reset.

Note: On C8051F91x-C8051F90x devices, both the VDD Monitor and the VDD Monitor reset source are enabled by hardware after a power-on reset.

- 4. As an added precaution, explicitly enable the VDD Monitor and enable the VDD Monitor as a reset source inside the functions that write and erase Flash memory. The VDD Monitor enable instructions should be placed just after the instruction to set PSWE to a 1, but before the Flash write or erase operation instruction.
- Make certain that all writes to the RSTSRC (Reset Sources) register use direct assignment operators and explicitly DO NOT use the bit-wise operators (such as AND or OR). For example, "RSTSRC = 0x02" is correct, but "RSTSRC |= 0x02" is incorrect.
- 6. Make certain that all writes to the RSTSRC register explicitly set the PORSF bit to a 1. Areas to check are initialization code which enables other reset sources, such as the Missing Clock Detector or Comparator, for example, and instructions which force a Software Reset. A global search on "RSTSRC" can quickly verify this.



SFR Definition 14.1. PMU0CF: Power Management Unit Configuration^{1,2}

Bit	7	6	5	4	3	2	1	0
Name	SLEEP	SUSPEND	CLEAR	RSTWK	RTCFWK	RTCAWK	PMATWK	CPT0WK
Туре	W	W	W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	Varies	Varies	Varies	Varies	Varies

SFR Page = 0x0; SFR Address = 0xB5

Bit	Name	Description	Write	Read
7	SLEEP	Sleep Mode Select	Writing 1 places the device in Sleep Mode.	N/A
6	SUSPEND	Suspend Mode Select	Writing 1 places the device in Suspend Mode.	N/A
5	CLEAR	Wake-up Flag Clear	Writing 1 clears all wake- up flags.	N/A
4	RSTWK	Reset Pin Wake-up Flag	N/A	Set to 1 if a falling edge has been detected on RST.
3	RTCFWK	SmaRTClock Oscillator Fail Wake-up Source Enable and Flag	0: Disable wake-up on SmaRTClock Osc. Fail. 1: Enable wake-up on SmaRTClock Osc. Fail.	Set to 1 if the SmaRT- Clock Oscillator has failed.
2	RTCAWK	SmaRTClock Alarm Wake-up Source Enable and Flag	0: Disable wake-up on SmaRTClock Alarm. 1: Enable wake-up on SmaRTClock Alarm.	Set to 1 if a SmaRTClock Alarm has occurred.
1	PMATWK	Port Match Wake-up Source Enable and Flag	0: Disable wake-up on Port Match Event. 1: Enable wake-up on Port Match Event.	Set to 1 if a Port Match Event has occurred.
0	CPT0WK	Comparator0 Wake-up Source Enable and Flag	0: Disable wake-up on Comparator0 rising edge. 1: Enable wake-up on Comparator0 rising edge.	Set to 1 if Comparator0 rising edge has occurred.

Notes:

1. Read-modify-write operations (ORL, ANL, etc.) should not be used on this register. Wake-up sources must be re-enabled each time the SLEEP or SUSPEND bits are written to 1.

- 2. The Low Power Internal Oscillator cannot be disabled and the MCU cannot be placed in Suspend or Sleep Mode if any wake-up flags are set to 1. Software should clear all wake-up sources after each reset and after each wake-up from Suspend or Sleep Modes.
- 3. PMU0 requires two system clocks to update the wake-up source flags after waking from Suspend mode. The wake-up source flags will read '0' during the first two system clocks following the wake from Suspend mode.



16. On-Chip DC-DC Converter (DC0)

C8051F91x-C8051F90x devices include an on-chip dc-dc converter to allow operation from a single cell battery with a supply voltage as low as 0.9 V. The dc-dc converter is a switching boost converter with an input voltage range of 0.9 to 1.8 V (C8051F911/01) or 3.6 V (C8051F912/11) and a programmable output voltage range of 1.8 to 3.3 V. The default output voltage is 1.9 V when the input is less than 1.9 V. Since the dc-dc converter uses a boost architecture, the output voltage will always be greater than or equal to the input voltage. The dc-dc converter can supply the system with up to 65 mW of regulated power (or up to 100 mW in some applications) and can be used for powering other devices in the system. This allows the most flexibility when interfacing to sensors and other analog signals which typically require a higher supply voltage than a single-cell battery can provide.

Figure 16.1 shows a block diagram of the dc-dc converter. During normal operation in the first half of the switching cycle, the Duty Cycle Control switch is closed and the Diode Bypass switch is open. Since the output voltage is higher than the voltage at the DCEN pin, no current flows through the diode and the load is powered from the output capacitor. During this stage, the DCEN pin is connected to ground through the Duty Cycle Control switch, generating a positive voltage across the inductor and forcing its current to ramp up.

In the second half of the switching cycle, the Duty Cycle control switch is opened and the Diode Bypass switch is closed. This connects DCEN directly to VDD/DC+ and forces the inductor current to charge the output capacitor. Once the inductor transfers its stored energy to the output capacitor, the Duty Cycle Control switch is closed, the Diode Bypass switch is opened, and the cycle repeats.

The dc-dc converter has a built in voltage reference and oscillator, and will automatically limit or turn off the switching activity in case the peak inductor current rises beyond a safe limit or the output voltage rises above the programmed target value. This allows the dc-dc converter output to be safely overdriven by a secondary power source (when available) in order to preserve battery life. The dc-dc converter's settings can be modified using SFR registers which provide the ability to change the target output voltage, oscillator frequency or source, Diode Bypass switch resistance, peak inductor current, and minimum duty cycle.



Figure 16.1. DC-DC Converter Block Diagram



20.2.5. Automatic Gain Control (Crystal Mode Only) and SmaRTClock Bias Doubling

Automatic Gain Control allows the SmaRTClock oscillator to trim the oscillation amplitude of a crystal in order to achieve the lowest possible power consumption. Automatic Gain Control automatically detects when the oscillation amplitude has reached a point where it safe to reduce the drive current, therefore, it may be enabled during crystal startup. It is recommended to enable Automatic Gain Control in most systems which use the SmaRTClock oscillator in Crystal Mode. The following are recommended crystal specifications and operating conditions when Automatic Gain Control is enabled:

- ESR < 50 kΩ
- Load Capacitance < 10 pF
- Supply Voltage < 3.0 V
- Temperature > -20 °C

When using Automatic Gain Control, it is recommended to perform an oscillation robustness test to ensure that the chosen crystal will oscillate under the worst case condition to which the system will be exposed. The worst case condition that should result in the least robust oscillation is at the following system conditions: lowest temperature, highest supply voltage, highest ESR, highest load capacitance, and lowest bias current (AGC enabled, Bias Double Disabled).

To perform the oscillation robustness test, the SmaRTClock oscillator should be enabled and selected as the system clock source. Next, the SYSCLK signal should be routed to a port pin configured as a push-pull digital output. The positive duty cycle of the output clock can be used as an indicator of oscillation robustness. As shown in Figure 20.2, duty cycles less than 55% indicate a robust oscillation. As the duty cycle approaches 60%, oscillation becomes less reliable and the risk of clock failure increases. Increasing the bias current (by disabling AGC) will always improve oscillation robustness and will reduce the output clock's duty cycle. This test should be performed at the worst case system conditions, as results at very low temperatures or high supply voltage will vary from results taken at room temperature or low supply voltage.





As an alternative to performing the oscillation robustness test, Automatic Gain Control may be disabled at the cost of increased power consumption (approximately 200 nA). Disabling Automatic Gain Control will provide the crystal oscillator with higher immunity against external factors which may lead to clock failure. Automatic Gain Control must be disabled if using the SmaRTClock oscillator in self-oscillate mode.

Table 20.3 shows a summary of the oscillator bias settings. The SmaRTClock Bias Doubling feature allows the self-oscillation frequency to be increased (almost doubled) and allows a higher crystal drive strength in crystal mode. High crystal drive strength is recommended when the crystal is exposed to poor environmental conditions such as excessive moisture. SmaRTClock Bias Doubling is enabled by setting BIASX2 (RTC0XCN.5) to 1.





Figure 21.4. Crossbar Priority Decoder with Crystal Pins Skipped



24.2. SPI Master Mode Operation

A SPI master device initiates all data transfers on a SPI bus. SPIn is placed in master mode by setting the Master Enable flag (MSTENn, SPInCN.6). Writing a byte of data to the SPIn data register (SPInDAT) when in master mode writes to the transmit buffer. If the SPI shift register is empty, the byte in the transmit buffer is moved to the shift register, and a data transfer begins. The SPIn master immediately shifts out the data serially on the MOSI line while providing the serial clock on SCK. The SPIFn (SPInCN.7) flag is set to logic 1 at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set. While the SPIn master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers the contents of its shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPInDAT.

When configured as a master, SPIn can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSnMD1 (SPInCN.3) = 0 and NSSnMD0 (SPInCN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPIn when another master is accessing the bus. When NSS is pulled low in this mode, MSTENn (SPInCN.6) and SPIENn (SPInCN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODFn, SPInCN.5 = 1). Mode Fault will generate an interrupt if enabled. SPIn must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 24.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSnMD1 (SPInCN.3) = 0 and NSSnMD0 (SPInCN.2) = 0. In this mode, NSS is not used, and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 24.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSnMD1 (SPInCN.3) = 1. In this mode, NSS is configured as an output pin, and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSnMD0 (SPInCN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 24.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.



SFR Definition 25.2. TCON: Timer Control

Bit	7	6	5	4	3	2	1	0		
		TP1	TEO	TPO	I⊑1	- IT1	IEO	ITO		
Name	9 171		IFU	INU	1⊂1	111	IEU	110		
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Rese	t 0	0	0	0	0	0	0	0		
SFR F	age = 0x0; SI	FR Address = 0x88; Bit-Addressable								
Bit	Name				Function					
7	TF1	Timer 1 Ov	erflow Flag	•						
		Set to 1 by l but is autom routine.	nardware wh natically clea	nen Timer 1 red when th	overflows. Tl e CPU vecto	nis flag can t rs to the Tim	be cleared by her 1 interrup	y software ot service		
6	TR1	Timer 1 Ru	n Control.							
		Timer 1 is e	nabled by se	etting this bit	to 1.					
5	TF0	Timer 0 Ov	erflow Flag							
		Set to 1 by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.								
4	TR0	Timer 0 Ru	Timer 0 Run Control.							
		Timer 0 is enabled by setting this bit to 1.								
3	IE1	External In	terrupt 1.							
		This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode.								
2	IT1	Interrupt 1	Type Select							
		This bit selects whether the configured INT1 interrupt will be edge or level sensitive. INT1 is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 12.7). 0: INT1 is level triggered. 1: INT1 is edge triggered.								
1	IE0	External In	terrupt 0.							
		This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode.								
0	IT0	Interrupt 0	Type Select	t.						
		This bit sele INT0 is cont Definition 12 0: INT0 is le 1: INT0 is e	cts whether igured active 2.7). vel triggered dge triggere	the configur e low or high d. d.	ed INTO intention by the INOF	rrupt will be PL bit in regis	edge or leve ster IT01CF (l sensitive. (see SFR		



26.3. Capture/Compare Modules

Each module can be configured to operate independently in one of six operation modes: edge-triggered capture, software timer, high speed output, frequency output, 8 to 11-bit pulse width modulator, or 16-bit pulse width modulator. Each module has special function registers (SFRs) associated with it in the CIP-51 system controller. These registers are used to exchange data with a module and configure the module's mode of operation. Table 26.2 summarizes the bit settings in the PCA0CPMn and PCA0PWM registers used to select the PCA capture/compare module's operating mode. Note that all modules set to use 8, 9, 10, or 11-bit PWM mode must use the same cycle length (8-11 bits). Setting the ECCFn bit in a PCA0CPMn register enables the module's CCFn interrupt.

Operational Mode				PCA0CPMn							PCA0PWM			
Bit Number	7	6	5	4	3	2	1	0	7	6	5	4-2	1–0	
Capture triggered by positive edge on CEXn	Х	Х	1	0	0	0	0	Α	0	Х	В	XXX	XX	
Capture triggered by negative edge on CEXn	Х	Х	0	1	0	0	0	А	0	Х	В	XXX	XX	
Capture triggered by any transition on CEXn	Х	Х	1	1	0	0	0	А	0	Х	В	XXX	XX	
Software Timer	Х	С	0	0	1	0	0	А	0	Х	В	XXX	XX	
High-Speed Output	Х	С	0	0	1	1	0	А	0	Х	В	XXX	XX	
Frequency Output	Х	С	0	0	0	1	1	А	0	Х	В	XXX	XX	
8-Bit Pulse Width Modulator (Note 7)	0	С	0	0	Е	0	1	А	0	Х	В	XXX	00	
9-Bit Pulse Width Modulator (Note 7)	0	С	0	0	Е	0	1	А	D	Х	В	XXX	01	
10-Bit Pulse Width Modulator (Note 7)	0	С	0	0	Е	0	1	А	D	Х	В	XXX	10	
11-Bit Pulse Width Modulator (Note 7)	0	С	0	0	Е	0	1	А	D	Х	В	XXX	11	
16-Bit Pulse Width Modulator	1	С	0	0	Е	0	1	А	0	Х	В	XXX	XX	
 Notes: 1. X = Don't Care (no functional difference for individual module if 1 or 0). 2. A = Enable interrupts for this module (PCA interrupt triggered on CCFn set to 1). 3. B = Enable 8th 9th 10th or 11th bit overflow interrupt (Depends on setting of CLSEI [1:0]). 														

Table 26.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Modules

C = When set to 0, the digital comparator is off. For high speed and frequency output modes, the associated pin will not toggle. In any of the PWM modes, this generates a 0% duty cycle (output = 0).

5. D = Selects whether the Capture/Compare register (0) or the Auto-Reload register (1) for the associated channel is accessed via addresses PCA0CPHn and PCA0CPLn.

6. E = When set, a match event will cause the CCFn flag for the associated channel to be set.

7. All modules set to 8, 9, 10 or 11-bit PWM mode use the same cycle length setting.



26.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.



Figure 26.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.



SFR Definition 26.4. PCA0CPMn: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address, Page: PCA0CPM0 = 0xDA, 0x0; PCA0CPM1 = 0xDB, 0x0; PCA0CPM2 = 0xDC, 0x0 PCA0CPM3 = 0xDD, 0x0; PCA0CPM4 = 0xDE, 0x0; PCA0CPM5 = 0xCE, 0x0

Bit	Name	Function				
7	PWM16n	16-bit Pulse Width Modulation Enable.				
		This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected.				
		1: 16-bit PWM selected.				
6	ECOMn	Comparator Function Enable.				
		This bit enables the comparator function for PCA module n when set to 1.				
5	CAPPn	Capture Positive Function Enable.				
		This bit enables the positive edge capture for PCA module n when set to 1.				
4	CAPNn	Capture Negative Function Enable.				
		This bit enables the negative edge capture for PCA module n when set to 1.				
3	MATn	Match Function Enable.				
		This bit enables the match function for PCA module n when set to 1. When enabled,				
		bit in PCA0MD register to be set to logic 1.				
2	TOGn	Toggle Function Enable.				
		This bit enables the toggle function for PCA module n when set to 1. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic				
		ates in Frequency Output Mode.				
1	PWMn	Pulse Width Modulation Mode Enable.				
		This bit enables the PWM function for PCA module n when set to 1. When enabled, a				
		PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is				
		also set, the module operates in Frequency Output Mode.				
0	ECCFn	Capture/Compare Flag Interrupt Enable.				
		This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.				
		U: Disable CCFn interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCFn is set				
Nete	M/bon the M	DTE bit is set to 1, the DCACCDME register connect be medified, and medials 5 sets as the				
NOTE:	: When the WDTE bit is set to 1, the PCA0CPM5 register cannot be modified, and module 5 acts as the watchdog timer. To change the contents of the PCA0CPM5 register or the function of module 5, the Watchdog Timer must be disabled.					



SFR Definition 26.5. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xF9

Bit	Name	Function				
7:0	PCA0[7:0]	PCA Counter/Timer Low Byte.				
		The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.				
Note:	: When the WDTE bit is set to 1, the PCA0L register cannot be modified by software. To change the contents o the PCA0L register, the Watchdog Timer must first be disabled.					

SFR Definition 26.6. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xFA

Bit	Name	Function				
7:0	PCA0[15:8]	PCA Counter/Timer High Byte.				
		The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a "snapshot" register, whose contents are updated only when the contents of PCA0L are read (see Section 26.1).				
Note:	lote: When the WDTE bit is set to 1, the PCA0H register cannot be modified by software. To change the content the PCA0H register, the Watchdog Timer must first be disabled.					



27.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely "borrow" the C2CK (RST) and C2D pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 27.1.



Figure 27.1. Typical C2 Pin Sharing

The configuration in Figure 27.1 assumes the following:

- 1. The <u>user input</u> (b) cannot change state while the target device is halted.
- 2. The \overline{RST} pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.

