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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f901-gmr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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1. System Overview

C8051F91x-C8051F90x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- Single/Dual Battery operation with on-chip dc-dc boost converter.
- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- 10-bit 300 ksps or 12-bit 75 ksps single-ended ADC with analog multiplexer
- 6-Bit Programmable Current Reference. Resolution can be increased with PWM.
- Precision programmable 24.5 MHz internal oscillator with spread spectrum technology.
- 16 kB or 8 kB of on-chip Flash memory
- 768 bytes of on-chip RAM
- SMBus/I²C, Enhanced UART, and two Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- Two On-chip Voltage Comparators with 15 Capacitive Touch Sense inputs.
- 16 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F91x-C8051F90x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 0.9 to 1.8 V, 0.9 to 3.6 V or 1.8 to 3.6 V operation over the industrial temperature range (-40 to +85 °C). The Port I/O and RST pins are tolerant of input signals up to 5 V. The C8051F91x-C8051F90x devices are available in 24-pin QFN or QSOP packages. Both package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 through Figure 1.4.



1.1. CIP-51[™] Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F91x-C8051F90x family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51[™] instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

1.1.3. Additional Features

The C8051F91x-C8051F90x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51 allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below safe levels), a Watchdog Timer, a Missing Clock Detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz and is accurate to $\pm 2\%$ over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.



SFR Definition 12.4. EIP1: Extended Interrupt Priority 1

Bit	7	6	5	4	3	2	1	0
Name	PT3	PCP1	PCP0	PPCA0	PADC0	PWADC0	PRTC0A	PSMB0
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xF6

Bit	Name	Function
7	PT3	Timer 3 Interrupt Priority Control.This bit sets the priority of the Timer 3 interrupt.0: Timer 3 interrupts set to low priority level.1: Timer 3 interrupts set to high priority level.
6	PCP1	Comparator1 (CP1) Interrupt Priority Control. This bit sets the priority of the CP1 interrupt. 0: CP1 interrupt set to low priority level. 1: CP1 interrupt set to high priority level.
5	PCP0	 Comparator0 (CP0) Interrupt Priority Control. This bit sets the priority of the CP0 interrupt. 0: CP0 interrupt set to low priority level. 1: CP0 interrupt set to high priority level.
4	PPCA0	 Programmable Counter Array (PCA0) Interrupt Priority Control. This bit sets the priority of the PCA0 interrupt. 0: PCA0 interrupt set to low priority level. 1: PCA0 interrupt set to high priority level.
3	PADC0	 ADC0 Conversion Complete Interrupt Priority Control. This bit sets the priority of the ADC0 Conversion Complete interrupt. 0: ADC0 Conversion Complete interrupt set to low priority level. 1: ADC0 Conversion Complete interrupt set to high priority level.
2	PWADC0	 ADC0 Window Comparator Interrupt Priority Control. This bit sets the priority of the ADC0 Window interrupt. 0: ADC0 Window interrupt set to low priority level. 1: ADC0 Window interrupt set to high priority level.
1	PRTC0A	 SmaRTClock Alarm Interrupt Priority Control. This bit sets the priority of the SmaRTClock Alarm interrupt. 0: SmaRTClock Alarm interrupt set to low priority level. 1: SmaRTClock Alarm interrupt set to high priority level.
0	PSMB0	 SMBus (SMB0) Interrupt Priority Control. This bit sets the priority of the SMB0 interrupt. 0: SMB0 interrupt set to low priority level. 1: SMB0 interrupt set to high priority level.



SFR Definition 13.1. PSCTL: Program Store R/W Control

Bit	7	6	5	4	3	2	1	0
Name						SFLE	PSEE	PSWE
Туре	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page =0x0; SFR Address = 0x8F

Bit	Name	Function
7:3	Unused	Unused.
		Read = 00000b, Write = don't care.
2	SFLE	Scratchpad Flash Memory Access Enable.
		When this bit is set, Flash MOVC reads and MOVX writes from user software are directed to the Scratchpad Flash sector. Flash accesses outside the address range 0x0000-0x01FF should not be attempted and may yield undefined results when SFLE is set to 1.
		0: Flash access from user software directed to the Program/Data Flash sector.1: Flash access from user software directed to the Scratchpad Sector.
1	PSEE	Program Store Erase Enable.
		Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter. 0: Flash program memory erasure disabled. 1: Flash program memory erasure enabled.
0	PSWE	Program Store Write Enable.
		 Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data. 0: Writes to Flash program memory disabled. 1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.



SFR Definition 15.4. CRC0AUTO: CRC0 Automatic Control

Bit	7	6	5	4	3	2	1	0	
Name	AUTOEN	CRCDONE		CRC0ST[5:0]					
Туре	R/W							R/W	
Reset	0	1	0	0	0	0	0	0	

SFR Page = 0xF; SFR Address = 0x96

Bit	Name	Function
7	AUTOEN	Automatic CRC Calculation Enable.
		When AUTOEN is set to 1, any write to CRC0CN will initiate an automatic CRC starting at Flash sector CRC0ST and continuing for CRC0CNT sectors.
6	CRCDONE	CRCDONE Automatic CRC Calculation Complete.
		Set to 0 when a CRC calculation is in progress. Code execution is stopped during a CRC calculation; therefore, reads from firmware will always return 1.
5:0	CRC0ST[5:0]	Automatic CRC Calculation Starting Flash Sector.
		These bits specify the Flash sector to start the automatic CRC calculation. The starting address of the first Flash sector included in the automatic CRC calculation is CRC0ST x Page Size. Note: 'F91x and 'F90x devices have a page size of 512 bytes.



SFR Definition 16.2. DC0CF: DC-DC Converter Configuration

Bit	7	6	5	4	3	2	1	0
Name	LPEN	CLKDIV[1:0]		AD0CKINV	CLKINV	ILIMIT	VDDSLP	CLKSEL
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x96

Bit	Name	Function
7	LPEN	Low Power Mode Enable.
		Enables the dc-dc low power mode which reduces bias currents, reduces peak inductor current, and increases efficiency for low load currents. Only available on 'F912 and 'F902 devices.
		0: Low Power Mode Disabled. 1: Low Power Mode Enabled.
6:5	CLKDIV[1:0]	DC-DC Clock Divider.
		Divides the dc-dc converter clock when the system clock is selected as the clock source for dc-dc converter. These bits are ignored when the dc-dc converter is clocked from its local oscillator.
		00: The dc-dc converter clock is system clock divided by 1.
		01: The dc-dc converter clock is system clock divided by 2.
		10: The dc-dc converter clock is system clock divided by 4.
Δ		ADC0 Clock Inversion (Clock Invert During Sync)
-	ADUCKINV	Inverte the ADCO SAR clock derived from the de-de converter clock when the SVNC
		bit (DC0CN.3) is enabled. This bit is ignored when the SYNC bit is set to zero.
		0: ADC0 SAR clock is inverted.
		1: ADC0 SAR clock is not inverted.
3	CLKINV	DC-DC Converter Clock Invert.
		Inverts the system clock used as the input to the dc-dc clock divider.
		0: The dc-dc converter clock is not inverted.
		1: The dc-dc converter clock is inverted.
2	ILIMIT	Peak Current Limit Threshold.
		Sets the threshold for the maximum allowed peak inductor current according to Table 16.1.
1	VDDSLP	VDD-DC+ Sleep Mode Connection.
		Specifies the power source for VDD/DC+ in Sleep Mode when the dc-dc converter is enabled.
		1: VDD-DC+ is floating in Sleep Mode.
0	CLKSEL	DC-DC Converter Clock Source Select.
		Specifies the dc-dc converter clock source.
		0: The dc-dc converter is clocked from its local oscillator.
		1: The dc-dc converter is clocked from the system clock.



18.3. External Reset

The external RST pin provides a means for external circuitry to force the device into a reset state. Asserting an active-low signal on the RST pin generates a reset; an external pullup and/or decoupling of the RST pin may be necessary to avoid erroneous noise-induced resets. See Table 4.4 for complete RST pin specifications. The external reset remains functional even when the device is in the low power suspend and sleep modes. The PINRSF flag (RSTSRC.0) is set on exit from an external reset.

18.4. Missing Clock Detector Reset

The Missing Clock Detector (MCD) is a one-shot circuit that is triggered by the system clock. If the system clock remains high or low for more than 100 μ s, the one-shot will time out and generate a reset. After a MCD reset, the MCDRSF flag (RSTSRC.2) will read 1, signifying the MCD as the reset source; otherwise, this bit reads 0. Writing a 1 to the MCDRSF bit enables the Missing Clock Detector; writing a 0 disables it. The missing clock detector reset is automatically disabled when the device is in the low power suspend or sleep mode. Upon exit from either low power state, the enabled/disabled state of this reset source is restored to its previous value. The state of the RST pin is unaffected by this reset.

18.5. Comparator0 Reset

Comparator0 can be configured as a reset source by writing a 1 to the CORSEF flag (RSTSRC.5). Comparator0 should be enabled and allowed to settle prior to writing to CORSEF to prevent any turn-on chatter on the output from generating an unwanted reset. The Comparator0 reset is active-low: if the non-inverting input voltage (on CP0+) is less than the inverting input voltage (on CP0–), the device is put into the reset state. After a Comparator0 reset, the CORSEF flag (RSTSRC.5) will read 1 signifying Comparator0 as the reset source; otherwise, this bit reads 0. The Comparator0 reset source remains functional even when the device is in the low power <u>suspend</u> and sleep states as long as Comparator0 is also enabled as a wake-up source. The state of the RST pin is unaffected by this reset.

18.6. PCA Watchdog Timer Reset

The programmable Watchdog Timer (WDT) function of the Programmable Counter Array (PCA) can be used to prevent software from running out of control during a system malfunction. The PCA WDT function can be enabled or disabled by software as described in Section "26.4. Watchdog Timer Mode" on page 304; the WDT is enabled and clocked by SYSCLK / 12 following any reset. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit (RSTSRC.5) is set to 1. The PCA Watchdog Timer reset source is automatically disabled when the device is in the low power suspend or sleep mode. Upon exit from either low power state, the enabled/disabled state of this reset source is restored to its previous value. The state of the RST pin is unaffected by this reset.





Figure 21.4. Crossbar Priority Decoder with Crystal Pins Skipped



SFR Definition 21.15. P1MDIN: Port1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name			P1MDIN[6:0]					
Туре			R/W					
Reset	1	1	1	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0xF2

Bit	Name	Function
7	Unused	Unused.
		Read =0b; Write = Don't Care.
6:0	P1MDIN[6:0]	Analog Configuration Bits for P1.6–P1.0 (respectively).
		Port pins configured for analog mode have their weak pullup and digital receiver disabled. The digital driver is not explicitly disabled. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.

SFR Definition 21.16. P1MDOUT: Port1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name				Р	1MDOUT[6:	0]		
Туре			R/W					
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xA5

Bit	Name	Function
7	Unused	Unused.
		Read =0b; Write = Don't Care.
6:0	P1MDOUT[6:0]	Output Configuration Bits for P1.6–P1.0 (respectively).
		These bits control the digital driver even when the corresponding bit in register P1MDIN is logic 0.0: Corresponding P1.n Output is open-drain.1: Corresponding P1.n Output is push-pull.



22. SMBus

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus. Reads and writes to the interface by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus interface may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The SMBus peripheral can be fully driven by software (i.e. software accepts/rejects slave addresses, and generates ACKs), or hardware slave address recognition and automatic ACK generation can be enabled to minimize software overhead. A block diagram of the SMBus peripheral and the associated SFRs is shown in Figure 22.1.



Figure 22.1. SMBus Block Diagram



23.1. Enhanced Baud Rate Generation

The UART0 baud rate is generated by Timer 1 in 8-bit auto-reload mode. The TX clock is generated by TL1; the RX clock is generated by a copy of TL1 (shown as RX Timer in Figure 23.2), which is not useraccessible. Both TX and RX Timer overflows are divided by two to generate the TX and RX baud rates. The RX Timer runs when Timer 1 is enabled, and uses the same reload value (TH1). However, an RX Timer reload is forced when a START condition is detected on the RX pin. This allows a receive to begin any time a START is detected, independent of the TX Timer state.



Figure 23.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload (see Section "25.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload" on page 274). The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK / 4, SYSCLK / 12, SYSCLK / 48, the external oscillator clock / 8, or an external input T1. For any given Timer 1 clock source, the UART0 baud rate is determined by Equation 23.1-A and Equation 23.1-B.

A) UartBaudRate =
$$\frac{1}{2} \times T1_Overflow_Rate$$

B) T1_Overflow_Rate = $\frac{T1_{CLK}}{256 - TH1}$

Equation 23.1. UART0 Baud Rate

Where $T1_{CLK}$ is the frequency of the clock supplied to Timer 1, and T1H is the high byte of Timer 1 (reload value). Timer 1 clock frequency is selected as described in Section "25.1. Timer 0 and Timer 1" on page 272. A quick reference for typical baud rates and system clock frequencies is given in Table 23.1 through Table 23.2. Note that the internal oscillator may still generate the system clock when the external oscillator is driving Timer 1.



SFR Definition 23.1. SCON0: Serial Port 0 Control

Bit	7	6	5	4	3	2	1	0
Name	SOMODE		MCE0	REN0	TB80	RB80	TI0	RI0
Туре	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x98; Bit-Addressable

Bit	Name	Function
7	SOMODE	Serial Port 0 Operation Mode. Selects the UART0 Operation Mode. 0: 8-bit UART with Variable Baud Rate. 1: 9-bit UART with Variable Baud Rate.
6	Unused	Unused. Read = 1b. Write = Don't Care.
5	MCE0	 Multiprocessor Communication Enable. For Mode 0 (8-bit UART): Checks for valid stop bit. 0: Logic level of stop bit is ignored. 1: RI0 will only be activated if stop bit is logic level 1. For Mode 1 (9-bit UART): Multiprocessor Communications Enable. 0: Logic level of ninth bit is ignored. 1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1.
4	REN0	Receive Enable. 0: UART0 reception disabled. 1: UART0 reception enabled.
3	TB80	Ninth Transmission Bit. The logic level of this bit will be sent as the ninth transmission bit in 9-bit UART Mode (Mode 1). Unused in 8-bit mode (Mode 0).
2	RB80	Ninth Receive Bit. RB80 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.
1	TIO	Transmit Interrupt Flag. Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.
0	RIO	Receive Interrupt Flag. Set to 1 by hardware when a byte of data has been received by UART0 (set at the STOP bit sampling time). When the UART0 interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.



25.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section "12.5. Interrupt Register Descriptions" on page 123); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section "12.5. Interrupt Register (Section "12.5. Interrupt Register (Section "12.5. Interrupt Register Descriptions" on page 123); Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

25.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section "21.3. Priority Crossbar Decoder" on page 209 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit (CKCON.3). When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 25.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 12.7). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section "12.5. Interrupt Register Descriptions" on page 123), facilitating pulse width measurements

TR0	GATE0	ΙΝΤΟ	Counter/Timer			
0	Х	Х	Disabled			
1	0	Х	Enabled			
1	1	0	Disabled			
1	1	1	Enabled			
Note: X = Don't Care						

Table 25.1. Timer 0 Running Modes

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT1 is used with Timer 1; the INT1 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 12.7).



25.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or when the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see Section "12.6. External Interrupts INT0 and INT1" on page 130 for details on the external input signals INT0 and INT1).



Figure 25.2. T0 Mode 2 Block Diagram



SFR Definition 25.11. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCC

Bit	Name	Function
7:0	TMR2L[7:0]	Timer 2 Low Byte.
		In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8- bit mode, TMR2L contains the 8-bit low byte timer value.

SFR Definition 25.12. TMR2H Timer 2 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xCD

Bit	Name	Function
7:0	TMR2H[7:0]	Timer 2 Low Byte.
		In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8- bit mode, TMR2H contains the 8-bit high byte timer value.



26.5. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of the PCA.

SFR Definition 26.1. PCA0CN: PCA Control

Bit	7	6	5	4	3	2	1	0
Name	CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD8; Bit-Addressable

Bit	Name	Function			
7	CF	PCA Counter/Timer Overflow Flag.			
		Set by hardware when the PCA Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.			
6	CR	PCA Counter/Timer Run Control.			
		This bit enables/disables the PCA Counter/Timer.			
		0: PCA Counter/Timer disabled.			
		1: PCA Counter/Timer enabled.			
5:0	CCF[5:0]	PCA Module n Capture/Compare Flag.			
		These bits are set by hardware when a match or capture occurs in the associated PCA Module n. When the CCFn interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.			



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