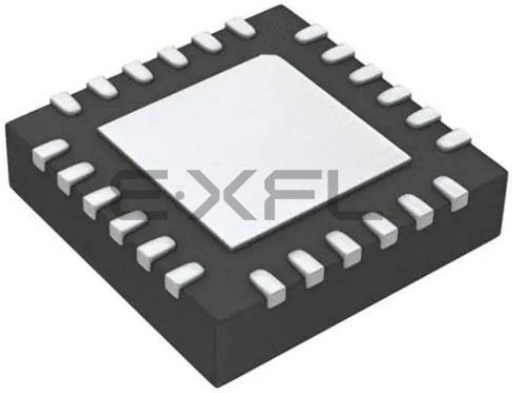

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f902-gmr

Table 4.13. IREF0 Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Static Performance					
Resolution[1]			6		bits
Output Compliance Range	Low Power Mode, Source High Current Mode, Source Low Power Mode, Sink High Current Mode, Sink	0 0 0.3 0.8	— — — —	V_{DD} – 0.4 V_{DD} – 0.8 V_{DD} V_{DD}	V
Integral Nonlinearity		—	<±0.2	±1.0	LSB
Differential Nonlinearity		—	<±0.2	±1.0	LSB
Offset Error		—	<±0.1	±0.5	LSB
Full Scale Error[2]	Low Power Mode, Source	—	—	±5	%
	High Current Mode, Source	—	—	±6	%
	Low Power Mode, Sink	—	—	±8	%
	High Current Mode, Sink	—	—	±8	%
Absolute Current Error	Low Power Mode Sourcing 20 µA	—	<±1	±3	%
Dynamic Performance					
Output Settling Time to 1/2 LSB		—	300	—	ns
Startup Time		—	1	—	µs
Power Consumption					
Net Power Supply Current (V_{DD} supplied to IREF0 minus any output source current)	Low Power Mode, Source				
	IREF0DAT = 000001	—	10	—	µA
	IREF0DAT = 111111	—	10	—	µA
	High Current Mode, Source				
	IREF0DAT = 000001	—	10	—	µA
	IREF0DAT = 111111	—	10	—	µA
	Low Power Mode, Sink				
	IREF0DAT = 000001	—	1	—	µA
	IREF0DAT = 111111	—	11	—	µA
	High Current Mode, Sink				
	IREF0DAT = 000001	—	12	—	µA
	IREF0DAT = 111111	—	81	—	µA

Notes:
1. Refer to “PWM Enhanced Mode” on page 86 for information on how to improve IREF0 resolution.
2. Full scale is 63 µA in Low Power Mode and 504 µA in High Power Mode.

SFR Definition 5.6. ADC0H: ADC0 Data Word High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0[15:8]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xBE

Bit	Name	Description	Read	Write
7:0	ADC0[15:8]	**ADC0 Data Word High Byte.**	Most Significant Byte of the 16-bit ADC0 Accumulator formatted according to the settings in AD0SJST[2:0].	Set the most significant byte of the 16-bit ADC0 Accumulator to the value written.
Note: If Accumulator shifting is enabled, the most significant bits of the value read will be zeros. This register should not be written when the SYNC bit is set to 1.				

SFR Definition 5.7. ADC0L: ADC0 Data Word Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xBD;

Bit	Name	Description	Read	Write
7:0	ADC0[7:0]	**ADC0 Data Word Low Byte.**	Least Significant Byte of the 16-bit ADC0 Accumulator formatted according to the settings in AD0SJST[2:0].	Set the least significant byte of the 16-bit ADC0 Accumulator to the value written.
Note: If Accumulator shifting is enabled, the most significant bits of the value read will be the least significant bits of the accumulator high byte. This register should not be written when the SYNC bit is set to 1.				

5.9. Voltage and Ground Reference Options

The voltage reference MUX is configurable to use an externally connected voltage reference, one of two internal voltage references, or one of two power supply voltages (see Figure 5.10). The ground reference MUX allows the ground reference for ADC0 to be selected between the ground pin (GND) or a port pin dedicated to analog ground (P0.1/AGND).

The voltage and ground reference options are configured using the REF0CN SFR described on page 85. Electrical specifications are can be found in the Electrical Specifications Chapter.

Important Note About the V_{REF} and AGND Inputs: Port pins are used as the external V_{REF} and AGND inputs. When using an external voltage reference or the internal precision reference, P0.0/VREF should be configured as an analog input and skipped by the Digital Crossbar. When using AGND as the ground reference to ADC0, P0.1/AGND should be configured as an analog input and skipped by the Digital Crossbar. Refer to Section “21. Port Input/Output” on page 205 for complete Port I/O configuration details. The external reference voltage must be within the range $0 \le V_{REF} \le$ VDD/DC+ and the external ground reference must be at the same DC voltage potential as GND.

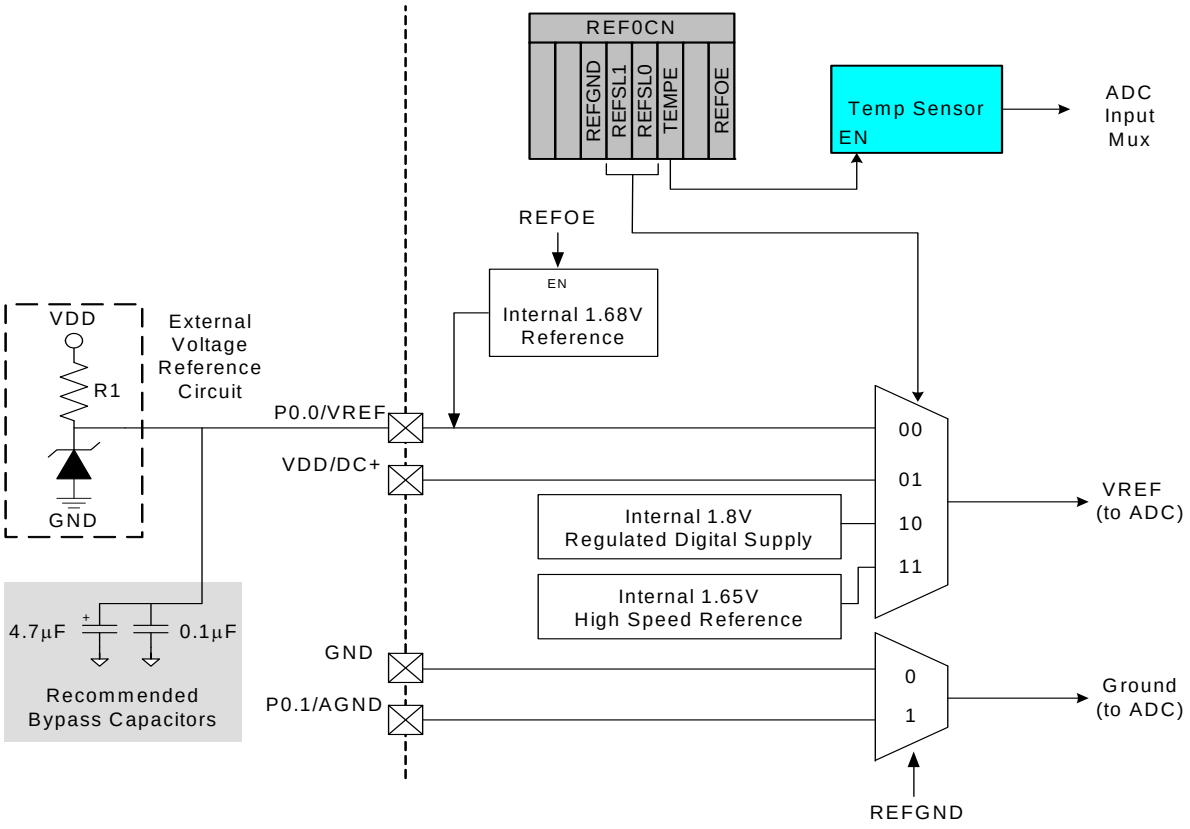

Figure 5.10. Voltage Reference Functional Block Diagram

SFR Definition 5.15. REF0CN: Voltage Reference Control

Bit	7	6	5	4	3	2	1	0
Name			REFGND	REFSL		TEMPE		REFOE
Type	R	R	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	1	1	0	0	0

SFR Page = 0x0; SFR Address = 0xD1

Bit	Name	Function
7:6	Unused	**Unused.** Read = 00b; Write = Don't Care.
5	REFGND	**Analog Ground Reference.** Selects the ADC0 ground reference. 0: The ADC0 ground reference is the GND pin. 1: The ADC0 ground reference is the P0.1/AGND pin.
4:3	REFSL	**Voltage Reference Select.** Selects the ADC0 voltage reference. 00: The ADC0 voltage reference is the P0.0/VREF pin. 01: The ADC0 voltage reference is the VDD/DC+ pin. 10: The ADC0 voltage reference is the internal 1.8 V digital supply voltage. 11: The ADC0 voltage reference is the internal 1.65 V high speed voltage reference.
2	TEMPE	**Temperature Sensor Enable.** Enables/Disables the internal temperature sensor. 0: Temperature Sensor Disabled. 1: Temperature Sensor Enabled.
1	Unused	**Unused.** Read = 0b; Write = Don't Care.
0	REFOE	**Internal Voltage Reference Output Enable.** Connects/Disconnects the internal voltage reference to the P0.0/VREF pin. 0: Internal 1.68 V Precision Voltage Reference disabled and not connected to P0.0/VREF. 1: Internal 1.68 V Precision Voltage Reference enabled and connected to P0.0/VREF.

5.14. Voltage Reference Electrical Specifications

See Table 4.12 on page 56 for detailed Voltage Reference Electrical Specifications.

7.2. Comparator Outputs

When a comparator is enabled, its output is a logic 1 if the voltage at the positive input is higher than the voltage at the negative input. When disabled, the comparator output is a logic 0. The comparator output is synchronized with the system clock as shown in Figure 7.2. The synchronous “latched” output (CP0, CP1) can be polled in software (CPnOUT bit), used as an interrupt source, or routed to a Port pin (configured for digital I/O) through the Crossbar.

The asynchronous “raw” comparator output (CP0A, CP1A) is used by the low power mode wake-up logic and reset decision logic. See the Power Options chapter and the Reset Sources chapter for more details on how the asynchronous comparator outputs are used to make wake-up and reset decisions. The asynchronous comparator output can also be routed directly to a Port pin through the Crossbar, and is available for use outside the device even if the system clock is stopped.

When using a Comparator as an interrupt source, Comparator interrupts can be generated on rising-edge and/or falling-edge comparator output transitions. Two independent interrupt flags (CPnRIF and CPnFIF) allow software to determine which edge caused the Comparator interrupt. The comparator rising-edge and falling-edge interrupt flags are set by hardware when a corresponding edge is detected regardless of the interrupt enable state. Once set, these bits remain set until cleared by software.

The rising-edge and falling-edge interrupts can be individually enabled using the CPnRIE and CPnFIE interrupt enable bits in the CPTnMD register. In order for the CPnRIF and/or CPnFIF interrupt flags to generate an interrupt request to the CPU, the Comparator must be enabled as an interrupt source and global interrupts must be enabled. See the Interrupt Handler chapter for additional information.

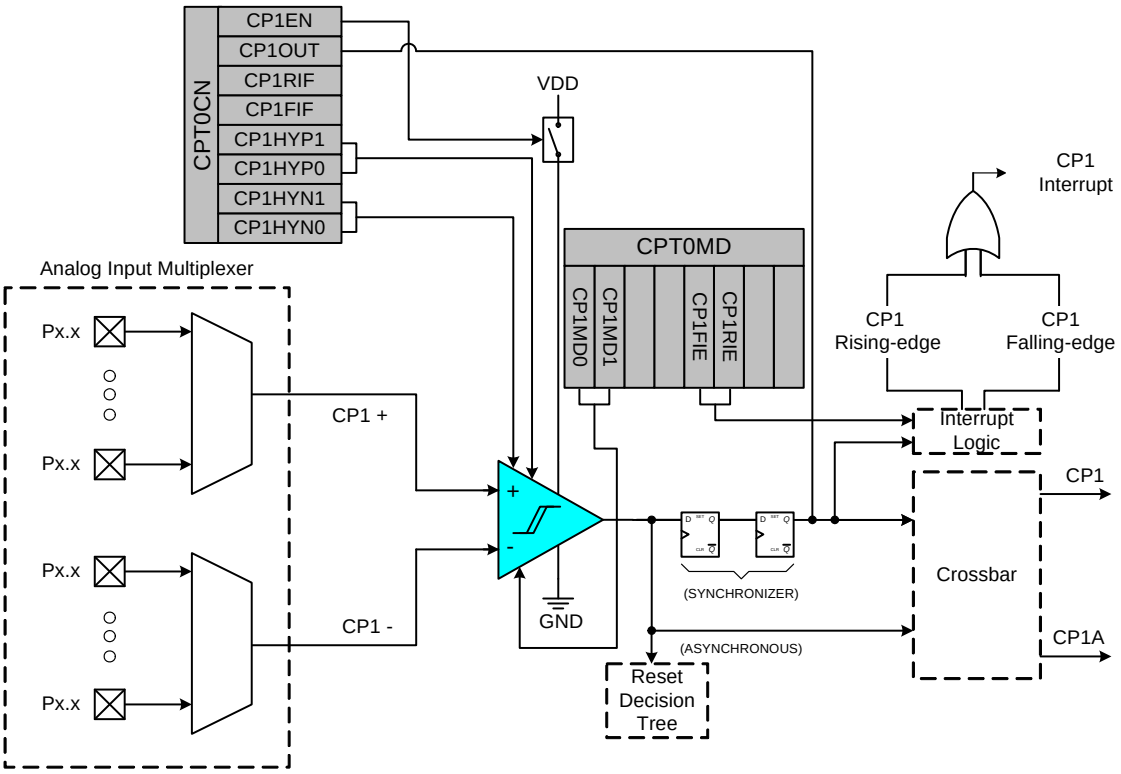

Figure 7.2. Comparator 1 Functional Block Diagram

whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 9.1 illustrates the data memory organization of the C8051F91x-C8051F90x.

9.2.1.1. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 8.6). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

9.2.1.2. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV    C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

Table 11.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved. SFRs highlighted in **blue** are only available on ‘F912 and ‘F902 devices.

Register	Address	SFR Page	Description	Page
CPT1MD	0x9C	0x0	Comparator1 Mode Selection	94
CPT1MX	0x9E	0x0	Comparator1 Mux Selection	97
CRC0AUTO	0x96	0xF	CRC0 Automatic Control	157
CRC0CN	0x92	0xF	CRC0 Control	155
CRC0CNT	0x97	0xF	CRC0 Automatic Flash Sector Count	158
CRC0DAT	0x91	0xF	CRC0 Data	156
CRC0FLIP	0x95	0xF	CRC0 Flip	159
CRC0IN	0x93	0xF	CRC0 Input	156
DC0CF	0x96	0x0	DC0 (DC-DC Converter) Configuration	168
DC0CN	0x97	0x0	DC0 (DC-DC Converter) Control	167
DC0MD	0x94	0xF	**DC0 (DC-DC Converter) Mode**	169
DPH	0x83	All	Data Pointer High	104
DPL	0x82	All	Data Pointer Low	104
EIE1	0xE6	All	Extended Interrupt Enable 1	126
EIE2	0xE7	All	Extended Interrupt Enable 2	128
EIP1	0xF6	0x0	Extended Interrupt Priority 1	127
EIP2	0xF7	0x0	Extended Interrupt Priority 2	129
EMI0CN	0xAA	0x0	EMIF Control	112
FLKEY	0xB7	0x0	Flash Lock And Key	141
FLSCL	0xB6	0x0	Flash Scale	141
IE	0xA8	All	Interrupt Enable	124
IP	0xB8	0x0	Interrupt Priority	125
IREF0CN	0xB9	0x0	Current Reference IREF Control	86
IREF0CF	0xB9	0xF	**Current Reference IREF Configuration**	87
IT01CF	0xE4	0x0	$\overline{\text{INT0}}$/$\overline{\text{INT1}}$ Configuration	131
OSCICL	0xB3	0x0	Internal Oscillator Calibration	186
OSCICN	0xB2	0x0	Internal Oscillator Control	186
OSCXCN	0xB1	0x0	External Oscillator Control	187
P0	0x80	All	Port 0 Latch	218
P0DRV	0xA4	0xF	Port 0 Drive Strength	220
P0MASK	0xC7	0x0	Port 0 Mask	215
P0MAT	0xD7	0x0	Port 0 Match	215
P0MDIN	0xF1	0x0	Port 0 Input Mode Configuration	219

SFR Definition 12.4. EIP1: Extended Interrupt Priority 1

Bit	7	6	5	4	3	2	1	0
Name	PT3	PCP1	PCP0	PPCA0	PADC0	PWADC0	PRTC0A	PSMB0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xF6

Bit	Name	Function
7	PT3	**Timer 3 Interrupt Priority Control.** This bit sets the priority of the Timer 3 interrupt. 0: Timer 3 interrupts set to low priority level. 1: Timer 3 interrupts set to high priority level.
6	PCP1	**Comparator1 (CP1) Interrupt Priority Control.** This bit sets the priority of the CP1 interrupt. 0: CP1 interrupt set to low priority level. 1: CP1 interrupt set to high priority level.
5	PCP0	**Comparator0 (CP0) Interrupt Priority Control.** This bit sets the priority of the CP0 interrupt. 0: CP0 interrupt set to low priority level. 1: CP0 interrupt set to high priority level.
4	PPCA0	**Programmable Counter Array (PCA0) Interrupt Priority Control.** This bit sets the priority of the PCA0 interrupt. 0: PCA0 interrupt set to low priority level. 1: PCA0 interrupt set to high priority level.
3	PADC0	**ADC0 Conversion Complete Interrupt Priority Control.** This bit sets the priority of the ADC0 Conversion Complete interrupt. 0: ADC0 Conversion Complete interrupt set to low priority level. 1: ADC0 Conversion Complete interrupt set to high priority level.
2	PWADC0	**ADC0 Window Comparator Interrupt Priority Control.** This bit sets the priority of the ADC0 Window interrupt. 0: ADC0 Window interrupt set to low priority level. 1: ADC0 Window interrupt set to high priority level.
1	PRTC0A	**SmaRTClock Alarm Interrupt Priority Control.** This bit sets the priority of the SmaRTClock Alarm interrupt. 0: SmaRTClock Alarm interrupt set to low priority level. 1: SmaRTClock Alarm interrupt set to high priority level.
0	PSMB0	**SMBus (SMB0) Interrupt Priority Control.** This bit sets the priority of the SMB0 interrupt. 0: SMB0 interrupt set to low priority level. 1: SMB0 interrupt set to high priority level.

14.2. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Note: To ensure the MCU enters a low power state upon entry into Idle Mode, the one-shot circuit should be enabled by clearing the BYPASS bit (FLSCL.6).

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to Section “18.6. PCA Watchdog Timer Reset” on page 176 for more information on the use and configuration of the WDT.

14.3. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter stop mode as soon as the instruction that sets the bit completes execution. In stop mode the precision internal oscillator and CPU are stopped; the state of the low power oscillator and the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering stop mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout.

Stop mode is a legacy 8051 power mode; it will not result in optimal power savings. Sleep or suspend mode will provide more power savings if the MCU needs to be inactive for a long period of time.

Note: To ensure the MCU enters a low power state upon entry into Stop Mode, the one-shot circuit should be enabled by clearing the BYPASS bit (FLSCL.6).

14.4. Suspend Mode

Setting the Suspend Mode Select bit (PMU0CF.6) causes the system clock to be gated off and all internal oscillators disabled. The system clock source must be set to the low power internal oscillator or the precision oscillator prior to entering suspend mode. All digital logic (timers, communication peripherals, interrupts, CPU, etc.) stops functioning until one of the enabled wake-up sources occurs.

The following wake-up sources can be configured to wake the device from suspend mode:

- SmaRTClock Oscillator Fail
- SmaRTClock Alarm
- Port Match Event
- Comparator0 Rising Edge

Note: Upon wake-up from suspend mode, PMU0 requires two system clocks in order to update the PMU0CF wake-up flags. All flags will read back a value of '0' during the first two system clocks following a wake-up from suspend mode.

In addition, a noise glitch on $\overline{\text{RST}}$ that is not long enough to reset the device will cause the device to exit suspend. In order for the MCU to respond to the pin reset event, software must not place the device back into suspend mode for a period of 15 µs. The PMU0CF register may be checked to determine if the wake-up was due to a falling edge on the /RST pin. If the wake-up source is not due to a falling edge on $\overline{\text{RST}}$, there is no time restriction on how soon software may place the device back into suspend mode. A 4.7 kW pullup resistor to VDD/DC+ is recommend for RST to prevent noise glitches from waking the device.

14.5. Sleep Mode

Setting the Sleep Mode Select bit (PMU0CF.6) turns off the internal 1.8 V regulator (VREG0) and switches the power supply of all on-chip RAM to the VBAT pin (see Figure 14.1). Power to most digital logic on the chip is disconnected; only PMU0 and the SmaRTClock remain powered. Analog peripherals remain powered in two-cell mode and lose their supply in one-cell mode because the dc-dc converter is disabled. In two-cell mode, only the Comparators remain functional when the device enters sleep mode. All other analog peripherals (ADC0, IREF0, External Oscillator, etc.) should be disabled prior to entering sleep mode. The system clock source must be set to the low power internal oscillator or the precision oscillator prior to entering sleep mode.

Note: When exiting sleep mode, 4 NOP instructions should be located immediately after the write to PMU0CF that placed the device in sleep mode.

Note: If the average active time (between successive entries into Sleep Mode) is less than 1 ms, peripherals that may cause a wake-up from Sleep Mode (SmaRTClock, Port Match, and Comparator0) or are enabled or configured in a way which may cause the wake-up flag to be set should be selected as wake-up sources. If these peripherals are not selected as wake-up sources, then it is recommended to bypass the Flash one-shot (FLSCL.6=1) before entering into Sleep Mode.

GPIO pins configured as digital outputs will retain their output state during sleep mode. In two-cell mode, they will maintain the same current drive capability in sleep mode as they have in normal mode. In one-cell mode, the VDD/DC+ supply will drop to the level of VBAT, which will reduce the output high-voltage level and the source and sink current drive capability.

GPIO pins configured as digital inputs can be used during sleep mode as wakeup sources using the port match feature. In two-cell mode, they will maintain the same input level specs in sleep mode as they have in normal mode. In one-cell mode, the VDD supply will drop to the level of VBAT, which will lower the switching threshold and increase the propagation delay.

C8051F912 and C8051F902 devices support a wakeup request for external devices. Upon exit from sleep mode, the wake-up request signal is driven high, allowing other devices in the system to wake up from their low power modes. An example of a system that may benefit from this function is one that uses a high-power dc-dc converter (>65 mW of output power). The dc-dc converter may be disabled when the system is asleep, and can be awoken by the wake-up request signal from the MCU. The wakeup request signal is high when the MCU is awake and low when the MCU is asleep.

SFR Definition 14.2. PMU0MD: Power Management Unit Mode

Bit	7	6	5	4	3	2	1	0
Name	RTCOE	WAKEOE	MONDIS					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xB5

Bit	Name	Function
7	RTCOE	**Buffered SmaRTClock Output Enable.** Enables the buffered SmaRTClock oscillator output on P0.2. Only available on ‘F912 and ‘F902 devices. 0: Buffered SmaRTClock output is not enabled. 1: Buffered SmaRTClock output is enabled.
6	WAKEOE	**Wakeup Request Output Enable.** Enables the Sleep Mode wake-up request signal on P0.3. Only available on ‘F912 and ‘F902 devices. 0: Wake-up request signal is not enabled. 1: Wake-up request signal is enabled.
5	MONDIS	**VBAT Supply Monitor Disable.** Writing a 1 to this bit disables the VBAT supply monitor. Writing a 0 to this bit when the VBAT supply monitor is disabled will trigger a power-on reset. Only available on ‘F912 and ‘F902 devices.
4:0	Unused	**Unused.** Read = 00000b. Write = Don’t Care.

16.4. Enabling the DC-DC Converter

On power-on reset, the state of the DCEN pin is sampled to determine if the device will power up in one-cell or two-cell mode. In two-cell mode, the dc-dc converter always remains disabled. In one-cell mode, the dc-dc converter remains disabled in Sleep Mode, and enabled in all other power modes. See Section “14. Power Management” on page 143 for complete details on available power modes.

The dc-dc converter is enabled (one-cell mode) in hardware by placing a 0.68 µH inductor between DCEN and VBAT. The dc-dc converter is disabled (two-cell mode) by shorting DCEN directly to GND. The DCEN pin should never be left floating. The device can only switch between one-cell and two-cell mode during a power-on reset. See Section “18. Reset Sources” on page 171 for more information regarding reset behavior.

Figure 16.2 shows the two dc-dc converter configuration options.

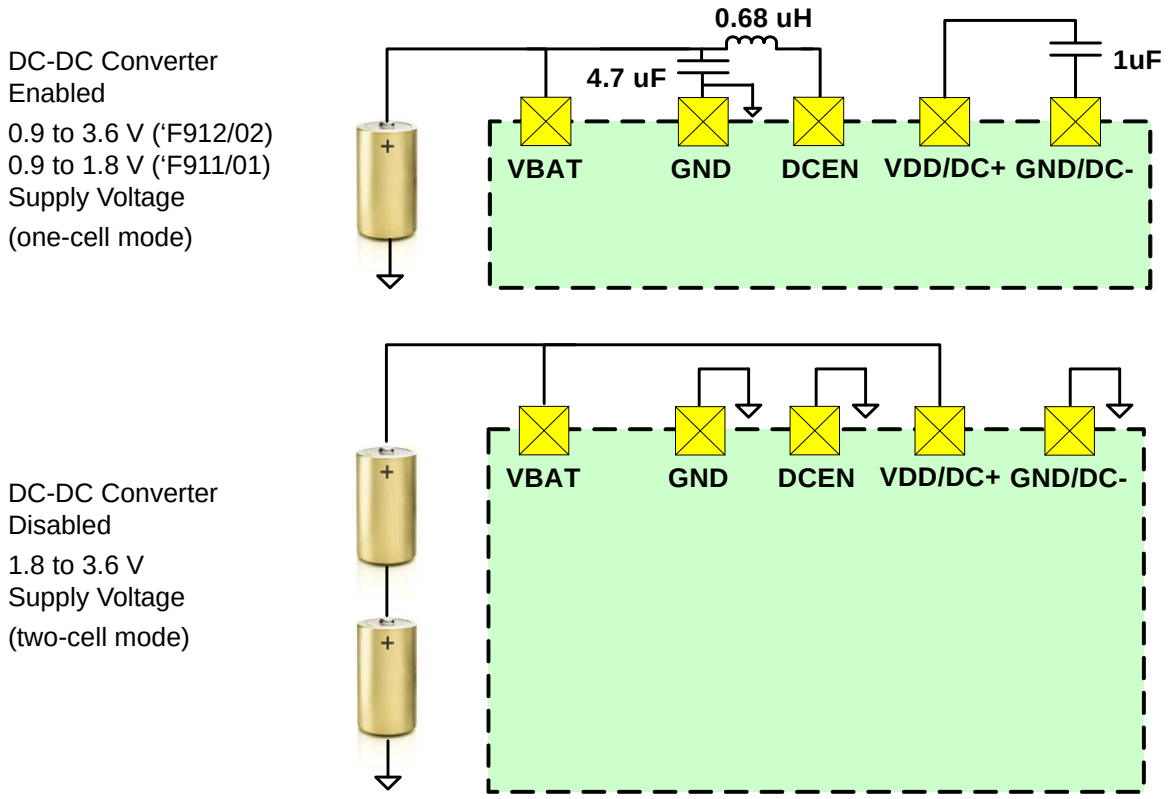

Figure 16.2. DC-DC Converter Configuration Options

When the dc-dc converter “Enabled” configuration (one-cell mode) is chosen, the following guidelines apply:

- In most cases, the GND/DC– pin should not be externally connected to GND.
- The 0.68 µH inductor should be placed as close as possible to the DCEN pin for maximum efficiency.
- The 4.7 µF capacitor should be placed as close as possible to the inductor.
- The current loop including GND, the 4.7 µF capacitor, the 0.68 µH inductor and the DCEN pin should be made as short as possible.
- The PCB traces connecting VDD/DC+ to the output capacitor and the output capacitor to GND/DC– should be as short and as thick as possible in order to minimize parasitic inductance.

SFR Definition 16.2. DC0CF: DC-DC Converter Configuration

Bit	7	6	5	4	3	2	1	0
Name	LPEN	CLKDIV[1:0]		AD0CKINV	CLKINV	ILIMIT	VDDSLP	CLKSEL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x96

Bit	Name	Function
7	LPEN	**Low Power Mode Enable.** Enables the dc-dc low power mode which reduces bias currents, reduces peak inductor current, and increases efficiency for low load currents. Only available on ‘F912 and ‘F902 devices. 0: Low Power Mode Disabled. 1: Low Power Mode Enabled.
6:5	CLKDIV[1:0]	**DC-DC Clock Divider.** Divides the dc-dc converter clock when the system clock is selected as the clock source for dc-dc converter. These bits are ignored when the dc-dc converter is clocked from its local oscillator. 00: The dc-dc converter clock is system clock divided by 1. 01: The dc-dc converter clock is system clock divided by 2. 10: The dc-dc converter clock is system clock divided by 4. 11: The dc-dc converter clock is system clock divided by 8.
4	AD0CKINV	**ADC0 Clock Inversion (Clock Invert During Sync).** Inverts the ADC0 SAR clock derived from the dc-dc converter clock when the SYNC bit (DC0CN.3) is enabled. This bit is ignored when the SYNC bit is set to zero. 0: ADC0 SAR clock is inverted. 1: ADC0 SAR clock is not inverted.
3	CLKINV	**DC-DC Converter Clock Invert.** Inverts the system clock used as the input to the dc-dc clock divider. 0: The dc-dc converter clock is not inverted. 1: The dc-dc converter clock is inverted.
2	ILIMIT	**Peak Current Limit Threshold.** Sets the threshold for the maximum allowed peak inductor current according to Table 16.1.
1	VDDSLP	**VDD-DC+ Sleep Mode Connection.** Specifies the power source for VDD/DC+ in Sleep Mode when the dc-dc converter is enabled. 0: VDD-DC+ connected to VBAT in Sleep Mode. 1: VDD-DC+ is floating in Sleep Mode.
0	CLKSEL	**DC-DC Converter Clock Source Select.** Specifies the dc-dc converter clock source. 0: The dc-dc converter is clocked from its local oscillator. 1: The dc-dc converter is clocked from the system clock.

20.1. SmaRTClock Interface

The SmaRTClock Interface consists of three registers: RTC0KEY, RTC0ADR, and RTC0DAT. These interface registers are located on the CIP-51's SFR map and provide access to the SmaRTClock internal registers listed in Table 20.1. The SmaRTClock internal registers can only be accessed indirectly through the SmaRTClock Interface.

Table 20.1. SmaRTClock Internal Registers

SmaRTClock Address	SmaRTClock Register	Register Name	Description
0x00–0x03	CAPTUREn	SmaRTClock Capture Registers	Four Registers used for setting the 32-bit SmaRTClock timer or reading its current value.
0x04	RTC0CN	SmaRTClock Control Register	Controls the operation of the SmaRTClock State Machine.
0x05	RTC0XCN	SmaRTClock Oscillator Control Register	Controls the operation of the SmaRTClock Oscillator. **Note:** Some bits in this register are only available on 'F912 and 'F902 devices.
0x06	RTC0XCF	SmaRTClock Oscillator Configuration Register	Controls the value of the progammable oscillator load capacitance and enables/disables AutoStep.
0x07	RTC0PIN	SmaRTClock Pin Configuration Register	Forces XTAL3 and XTAL4 to be internally shorted. **Note:** This register also contains other reserved bits which should not be modified.
0x08–0x0B	ALARMn	SmaRTClock Alarm Registers	Four registers used for setting or reading the 32-bit SmaRTClock alarm value.

20.1.1. SmaRTClock Lock and Key Functions

The SmaRTClock Interface is protected with a lock and key function. The SmaRTClock Lock and Key Register (RTC0KEY) must be written with the correct key codes, in sequence, before writes and reads to RTC0ADR and RTC0DAT may be performed. The key codes are: 0xA5, 0xF1. There are no timing restrictions, but the key codes must be written in order. If the key codes are written out of order, the wrong codes are written, or an indirect register read or write is attempted while the interface is locked, the SmaRTClock interface will be disabled, and the RTC0ADR and RTC0DAT registers will become inaccessible until the next system reset. Once the SmaRTClock interface is unlocked, software may perform any number of accesses to the SmaRTClock registers until the interface is re-locked or the device is reset. Any write to RTC0KEY while the SmaRTClock interface is unlocked will re-lock the interface.

Reading the RTC0KEY register at any time will provide the SmaRTClock Interface status and will not interfere with the sequence that is being written. The RTC0KEY register description in SFR Definition 20.1 lists the definition of each status code.

Internal Register Definition 20.4. RTC0CN: SmaRTClock Control

Bit	7	6	5	4	3	2	1	0
Name	RTC0EN	MCLKEN	OSCFAIL	RTC0TR	RTC0AEN	ALRM	RTC0SET	RTC0CAP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	Varies	0	0	0	0	0

SmaRTClock Address = 0x04

Bit	Name	Function		
7	RTC0EN	**SmaRTClock Enable.** Enables/disables the SmaRTClock oscillator and associated bias currents. 0: SmaRTClock oscillator disabled. 1: SmaRTClock oscillator enabled.		
6	MCLKEN	**Missing SmaRTClock Detector Enable.** Enables/disables the missing SmaRTClock detector. 0: Missing SmaRTClock detector disabled. 1: Missing SmaRTClock detector enabled.		
5	OSCFAIL	**SmaRTClock Oscillator Fail Event Flag.** Set by hardware when a missing SmaRTClock detector timeout occurs. Must be cleared by software. The value of this bit is not defined when the SmaRTClock oscillator is disabled.		
4	RTC0TR	**SmaRTClock Timer Run Control.** Controls if the SmaRTClock timer is running or stopped (holds current value). 0: SmaRTClock timer is stopped. 1: SmaRTClock timer is running.		
3	RTC0AEN	**SmaRTClock Alarm Enable.** Enables/disables the SmaRTClock alarm function. Also clears the ALRM flag. 0: SmaRTClock alarm disabled. 1: SmaRTClock alarm enabled.		
2	ALRM	**SmaRTClock Alarm Event Flag and Auto Reset Enable.** Reads return the state of the alarm event flag. Writes enable/disable the Auto Reset function.	Read: 0: SmaRTClock alarm event flag is de-asserted. 1: SmaRTClock alarm event flag is asserted.	Write: 0: Disable Auto Reset. 1: Enable Auto Reset.
1	RTC0SET	**SmaRTClock Timer Set.** Writing 1 initiates a SmaRTClock timer set operation. This bit is cleared to 0 by hardware to indicate that the timer set operation is complete.		
0	RTC0CAP	**SmaRTClock Timer Capture.** Writing 1 initiates a SmaRTClock timer capture operation. This bit is cleared to 0 by hardware to indicate that the timer capture operation is complete.		
Note: The ALRM flag will remain asserted for a maximum of one SmaRTClock cycle. See Section “Power Management” on page 143 for information on how to capture a SmaRTClock Alarm event using a flag which is not automatically cleared by hardware.				

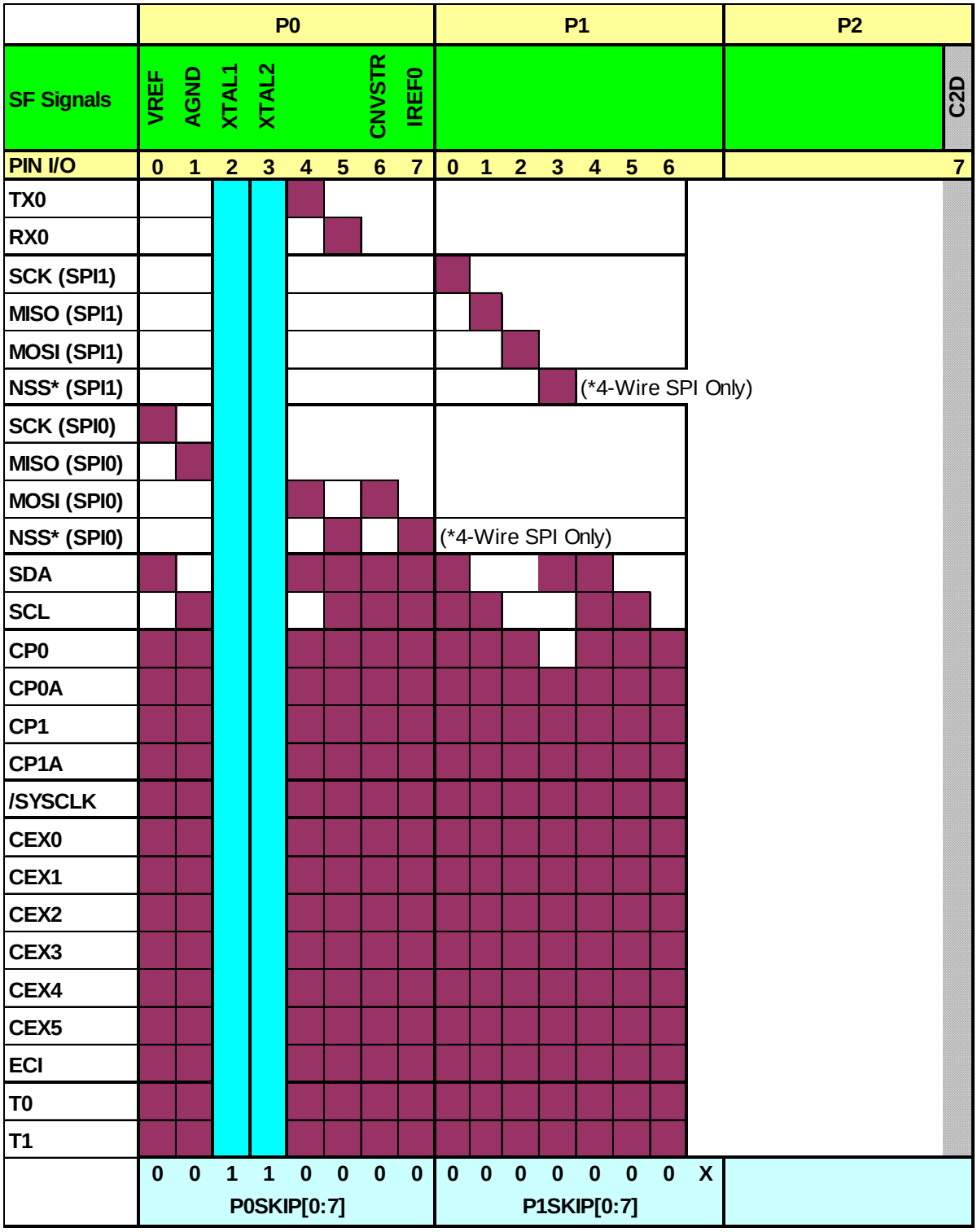

Figure 21.4. Crossbar Priority Decoder with Crystal Pins Skipped

master continues its transmission without interruption; the losing master becomes a slave and receives the rest of the transfer if addressed. This arbitration scheme is non-destructive: one device always wins, and no data is lost.

22.3.3. Clock Low Extension

SMBus provides a clock synchronization mechanism, similar to I^2C, which allows devices with different speed capabilities to coexist on the bus. A clock-low extension is used during a transfer in order to allow slower slave devices to communicate with faster masters. The slave may temporarily hold the SCL line LOW to extend the clock low period, effectively decreasing the serial clock frequency.

22.3.4. SCL Low Timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a “timeout” condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.

When the SMBTOE bit in SMB0CF is set, Timer 3 is used to detect SCL low timeouts. Timer 3 is forced to reload when SCL is high, and allowed to count when SCL is low. With Timer 3 enabled and configured to overflow after 25 ms (and SMBTOE set), the Timer 3 interrupt service routine can be used to reset (disable and re-enable) the SMBus in the event of an SCL low timeout.

22.3.5. SCL High (SMBus Free) Timeout

The SMBus specification stipulates that if the SCL and SDA lines remain high for more that 50 µs, the bus is designated as free. When the SMBFTE bit in SMB0CF is set, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods (as defined by the timer configured for the SMBus clock source). If the SMBus is waiting to generate a Master START, the START will be generated following this timeout. Note that a clock source is required for free timeout detection, even in a slave-only implementation.

24.5. Serial Clock Phase and Polarity

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI Configuration Register (SPInCFG). The CKPHA bit (SPInCFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPInCFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIENn bit, SPInCN.0) when changing the clock phase or polarity. The clock and data line relationships for master mode are shown in Figure 24.5. For slave mode, the clock and data relationships are shown in Figure 24.6 and Figure 24.7. Note that CKPHA must be set to 0 on both the master and slave SPI when communicating between two of the following devices: C8051F04x, C8051F06x, C8051F12x, C8051F31x, C8051F32x, and C8051F33x.

The SPIn Clock Rate Register (SPInCKR) as shown in SFR Definition 24.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

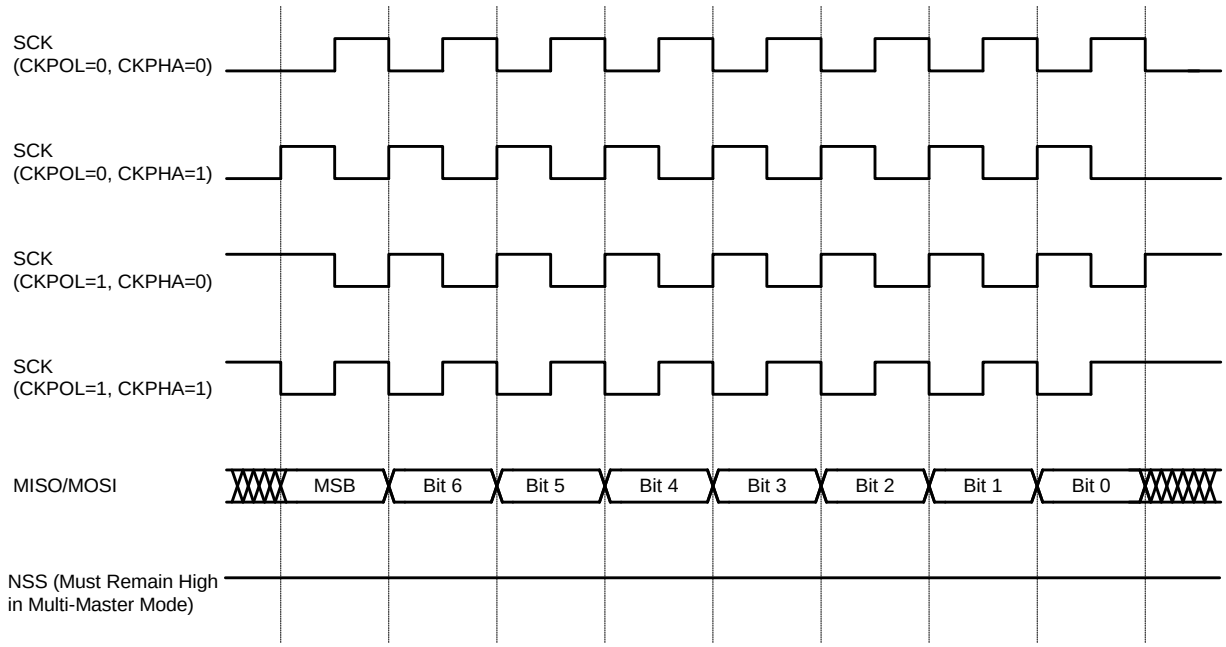

Figure 24.5. Master Mode Data/Clock Timing

SFR Definition 24.1. SPInCFG: SPI Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Addresses: SPI0CFG = 0xA1, SPI1CFG = 0x84
SFR Pages: SPI0CFG = 0x0, SPI1CFG = 0x0

Bit	Name	Function
7	SPIBSY	**SPI Busy.** This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	**Master Mode Enable.** 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	**SPI Clock Phase.** 0: Data centered on first edge of SCK period.* 1: Data centered on second edge of SCK period.*
4	CKPOL	**SPI Clock Polarity.** 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	**Slave Selected Flag.** Set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	**NSS Instantaneous Pin Input.** This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	**Shift Register Empty (valid in slave mode only).** Set to logic 1 when data has been transferred in/out of the shift register, and there is no data is available to read from the transmit buffer or write to the receive buffer. Set to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. Note: SRMT = 1 in Master Mode.
0	RXBMT	**Receive Buffer Empty (valid in slave mode only).** Set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. Note: RXBMT = 1 in Master Mode.

***Note:** In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 24.1 for timing parameters.

SFR Definition 24.4. SPInDAT: SPI Data

Bit	7	6	5	4	3	2	1	0
Name	SPInDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Addresses: SPI0DAT = 0xA3, SPI1DAT = 0x86
SFR Pages: SPI0DAT = 0x0, SPI1DAT = 0x0

Bit	Name	Function
7:0	SPInDAT	**SPIn Transmit and Receive Data.** The SPInDAT register is used to transmit and receive SPIn data. Writing data to SPInDAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPInDAT returns the contents of the receive buffer.