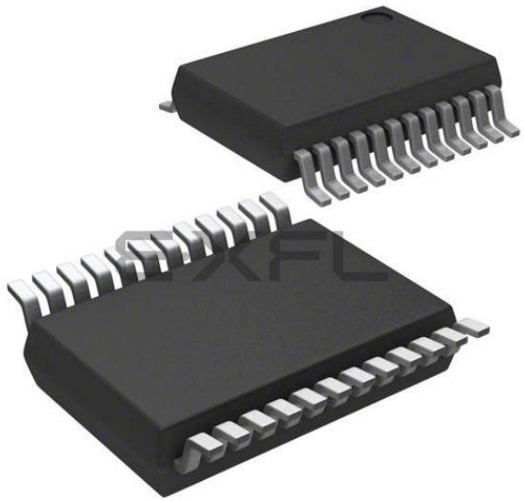

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f911-gu

1.3. Serial Ports

The C8051F91x-C8051F90x Family includes an SMBus/I^2C interface, a full-duplex UART with enhanced baud rate configuration, and two Enhanced SPI interfaces. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.4. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with six programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8. ‘F912 and ‘F902 devices also support a SmaRTClock divided by 8 clock source.

Each capture/compare module can be configured to operate in a variety of modes: edge-triggered capture, software timer, high-speed output, pulse width modulator (8, 9, 10, 11, or 16-bit), or frequency output. Additionally, Capture/Compare Module 5 offers watchdog timer (WDT) capabilities. Following a system reset, Module 5 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

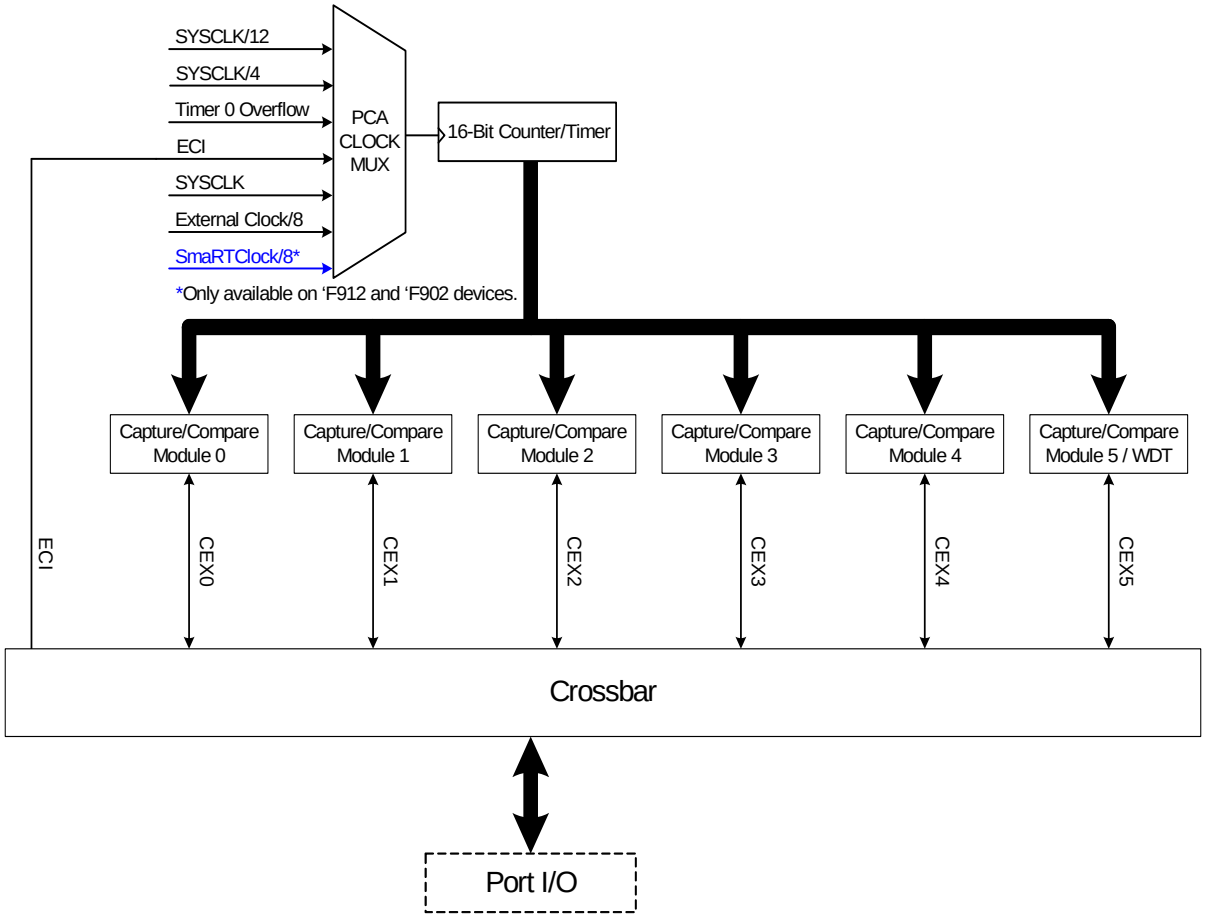


Figure 1.6. PCA Block Diagram

Table 3.1. Pin Definitions for the C8051F91x-C8051F90x (Continued)

Name	Pin Numbers		Type	Description
	'F912-GM 'F902-GM 'F911-GM 'F901-GM	'F912-GU 'F902-GU 'F911-GU 'F901-GU		
XTAL3	9	12	A In	SmaRTClock Oscillator Crystal Input. See Section 20 for a complete description.
XTAL4	8	11	A Out	SmaRTClock Oscillator Crystal Output. See Section 20 for a complete description.
P0.0	24	3	D I/O or A In	Port 0.0. See Port I/O Section for a complete description.
V_{REF}			A In A Out	External V_{REF} Input. Internal V_{REF} Output. External V_{REF} decoupling capacitors are recommended. See Section "5.9. Voltage and Ground Reference Options" on page 83.
P0.1	23	2	D I/O or A In	Port 0.1. See Port I/O Section for a complete description.
AGND			G	Optional Analog Ground. See Section "5.9. Voltage and Ground Reference Options" on page 83.
P0.2	22	1	D I/O or A In	Port 0.2. See Port I/O Section for a complete description.
XTAL1			A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator. See Section "19. Clocking Sources" on page 179.
RTCOUT*				Buffered SmaRTClock oscillator output.
P0.3	21	24	D I/O or A In	Port 0.3. See Section "21. Port Input/Output" on page 205 for a complete description.
XTAL2			A Out	External Clock Output. This pin is the excitation driver for an external crystal or resonator.
			D In	External Clock Input. This pin is the external clock input in external CMOS clock mode.
			A In	External Clock Input. This pin is the external clock input in capacitor or RC oscillator configurations. See Section "19. Clocking Sources" on page 179 for complete details.
WAKEOUT*				Wake-up request signal to wake up external devices (e.g. an external DC-DC converter).
P0.4	20	23	D I/O or A In	Port 0.4. See Section "21. Port Input/Output" on page 205 for a complete description.
TX			D Out	UART TX Pin. See Section "21. Port Input/Output" on page 205.
P0.5	19	22	D I/O or A In	Port 0.5. See Section "21. Port Input/Output" on page 205 for a complete description.
RX			D In	UART RX Pin. See Section "21. Port Input/Output" on page 205.

***Note:** Available only on the C8051F912/02.

4. Electrical Characteristics

Throughout the Electrical Characteristics chapter, “VDD” refers to the VDD/DC+ Supply Voltage.

Blue indicates a feature only available on ‘F912 and ‘F902 devices.

4.1. Absolute Maximum Specifications

Table 4.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Port I/O Pin or $\overline{\text{RST}}$ with respect to GND	VDD > 2.2 V VDD < 2.2 V	–0.3 –0.3	— —	5.8 VDD + 3.6	V
Voltage on VBAT with respect to GND	One-Cell Mode (F912/02 One-Cell Mode (F911/01) Two-Cell Mode	–0.3 –0.3 –0.3	— — —	4.0 2.0 4.0	V
Voltage on VDD/DC+ with respect to GND		–0.3	—	4.0	V
Maximum total current through VBAT, DCEN, VDD/DC+ or GND		—	—	500	mA
Maximum current through $\overline{\text{RST}}$ or any Port pin		—	—	100	mA
Maximum total current through all Port pins		—	—	200	mA
DC-DC Converter Output Power		—	—	110	mW

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

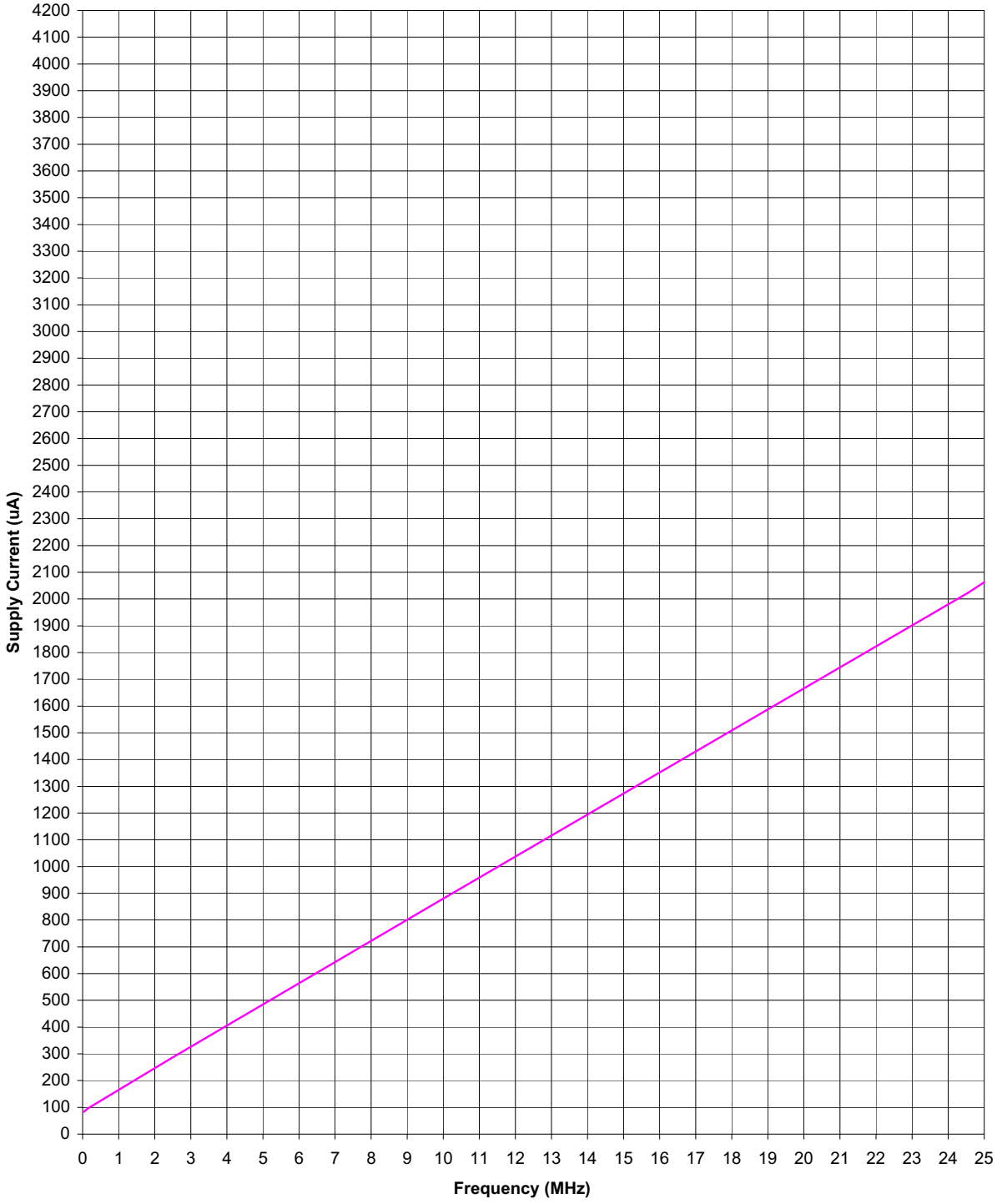


Figure 4.2. Idle Mode Current (External CMOS Clock)

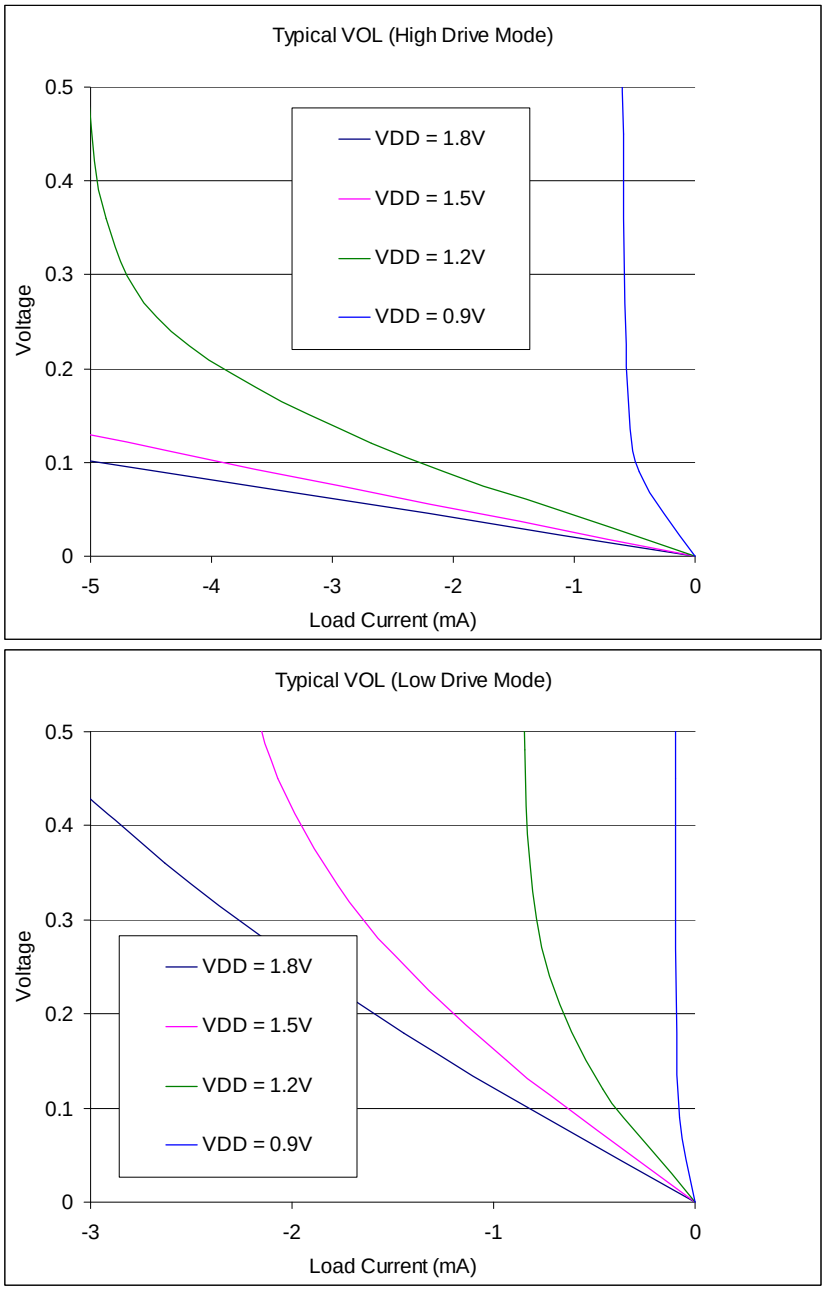


Figure 4.10. Typical VOL Curves, 0.9–1.8 V

Table 4.4. Reset Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{RST}$ Output Low Voltage	I_{OL} = 1.4 mA,	—	—	0.6	V
$\overline{RST}$ Input High Voltage	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
	V_{DD} = 0.9 to 2.0 V	0.7 x V_{DD}	—	—	V
$\overline{RST}$ Input Low Voltage	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
	V_{DD} = 0.9 to 2.0 V	—	—	0.3 x V_{DD}	V
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 0.0 V, VDD = 1.8 V	—	4	—	µA
	$\overline{RST}$ = 0.0 V, VDD = 3.6 V	—	20	35	
VDD/DC+ Monitor Threshold (V_{RST})	Early Warning	1.8	1.85	1.9	V
	Reset Trigger (all power modes except Sleep)	1.7	1.75	1.8	
VBAT Ramp Time for Power On	VBAT Ramp from 0–0.9 V	—	—	3	ms
VBAT Monitor Threshold (V_{POR})	Initial Power-On (VBAT Rising)	—	0.75	—	V
	Early Warning	**0.9**	**1.0**	**1.1**	
	Brownout Condition (VBAT Falling)	0.7	0.8	0.9	
	Recovery from Brownout (VBAT Rising)	—	0.95	—	
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation	100	525	1000	µs
Minimum System Clock w/ Missing Clock Detector Enabled	System clock frequency which triggers a missing clock detector timeout	—	2	10	kHz
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	10	—	µs
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs
V_{DD} Monitor Turn-on Time		—	300	—	ns
V_{DD} Monitor Supply Current		—	10	—	µA

***Note:** **Blue** indicates a feature only available on ‘F912 and ‘F902 devices.

SFR Definition 5.2. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD08BE	AD0TM	AMP0GN
Type	R/W					R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	0

SFR Page = 0x0; SFR Address = 0xBC

Bit	Name	Function
7:3	AD0SC[4:0]	**ADC0 SAR Conversion Clock Divider.** SAR Conversion clock is derived from FCLK by the following equation, where *AD0SC* refers to the 5-bit value held in bits AD0SC[4:0]. SAR Conversion clock requirements are given in Table 4.10. BURSTEN = 0: FCLK is the current system clock. BURSTEN = 1: FCLK is the 20 MHz low power oscillator, independent of the system clock. $AD0SC = \frac{FCLK}{CLK_{SAR}} - 1$ * *Round the result up. or $CLK_{SAR} = \frac{FCLK}{AD0SC + 1}$
2	AD08BE	**ADC0 8-Bit Mode Enable.** 0: ADC0 operates in 10-bit mode (normal operation). 1: ADC0 operates in 8-bit mode.
1	AD0TM	**ADC0 Track Mode.** Selects between Normal or Delayed Tracking Modes. 0: Normal Track Mode: When ADC0 is enabled, conversion begins immediately following the start-of-conversion signal. 1: Delayed Track Mode: When ADC0 is enabled, conversion begins 3 SAR clock cycles following the start-of-conversion signal. The ADC is allowed to track during this time.
0	AMP0GN	**ADC0 Gain Control.** 0: The on-chip PGA gain is 0.5. 1: The on-chip PGA gain is 1.

7.5. Comparator Register Descriptions

The SFRs used to enable and configure the comparators are described in the following register descriptions. A Comparator must be enabled by setting the CPnEN bit to logic 1 before it can be used. From an enabled state, a comparator can be disabled and placed in a low power state by clearing the CPnEN bit to logic 0.

Important Note About Comparator Settings: False rising and falling edges can be detected by the Comparator while powering on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed. The Comparator Power Up Time is specified in Section “Table 4.14. Comparator Electrical Characteristics” on page 58.

SFR Definition 7.1. CPT0CN: Comparator 0 Control

Bit	7	6	5	4	3	2	1	0
Name	CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0HYP[1:0]		CP0HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0x9B

Bit	Name	Function
7	CP0EN	**Comparator0 Enable Bit.** 0: Comparator0 Disabled. 1: Comparator0 Enabled.
6	CP0OUT	**Comparator0 Output State Flag.** 0: Voltage on CP0+ < CP0–. 1: Voltage on CP0+ > CP0–.
5	CP0RIF	**Comparator0 Rising-Edge Flag. Must be cleared by software.** 0: No Comparator0 Rising Edge has occurred since this flag was last cleared. 1: Comparator0 Rising Edge has occurred.
4	CP0FIF	**Comparator0 Falling-Edge Flag. Must be cleared by software.** 0: No Comparator0 Falling-Edge has occurred since this flag was last cleared. 1: Comparator0 Falling-Edge has occurred.
3-2	CP0HYP[1:0]	**Comparator0 Positive Hysteresis Control Bits.** 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = Hysteresis 1. 10: Positive Hysteresis = Hysteresis 2. 11: Positive Hysteresis = Hysteresis 3 (Maximum).
1:0	CP0HYN[1:0]	**Comparator0 Negative Hysteresis Control Bits.** 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = Hysteresis 1. 10: Negative Hysteresis = Hysteresis 2. 11: Negative Hysteresis = Hysteresis 3 (Maximum).

Table 11.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved. SFRs highlighted in **blue** are only available on ‘F912 and ‘F902 devices.

Register	Address	SFR Page	Description	Page
PCA0MD	0xD9	0x0	PCA0 Mode	307
PCA0PWM	0xDF	0x0	PCA0 PWM Configuration	308
PCON	0x87	0x0	Power Control	151
PMU0CF	0xB5	0x0	PMU0 Configuration	149
PMU0MD	0xB5	0xF	**PMU0 Mode**	150
PSCTL	0x8F	0x0	Program Store R/W Control	140
PSW	0xD0	All	Program Status Word	106
REF0CN	0xD1	0x0	Voltage Reference Control	85
REG0CN	0xC9	0x0	Voltage Regulator (VREG0) Control	170
RSTSRC	0xEF	0x0	Reset Source Configuration/Status	178
RTC0ADR	0xAC	0x0	RTC0 Address	193
RTC0DAT	0xAD	0x0	RTC0 Data	193
RTC0KEY	0xAE	0x0	RTC0 Key	192
SBUF0	0x99	0x0	UART0 Data Buffer	253
SCON0	0x98	0x0	UART0 Control	252
SFRPAGE	0xA7	All	SFR Page	115
SMB0ADM	0xF5	0x0	SMBus Slave Address Mask	237
SMB0ADR	0xF4	0x0	SMBus Slave Address	237
SMB0CF	0xC1	0x0	SMBus Configuration	232
SMB0CN	0xC0	0x0	SMBus Control	234
SMB0DAT	0xC2	0x0	SMBus Data	238
SP	0x81	All	Stack Pointer	105
SPI0CFG	0xA1	0x0	SPI0 Configuration	263
SPI0CKR	0xA2	0x0	SPI0 Clock Rate Control	265
SPI0CN	0xF8	0x0	SPI0 Control	264
SPI0DAT	0xA3	0x0	SPI0 Data	266
SPI1CFG	0x84	0x0	SPI1 Configuration	263
SPI1CKR	0x85	0x0	SPI1 Clock Rate Control	265
SPI1CN	0xB0	0x0	SPI1 Control	264
SPI1DAT	0x86	0x0	SPI1 Data	266
TCON	0x88	0x0	Timer/Counter Control	276
TH0	0x8C	0x0	Timer/Counter 0 High	279
TH1	0x8D	0x0	Timer/Counter 1 High	279

Table 11.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved. SFRs highlighted in **blue** are only available on ‘F912 and ‘F902 devices.

Register	Address	SFR Page	Description	Page
TL0	0x8A	0x0	Timer/Counter 0 Low	278
TL1	0x8B	0x0	Timer/Counter 1 Low	278
TMOD	0x89	0x0	Timer/Counter Mode	277
TMR2CN	0xC8	0x0	Timer/Counter 2 Control	283
TMR2H	0xCD	0x0	Timer/Counter 2 High	285
TMR2L	0xCC	0x0	Timer/Counter 2 Low	285
TMR2RLH	0xCB	0x0	Timer/Counter 2 Reload High	284
TMR2RLL	0xCA	0x0	Timer/Counter 2 Reload Low	284
TMR3CN	0x91	0x0	Timer/Counter 3 Control	289
TMR3H	0x95	0x0	Timer/Counter 3 High	291
TMR3L	0x94	0x0	Timer/Counter 3 Low	291
TMR3RLH	0x93	0x0	Timer/Counter 3 Reload High	290
TMR3RLL	0x92	0x0	Timer/Counter 3 Reload Low	290
TOFFH	0x86	0xF	Temperature Offset High	82
TOFFL	0x85	0xF	Temperature Offset Low	82
VDM0CN	0xFF	0x0	VDD Monitor Control	175
XBR0	0xE1	0x0	Port I/O Crossbar Control 0	212
XBR1	0xE2	0x0	Port I/O Crossbar Control 1	213
XBR2	0xE3	0x0	Port I/O Crossbar Control 2	214

12.5. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described in the following register descriptions. Refer to the data sheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

SFR Definition 12.1. IE: Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name	EA	ESPI0	ET2	ES0	ET1	EX1	ET0	EX0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xA8; Bit-Addressable

Bit	Name	Function
7	EA	**Enable All Interrupts.** Globally enables/disables all interrupts. It overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	ESPI0	**Enable Serial Peripheral Interface (SPI0) Interrupt.** This bit sets the masking of the SPI0 interrupts. 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPI0.
5	ET2	**Enable Timer 2 Interrupt.** This bit sets the masking of the Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable interrupt requests generated by the TF2L or TF2H flags.
4	ES0	**Enable UART0 Interrupt.** This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	**Enable Timer 1 Interrupt.** This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupt requests generated by the TF1 flag.
2	EX1	**Enable External Interrupt 1.** This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupt requests generated by the $\overline{\text{INT1}}$ input.
1	ET0	**Enable Timer 0 Interrupt.** This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupt requests generated by the TF0 flag.
0	EX0	**Enable External Interrupt 0.** This bit sets the masking of External Interrupt 0. 0: Disable external interrupt 0. 1: Enable interrupt requests generated by the $\overline{\text{INT0}}$ input.

outputs during sleep mode, then the VDD/DC+ output can be made to float during Sleep mode by setting the VDDSLP bit in the DC0CF register to 1.

Setting this bit can provide power savings in two ways. First, if the sleep interval is relatively short and the VDD/DC+ load current (include leakage currents) is negligible, then the capacitor on VDD/DC+ will maintain the output voltage near the programmed value, which means that the VDD/DC+ capacitor will not need to be recharged upon every wake up event. The second power advantage is that internal or external low-power circuits that require more than 1.8 V can continue to function during Sleep mode without operating the dc-dc converter, powered by the energy stored in the 1 µF output decoupling capacitor. For example, the C8051F91x-C8051F90x comparators require about 0.4 µA when operating in their lowest power mode. If the dc-dc converter output were increased to 3.3 V just before putting the device into Sleep mode, then the comparator could be powered for more than 3 seconds before the output voltage dropped to 1.8 V. In this example, the overall energy consumption would be much lower than if the dc-dc converter were kept running to power the comparator.

If the load current on VDD/DC+ is high enough to discharge the VDD/DC+ capacitance to a voltage lower than VBAT during the sleep interval, an internal diode will prevent VDD/DC+ from dropping more than a few hundred millivolts below VBAT. There may be some additional leakage current from VBAT to ground when the VDD/DC+ level falls below VBAT, but this leakage current should be small compared to the current from VDD/DC+.

The amount of time that it takes for a device configured in one-cell mode to wake up from Sleep mode depends on a number of factors, including the dc-dc converter clock speed, the settings of the SWSEL, ILIMIT, and LPEN bits, the battery internal resistance, the load current, and the difference between the VBAT voltage level and the programmed output voltage. The wake up time can be as short as 2 µs, though it is more commonly in the range of 5 to 10 µs, and it can exceed 50 µs under extreme conditions.

See Section “14. Power Management” on page 143 for more information about sleep mode.

16.9. Bypass Mode (C8051F912/02 only)

During normal operation, if the dc-dc converter input voltage exceeds the programmed output voltage, the converter will stop switching and the Diode Bypass switch will remain in the “on” state. The output voltage will be equal to the input voltage minus any resistive loss in the switch and all of the converter’s analog circuits will remain biased. The bypass feature automatically shuts off the dc-dc converter when the input voltage is greater than the programmed output voltage by 150 mV. In bypass, the Diode Bypass switch and dc-dc converter bias currents are disabled except for the voltage comparison circuitry (~ 3 µA, depending on the configuration settings in the DC0MD register). If the input voltage drops within 50 mV of the programmed output value, then the dc-dc converter automatically starts operating in the normal state. There is 100 mV voltage hysteresis built in the bypass comparator to enhance stability.

The bypass mode increases system operating time in systems which have a minimum operating voltage higher than the battery end of life voltage. For instance, if an external chip requires a minimum supply voltage of 2.7 V and a lithium coin cell battery is used as power source (end-of-life voltage is approximately 2 V), then the C8051F912/902’s dc-dc converter could be configured for an output voltage of 2.7 V with bypass mode enabled. The dc-dc converter would be bypassed when the battery was fresh, but as soon as the battery voltage dropped below 2.75 V, the dc-dc converter would turn on to ensure that the external chip was provided with a minimum of 2.7 V for the remainder of the battery life.

16.10. Low Power Mode (C8051F912/02 only)

Setting the LPEN bit in the DC0CF register will enable a Low Power Mode for the dc-dc converter. In Low Power Mode, the bias currents are substantially reduced, which can lead to an efficiency improvement with light load currents (generally less than a few mA). The drawback to this mode is that the response time of the converter’s analog blocks is increased; larger delay in the circuits controlling the Diode Bypass switch can lead to loss of efficiency at medium and high load currents due to reverse leakage in the switch. The Low power mode also reduces the peak inductor current limit as shown in Table 16.1.

19. Clocking Sources

C8051F91x-C8051F90x devices include a programmable precision internal oscillator, an external oscillator drive circuit, a low power internal oscillator, and a SmaRTClock real time clock oscillator. The precision internal oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 19.1. The external oscillator can be configured using the OSCXCN register. The low power internal oscillator is automatically enabled and disabled when selected and deselected as a clock source. SmaRTClock operation is described in the SmaRTClock oscillator chapter.

The system clock (SYSCLK) can be derived from the precision internal oscillator, external oscillator, low power internal oscillator, or SmaRTClock oscillator. The global clock divider can generate a system clock that is 1, 2, 4, 8, 16, 32, 64, or 128 times slower that the selected input clock source. Oscillator electrical specifications can be found in the Electrical Specifications Chapter.

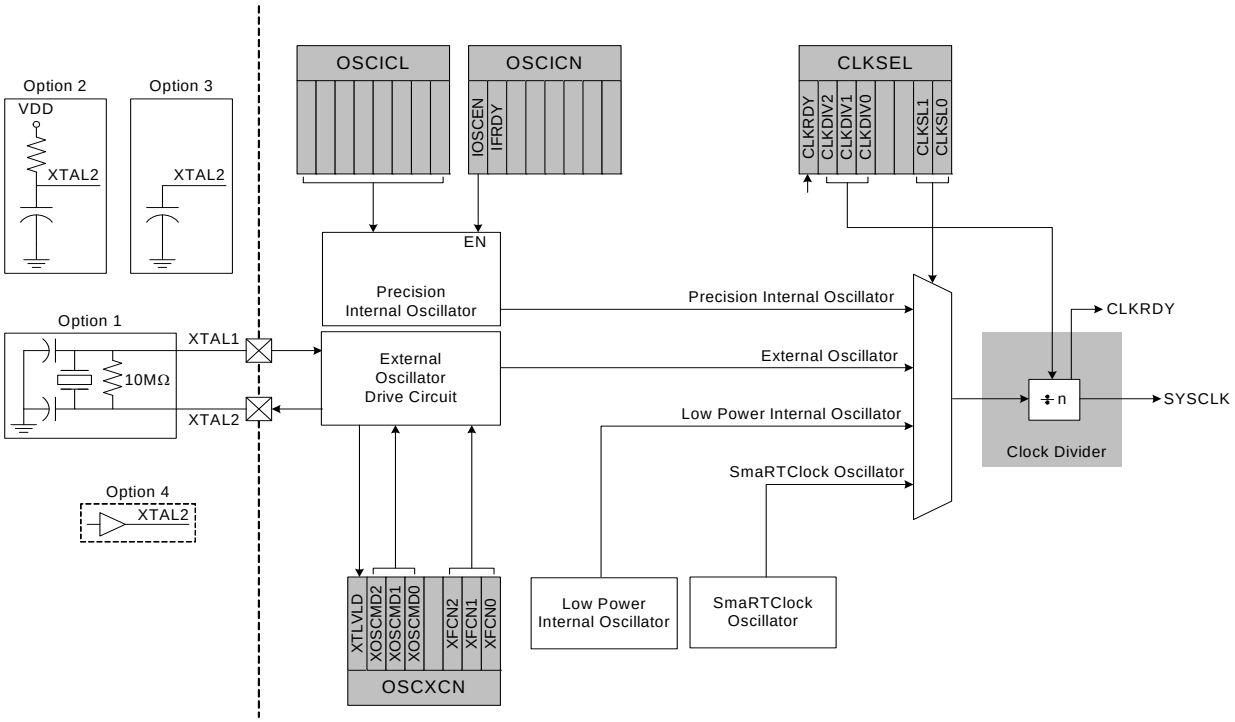


Figure 19.1. Clocking Sources Block Diagram

The proper way of changing the system clock when both the clock source and the clock divide value are being changed is as follows:

If switching from a fast “undivided” clock to a slower “undivided” clock:

a. Change the clock divide value.

b. Poll for CLKRDY > 1.

c. Change the clock source.

If switching from a slow “undivided” clock to a faster “undivided” clock:

a. Change the clock source.

b. Change the clock divide value.

c. Poll for CLKRDY > 1.

SFR Definition 19.4. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	XCLKVLD	XOSCMD[2:0]			Reserved	XFCN[2:0]		
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xB1

Bit	Name	Function
7	XCLKVLD	**External Oscillator Valid Flag.** Provides External Oscillator status and is valid at all times for all modes of operation except External CMOS Clock Mode and External CMOS Clock Mode with divide by 2. In these modes, XCLKVLD always returns 0. 0: External Oscillator is unused or not yet stable. 1: External Oscillator is running and stable.
6:4	XOSCMD	**External Oscillator Mode Bits.** Configures the external oscillator circuit to the selected mode. 00x: External Oscillator circuit disabled. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide by 2 stage. 100: RC Oscillator Mode. 101: Capacitor Oscillator Mode. 110: Crystal Oscillator Mode. 111: Crystal Oscillator Mode with divide by 2 stage.
3	Reserved	**Reserved.** Read = 0b. Must Write 0b.
2:0	XFCN	**External Oscillator Frequency Control Bits.** Controls the external oscillator bias current. 000-111: See Table 19.1 on page 181 (Crystal Mode) or Table 19.2 on page 182 (RC or C Mode) for recommended settings.

21.1.3. Interfacing Port I/O to 5 V and 3.3 V Logic

All Port I/O configured for digital, open-drain operation are capable of interfacing to digital logic operating at a supply voltage higher than 4.5 V and less than 5.25 V. When the supply voltage is in the range of 1.8 to 2.2 V, the I/O may also interface to digital logic operating between 3.0 to 3.6 V if the input signal frequency is less than 12.5 MHz or less than 25 MHz if the signal rise time (10% to 90%) is less than 1.2 ns. When operating at a supply voltage above 2.2 V, the device should not interface to 3.3 V logic; however, interfacing to 5 V logic is permitted. An external pull-up resistor to the higher supply voltage is typically required for most systems.

Important Note:

- When interfacing to a signal that is between 4.5 and 5.25 V, the maximum clock frequency that may be input on a GPIO pin is 12.5 MHz. The exception to this rule is when routing an external CMOS clock to P0.3, in which case, a signal up to 25 MHz is valid as long as the rise time (10% to 90%) is shorter than 1.8 ns.
- When the supply voltage is less than 2.2 V and interfacing to a signal that is between 3.0 and 3.6 V, the maximum clock frequency that may be input on a GPIO pin is 3.125 MHz. The exception to this rule is when routing an external CMOS clock to P0.3, in which case, a signal up to 25 MHz is valid as long as the rise time (10% to 90%) is shorter than 1.2 ns.
- In a multi-voltage interface, the external pull-up resistor should be sized to allow a current of at least 150 µA to flow into the Port pin when the supply voltage is between (VDD/DC+ plus 0.4 V) and (VDD/DC+ plus 1.0 V). Once the Port pad voltage increases beyond this range, the current flowing into the Port pin is minimal.
- These guidelines only apply to multi-voltage interfaces. Port I/Os may always interface to digital logic operating at the same supply voltage.

21.1.4. Increasing Port I/O Drive Strength

Port I/O output drivers support a high and low drive strength; the default is low drive strength. The drive strength of a Port I/O can be configured using the PnDRV registers. See Section “4. Electrical Characteristics” on page 36 for the difference in output drive strength between the two modes.

21.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins P0.0–P1.6 can be assigned to various analog, digital, and external interrupt functions. The Port pins assuaged to analog functions should be configured for analog I/O and Port pins assuaged to digital or external interrupt functions should be configured for digital I/O.

21.2.1. Assigning Port I/O Pins to Analog Functions

Table 21.1 shows all available analog functions that need Port I/O assignments. **Port pins selected for these analog functions should have their digital drivers disabled (PnMDOUT.n = 0 and Port Latch = 1) and their corresponding bit in PnSKIP set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the Crossbar. Table 21.1 shows the potential mapping of Port I/O to each analog function.

Table 21.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P1.6	ADC0MX, PnSKIP
Comparator0 Input	P0.0–P1.6	CPT0MX, PnSKIP
Comparator1 Input	P0.0–P1.6	CPT1MX, PnSKIP

22.4. Using the SMBus

The SMBus can operate in both Master and Slave modes. The interface provides timing and shifting control for serial transfers; higher level protocol is determined by user software. The SMBus interface provides the following application-independent features:

- Byte-wise serial data transfers
- Clock signal generation on SCL (Master Mode only) and SDA data synchronization
- Timeout/bus error recognition, as defined by the SMB0CF configuration register
- START/STOP timing, detection, and generation
- Bus arbitration
- Interrupt generation
- Status information
- Optional hardware recognition of slave address and automatic acknowledgement of address/data

SMBus interrupts are generated for each data byte or slave address that is transferred. When hardware acknowledgement is disabled, the point at which the interrupt is generated depends on whether the hardware is acting as a data transmitter or receiver. When a transmitter (i.e. sending address/data, receiving an ACK), this interrupt is generated after the ACK cycle so that software may read the received ACK value; when receiving data (i.e. receiving address/data, sending an ACK), this interrupt is generated before the ACK cycle so that software may define the outgoing ACK value. If hardware acknowledgement is enabled, these interrupts are always generated after the ACK cycle. See Section 22.5 for more details on transmission sequences.

Interrupts are also generated to indicate the beginning of a transfer when a master (START generated), or the end of a transfer when a slave (STOP detected). Software should read the SMB0CN (SMBus Control register) to find the cause of the SMBus interrupt. The SMB0CN register is described in Section 22.4.2; Table 22.5 provides a quick SMB0CN decoding reference.

22.4.4. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

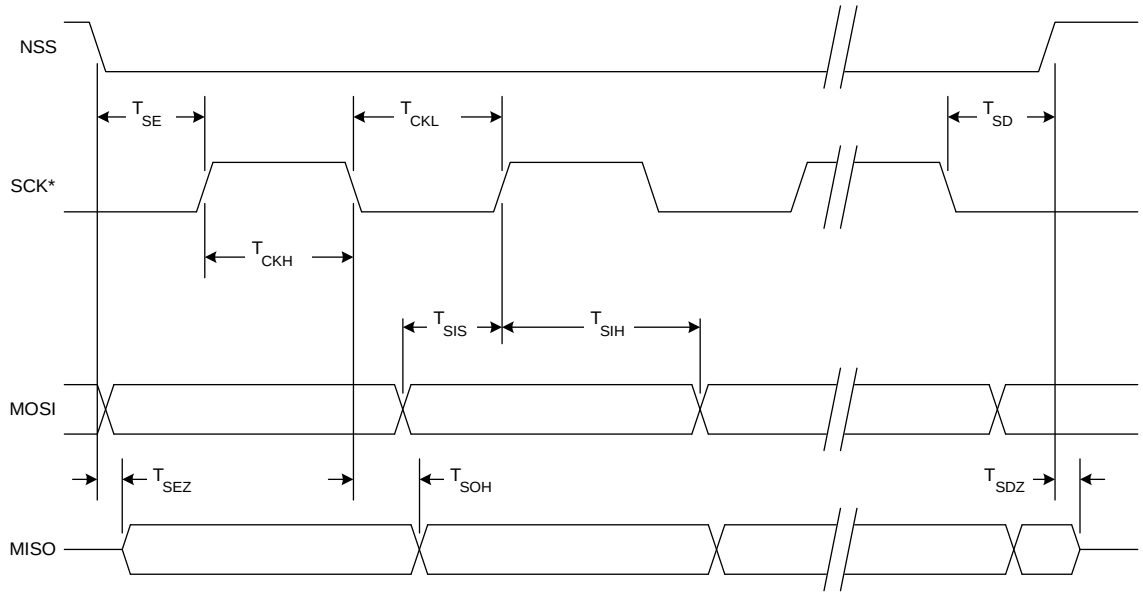
Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 22.5. SMB0DAT: SMBus Data

Bit	7	6	5	4	3	2	1	0
Name	SMB0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

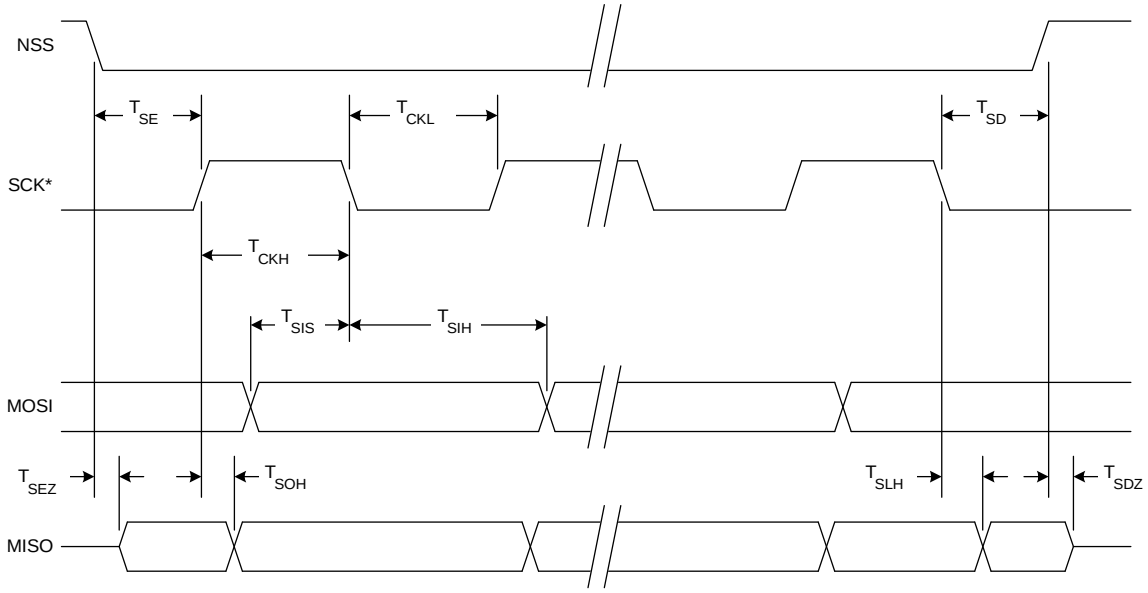
SFR Page = 0x0; SFR Address = 0xC2

Bit	Name	Function
7:0	SMB0DAT[7:0]	**SMBus Data.** The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.10. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.11. SPI Slave Timing (CKPHA = 1)

26.3.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8/9/10/11-bit) PWM modes. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the 16-bit counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a 16-bit comparator match (rising edge) occurs. The CF flag in PCA0CN can be used to detect the overflow (falling edge). The duty cycle for 16-Bit PWM Mode is given by Equation 26.4.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(65536 - PCA0CPn)}{65536}$$

Equation 26.4. 16-Bit PWM Duty Cycle

Using Equation 26.4, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

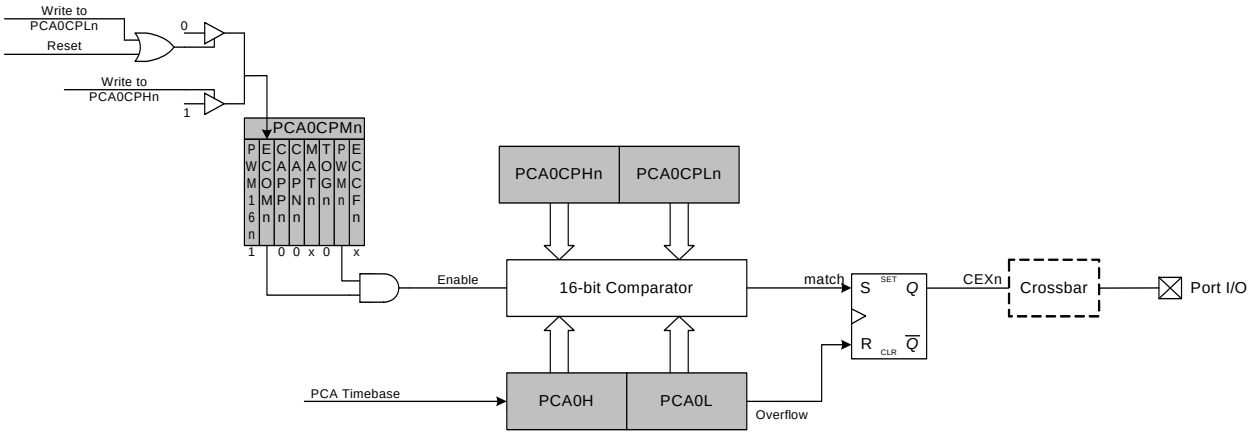


Figure 26.10. PCA 16-Bit PWM Mode