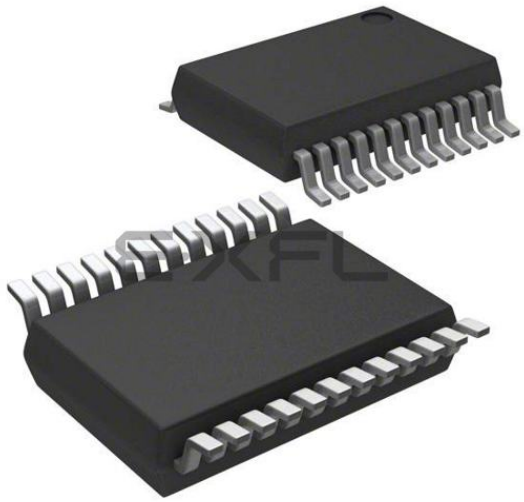

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f912-d-gu

Table 4.2. Global Electrical Characteristics (Continued)

–40 to +85 °C, 25 MHz system clock unless otherwise specified. See "AN358: Optimizing Low Power Operation of the ‘F9xx" for details on how to achieve the supply current specifications listed in this table.

Parameter	Conditions	Min	Typ	Max	Units

Notes:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the Flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of Flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 64-byte Flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 64-byte address boundaries.
4. Includes oscillator and regulator supply current.
5. IDD can be estimated for frequencies $\leq$14 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 90 µA. When using these numbers to estimate I_{DD} for >14 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 4 mA – (25 MHz – 20 MHz) x 0.102 mA/MHz = 3.5 mA assuming the same oscillator setting.
6. The supply current specifications in Table 4.2 are for two cell mode. The VBAT current in one-cell mode can be estimated using the following equation:

$$\text{VBAT Current (one-cell mode)} = \frac{\text{Supply Voltage} \times \text{Supply Current (two-cell mode)}}{\text{DC-DC Converter Efficiency} \times \text{VBAT Voltage}}$$

   The VBAT Voltage is the voltage at the VBAT pin, typically 0.9 to 1.8 V.
   The Supply Current (two-cell mode) is the data sheet specification for supply current.
   The Supply Voltage is the voltage at the VDD/DC+ pin, typically 1.8 to 3.3 V (default = 1.9 V).
   The DC-DC Converter Efficiency can be estimated using Figure 4.3–Figure 4.5.
7. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 2.1 mA – (25 MHz – 5 MHz) x 0.079 mA/MHz = 0.52 mA.
8. Internal LFO only available on ‘F912 and ‘F902 devices.
9. Ability to disable VBAT supply monitor only available on ‘F912 and ‘F902 devices.

Table 4.10. ADC0 Electrical Characteristics (Continued)

V_{DD} = 1.8 to 3.6V V, VREF = 1.65 V (REFSL[1:0] = 11), –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Inputs					
ADC Input Voltage Range	Single Ended (AIN+ – GND)	0	—	VREF	V
Absolute Pin Voltage with respect to GND	Single Ended	0	—	V_{DD}	V
Sampling Capacitance (C8051F912/11/02/01)	1x Gain 0.5x Gain	—	28 26	—	pF
Input Multiplexer Impedance		—	5	—	kΩ
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC0)	Conversion Mode (300 ksps) Tracking Mode (0 ksps)	— —	720 680	— —	µA
Power Supply Rejection	Internal High Speed VREF External VREF	— —	67 74	— —	dB

Notes:
1. **Blue** indicates a feature only available on ‘F912 and ‘F902 devices.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code.
4. Performance in 8-bit mode is similar to 10-bit mode.

Table 4.11. Temperature Sensor Electrical Characteristics

V_{DD} = 1.8 to 3.6V V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity		—	±1	—	°C
Slope		—	3.40	—	mV/°C
Slope Error[1]		—	40	—	µV/°C
Offset	Temp = 25 °C	—	1025	—	mV
Offset Error[1]	Temp = 25 °C	—	18	—	mV
Temperature Sensor Settling Time[2]	Initial Voltage=0 V Initial Voltage=3.6 V	—	—	3.0 6.5	µs
Supply Current		—	35	—	µA

Notes:
1. Represents one standard deviation from the mean.
2. The temperature sensor settling time, resulting from an ADC mux change or enabling of the temperature sensor, varies with the voltage of the previously sampled channel and can be up to 6 µs if the previously sampled channel voltage was greater than 3 V. To minimize the temperature sensor settling time, the ADC mux can be momentarily set to ground before being set to the temperature sensor output. This ensures that the temperature sensor output will settle in 3 µs or less.

5.2.5. Gain Setting

The ADC has gain settings of 1x and 0.5x. In 1x mode, the full scale reading of the ADC is determined directly by V_{REF}. In 0.5x mode, the full-scale reading of the ADC occurs when the input voltage is V_{REF} x 2. The 0.5x gain setting can be useful to obtain a higher input Voltage range when using a small V_{REF} voltage, or to measure input voltages that are between V_{REF} and V_{DD}. Gain settings for the ADC are controlled by the AMP0GN bit in register ADC0CF.

5.3. 8-Bit Mode

Setting the ADC08BE bit in register ADC0CF to 1 will put the ADC in 8-bit mode.In 8-bit mode, only the 8 MSBs of data are converted, allowing the conversion to be completed in two fewer SAR clock cycles than a 10-bit conversion. This can result in an overall lower power consumption since the system can spend more time in a low power mode. The two LSBs of a conversion are always 00 in this mode, and the ADC0L register will always read back 0x00.

5.4. 12-Bit Mode (C8051F912/02 Only)

C8051F912/02 devices have an enhanced SAR converter that provides 12-bit resolution while retaining the 10- and 8-bit operating modes of the other devices in the family. When configured for 12-bit conversions, the ADC performs four 10-bit conversions using four different reference voltages and combines the results into a single 12-bit value. Unlike simple averaging techniques, this method provides true 12-bit resolution of AC or DC input signals without depending on noise to provide dithering. The converter also employs a hardware Dynamic Element Matching algorithm that reconfigures the largest elements of the internal DAC for each of the four 10-bit conversions to cancel the any matching errors, enabling the converter to achieve 12-bit linearity performance to go along with its 12-bit resolution. For best performance, the Low Power Oscillator should be selected as the system clock source while taking 12-bit ADC measurements.

The 12-bit mode is enabled by setting the AD012BE bit (ADC0AC.7) to logic 1 and configuring Burst Mode for four conversions as described in Section 5.2.3. The conversion can be initiated using any of the methods described in Section 5.2.1, and the 12-bit result will appear in the ADC0H and ADC0L registers. Since the 12-bit result is formed from a combination of four 10-bit results, the maximum output value is 4 x (1023) = 4092, rather than the max value of (2^12 – 1) = 4095 that is produced by a traditional 12-bit converter. To further increase resolution, the burst mode repeat value may be configured to any multiple of four conversions. For example, if a repeat value of 16 is selected, the ADC0 output will be a 14-bit number (sum of four 12-bit numbers) with 13 effective bits of resolution.

5.5. Low Power Mode (C8051F912/902 only)

The C8051F912/02 SAR converter provides a low power mode that allows a significant reduction in operating current when operating at low SAR clock frequencies. Low power mode is enabled by setting the AD0LPM bit (ADC0PWR.7) to 1. In general, low power mode is recommended when operating with SAR conversion clock frequency at 4 MHz or less. See the Electrical Characteristics chapter for details on power consumption and the maximum clock frequencies allowed in each mode. Setting the Low Power Mode bit reduces the bias currents in both the SAR converter and in the High-Speed Voltage Reference. describes the various modes of the ADC.

SFR Definition 5.2. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD0SC[4:0]					AD08BE	AD0TM	AMP0GN
Type	R/W					R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	0

SFR Page = 0x0; SFR Address = 0xBC

Bit	Name	Function
7:3	AD0SC[4:0]	**ADC0 SAR Conversion Clock Divider.** SAR Conversion clock is derived from FCLK by the following equation, where *AD0SC* refers to the 5-bit value held in bits AD0SC[4:0]. SAR Conversion clock requirements are given in Table 4.10. BURSTEN = 0: FCLK is the current system clock. BURSTEN = 1: FCLK is the 20 MHz low power oscillator, independent of the system clock. $AD0SC = \frac{FCLK}{CLK_{SAR}} - 1$ * *Round the result up. or $CLK_{SAR} = \frac{FCLK}{AD0SC + 1}$
2	AD08BE	**ADC0 8-Bit Mode Enable.** 0: ADC0 operates in 10-bit mode (normal operation). 1: ADC0 operates in 8-bit mode.
1	AD0TM	**ADC0 Track Mode.** Selects between Normal or Delayed Tracking Modes. 0: Normal Track Mode: When ADC0 is enabled, conversion begins immediately following the start-of-conversion signal. 1: Delayed Track Mode: When ADC0 is enabled, conversion begins 3 SAR clock cycles following the start-of-conversion signal. The ADC is allowed to track during this time.
0	AMP0GN	**ADC0 Gain Control.** 0: The on-chip PGA gain is 0.5. 1: The on-chip PGA gain is 1.

SFR Definition 5.10. ADC0LTH: ADC0 Less-Than High Byte

Bit	7	6	5	4	3	2	1	0
Name	AD0LT[15:8]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC6

Bit	Name	Function
7:0	AD0LT[15:8]	**ADC0 Less-Than High Byte.** Most Significant Byte of the 16-bit Less-Than window compare register.

SFR Definition 5.11. ADC0LTL: ADC0 Less-Than Low Byte

Bit	7	6	5	4	3	2	1	0
Name	AD0LT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC5

Bit	Name	Function
7:0	AD0LT[7:0]	**ADC0 Less-Than Low Byte.** Least Significant Byte of the 16-bit Less-Than window compare register.
Note: In 8-bit mode, this register should be set to 0x00.		

5.6.1. Window Detector In Single-Ended Mode

Figure 5.5 shows two example window comparisons for right-justified data, with ADC0LTH:ADC0LTL = 0x0080 (128d) and ADC0GTH:ADC0GTL = 0x0040 (64d). The input voltage can range from 0 to VREF x (1023/1024) with respect to GND, and is represented by a 10-bit unsigned integer value. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0040 < ADC0H:ADC0L < 0x0080). In the right example, and AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0040 or ADC0H:ADC0L > 0x0080). Figure 5.6 shows an example using left-justified data with the same comparison values.

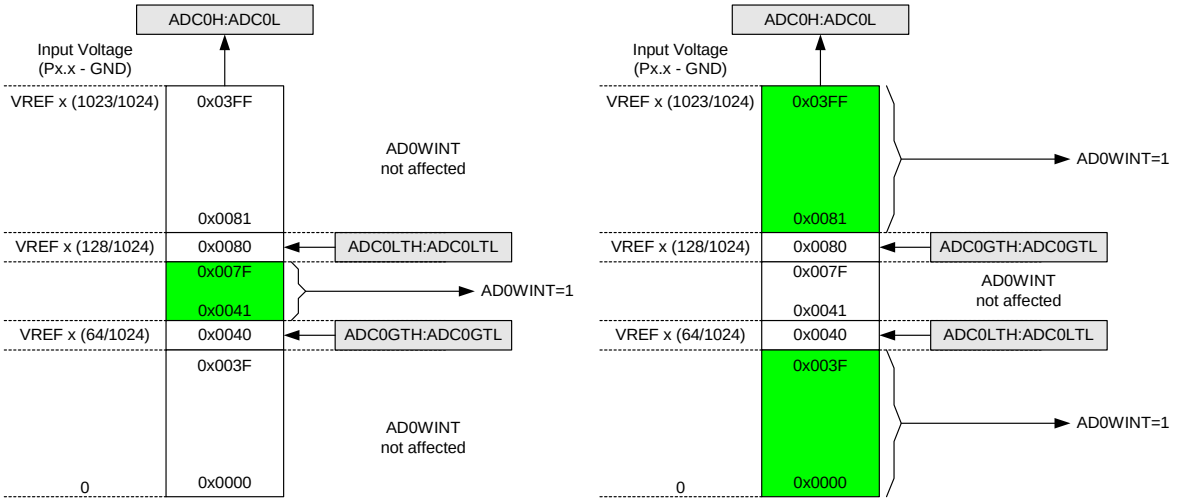


Figure 5.5. ADC Window Compare Example: Right-Justified Single-Ended Data

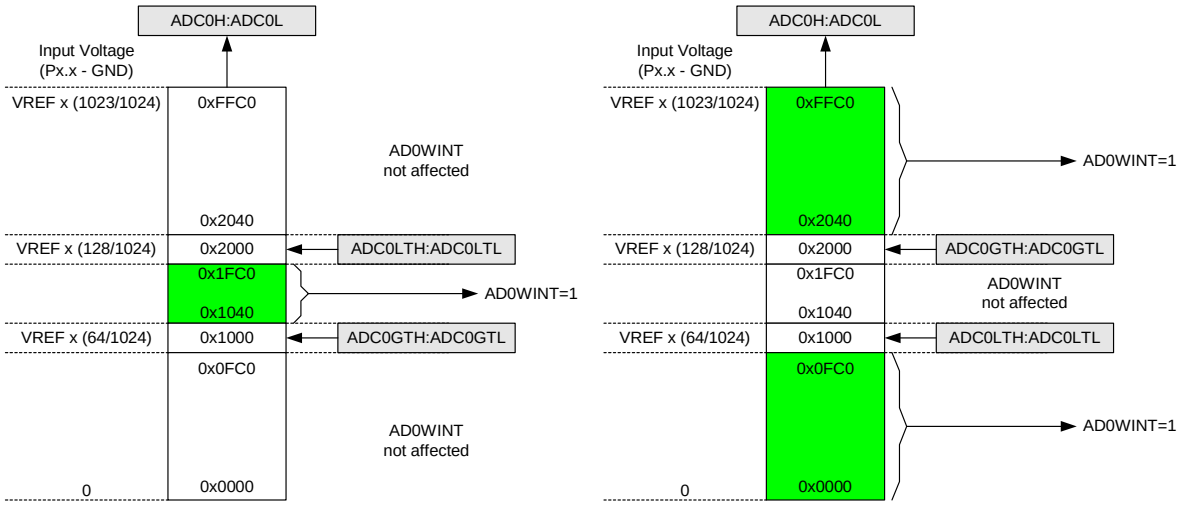


Figure 5.6. ADC Window Compare Example: Left-Justified Single-Ended Data

5.6.2. ADC0 Specifications

See “4. Electrical Characteristics” on page 36 for a detailed listing of ADC0 specifications.

6. Programmable Current Reference (IREF0)

C8051F91x-C8051F90x devices include an on-chip programmable current reference (source or sink) with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63 µA (1 µA steps) and the maximum current output in High Current Mode is 504 µA (8 µA steps).

The current source/sink is controlled though the IREF0CN special function register. It is enabled by setting the desired output current to a non-zero value. It is disabled by writing 0x00 to IREF0CN. The port I/O pin associated with ISRC0 should be configured as an analog input and skipped in the Crossbar. See Section "21. Port Input/Output" on page 205 for more details.

SFR Definition 6.1. IREF0CN: Current Reference Control

Bit	7	6	5	4	3	2	1	0
Name	SINK	MODE	IREF0DAT					
Type	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xB9

Bit	Name	Function
7	SINK	**IREF0 Current Sink Enable.** Selects if IREF0 is a current source or a current sink. 0: IREF0 is a current source. 1: IREF0 is a current sink.
6	MDSEL	**IREF0 Output Mode Select.** Selects Low Power or High Current Mode. 0: Low Power Mode is selected (step size = 1 µA). 1: High Current Mode is selected (step size = 8 µA).
5:0	IREF0DAT[5:0]	**IREF0 Data Word.** Specifies the number of steps required to achieve the desired output current. Output current = direction x step size x IREF0DAT. IREF0 is in a low power state when IREF0DAT is set to 0x00.

6.1. PWM Enhanced Mode

On 'F912 and 'F902 devices, the precision of the current reference can be increased by fine tuning the IREF0 output using a PWM signal generated by the PCA. This mode allows the IREF0DAT bits to perform a course adjustment on the IREF0 output. Any available PCA channel can perform a fine adjustment on the IREF0 output. When enabled (PWMEN = 1), the CEX signal selected using the PWMSS bit field is internally routed to IREF0 to control the on time of a current source having the weight of 2 LSBs. With the two least significant bits of IREF0DAT set to 00b, applying a 100% duty cycle on the CEX signal will be equivalent to setting the two LSBs of IREF0DAT to 10b. PWM enhanced mode is enabled and setup using the IREF0CF register.

SFR Definition 7.3. CPT1CN: Comparator 1 Control

Bit	7	6	5	4	3	2	1	0
Name	CP1EN	CP1OUT	CP1RIF	CP1FIF	CP1HYP[1:0]		CP1HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0x9A

Bit	Name	Function
7	CP1EN	**Comparator1 Enable Bit.** 0: Comparator1 Disabled. 1: Comparator1 Enabled.
6	CP1OUT	**Comparator1 Output State Flag.** 0: Voltage on CP1+ < CP1–. 1: Voltage on CP1+ > CP1–.
5	CP1RIF	**Comparator1 Rising-Edge Flag. Must be cleared by software.** 0: No Comparator1 Rising Edge has occurred since this flag was last cleared. 1: Comparator1 Rising Edge has occurred.
4	CP1FIF	**Comparator1 Falling-Edge Flag. Must be cleared by software.** 0: No Comparator1 Falling-Edge has occurred since this flag was last cleared. 1: Comparator1 Falling-Edge has occurred.
3:2	CP1HYP[1:0]	**Comparator1 Positive Hysteresis Control Bits.** 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = Hysteresis 1. 10: Positive Hysteresis = Hysteresis 2. 11: Positive Hysteresis = Hysteresis 3 (Maximum).
1:0	CP1HYN[1:0]	**Comparator1 Negative Hysteresis Control Bits.** 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = Hysteresis 1. 10: Negative Hysteresis = Hysteresis 2. 11: Negative Hysteresis = Hysteresis 3 (Maximum).

SFR Definition 7.6. CPT1MX: Comparator1 Input Channel Select

Bit	7	6	5	4	3	2	1	0
Name	CMX1N[3:0]				CMX1P[3:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0x9E

Bit	Name	Function			
7:4	CMX1N	**Comparator1 Negative Input Selection.** Selects the negative input channel for Comparator1.			
		0000:	P0.1	1000:	Reserved
		0001:	P0.3	1001:	Reserved
		0010:	P0.5	1010:	Reserved
		0011:	P0.7	1011:	Reserved
		0100:	P1.1	1100:	Capacitive Touch Sense Compare
		0101:	P1.3	1101:	VDD/DC+ divided by 2
		0110:	P1.5	1110:	Digital Supply Voltage
		0111:	Reserved	1111:	Ground
3:0	CMX1P	**Comparator1 Positive Input Selection.** Selects the positive input channel for Comparator1.			
		0000:	P0.0	1000:	Reserved
		0001:	P0.2	1001:	Reserved
		0010:	P0.4	1010:	Reserved
		0011:	P0.6	1011:	Reserved
		0100:	P1.0	1100:	Capacitive Touch Sense Compare
		0101:	P1.2	1101:	VDD/DC+ divided by 2
		0110:	P1.4	1110:	VBAT Supply Voltage
		0111:	P1.6	1111:	VDD/DC+ Supply Voltage

12. Interrupt Handler

The C8051F91x-C8051F90x microcontroller family includes an extended interrupt system supporting multiple interrupt sources and two priority levels. The allocation of interrupt sources between on-chip peripherals and external input pins varies according to the specific version of the device. Refer to Table 12.1, “Interrupt Summary,” on page 122 for a detailed listing of all interrupt sources supported by the device. Refer to the data sheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

Each interrupt source has one or more associated interrupt-pending flag(s) located in an SFR or an indirect register. When a peripheral or external source meets a valid interrupt condition, the associated interrupt-pending flag is set to logic 1. If both global interrupts and the specific interrupt source is enabled, a CPU interrupt request is generated when the interrupt-pending flag is set.

As soon as execution of the current instruction is complete, the CPU generates an LCALL to a predetermined address to begin execution of an interrupt service routine (ISR). Each ISR must end with an RETI instruction, which returns program execution to the next instruction that would have been executed if the interrupt request had not occurred. If interrupts are not enabled, the interrupt-pending flag is ignored by the hardware and program execution continues as normal. (The interrupt-pending flag is set to logic 1 regardless of the interrupt's enable/disable state.)

Some interrupt-pending flags are automatically cleared by hardware when the CPU vectors to the ISR. However, most are not cleared by the hardware and must be cleared by software before returning from the ISR. If an interrupt-pending flag remains set after the CPU completes the return-from-interrupt (RETI) instruction, a new interrupt request will be generated immediately and the CPU will re-enter the ISR after the completion of the next instruction.

12.1. Enabling Interrupt Sources

Each interrupt source can be individually enabled or disabled through the use of an associated interrupt enable bit in the Interrupt Enable and Extended Interrupt Enable SFRs. However, interrupts must first be globally enabled by setting the EA bit (IE.7) to logic 1 before the individual interrupt enables are recognized. Setting the EA bit to logic 0 disables all interrupt sources regardless of the individual interrupt-enable settings. Note that interrupts which occur when the EA bit is set to logic 0 will be held in a pending state, and will not be serviced until the EA bit is set back to logic 1.

12.2. MCU Interrupt Sources and Vectors

The CPU services interrupts by generating an LCALL to a predetermined address (the interrupt vector address) to begin execution of an interrupt service routine (ISR). The interrupt vector addresses associated with each interrupt source are listed in Table 12.1 on page 122. Software should ensure that the interrupt vector for each enabled interrupt source contains a valid interrupt service routine.

Software can simulate an interrupt by setting any interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag.

16.5. Minimizing Power Supply Noise

To minimize noise on the power supply lines, the GND and GND/DC- pins should be kept separate, as shown in Figure 16.2; one or the other should be connected to the pc board ground plane. For applications in which the dc-dc converter is used only to power internal circuits, the GND pin is normally connected to the board ground.

The large decoupling capacitors in the input and output circuits ensure that each supply is relatively quiet with respect to its own ground. However, connecting a circuit element "diagonally" (e.g. connecting an external chip between VDD/DC+ and GND, or between VBAT and GND/DC-) can result in high supply noise across that circuit element. For applications in which the dc-dc converter is used to power external analog circuitry, it is recommended to connect the GND/DC– pin to the board ground and connect the battery's negative terminal to the GND pin only, which is not connected to board ground.

To accommodate situations in which ADC0 is sampling a signal that is referenced to one of the external grounds, we recommend using the Analog Ground Reference (P0.1/AGND) option described in Section 5.12. This option prevents any voltage differences between the internal chip ground and the external grounds from modulating the ADC input signal. If this option is enabled, the P0.1 pin should be tied to the ground reference of the external analog input signal. When using the ADC with the dc-dc converter, we also recommend enabling the SYNC bit in the DC0CN register to minimize interference.

These general guidelines provide the best performance in most applications, though some situations may benefit from experimentation to eliminate any residual noise issues. Examples might include tying the grounds together, using additional low-inductance decoupling caps in parallel with the recommended ones, investigating the effects of different dc-dc converter settings, etc.

16.6. Selecting the Optimum Switch Size

The dc-dc converter has two built-in switches (the diode bypass switch and duty cycle control switch). To maximize efficiency, one of two switch sizes may be selected. The large switches are ideal for carrying high currents and the small switches are ideal for low current applications. The ideal switchover point to switch from the small switches to the large switches varies with the programmed output voltage. At an output voltage of 2 V, the ideal switchover point is at approximately 4 mA total output current. At an output voltage of 3 V, the ideal switchover point is at approximately 8 mA total output current.

16.7. DC-DC Converter Clocking Options

The dc-dc converter may be clocked from its internal oscillator, or from any system clock source, selectable by the CLKSEL bit (DC0CF.0). The dc-dc converter internal oscillator frequency is approximately 2.4 MHz. For a more accurate clock source, the system clock, or a divided version of the system clock may be used as the dc-dc clock source. The dc-dc converter has a built in clock divider (configured using DC0CF[6:5]) which allows any system clock frequency over 1.6 MHz to generate a valid clock in the range of 1.6 to 3.2 MHz.

When the precision internal oscillator is selected as the system clock source, the OSCICL register may be used to fine tune the oscillator frequency and the dc-dc converter clock. The oscillator frequency should only be decreased since it is factory calibrated at its maximum frequency. The minimum frequency which can be reached by the oscillator after taking into account process variations is approximately 16 MHz. The system clock routed to the dc-dc converter clock divider also may be inverted by setting the CLKINV bit (DC0CF.3) to logic 1. These options can be used to minimize interference in noise sensitive applications.

16.8. DC-DC Converter Behavior in Sleep Mode

When the C8051F91x-C8051F90x devices are placed in Sleep mode, the dc-dc converter is disabled, and the VDD/DC+ output is internally connected to VBAT by default. This behavior ensures that the GPIO pins are powered from a low-impedance source during sleep mode. If the GPIO pins are not used as inputs or

SFR Definition 19.4. OSCXCN: External Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	XCLKVLD	XOSCMD[2:0]			Reserved	XFCN[2:0]		
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xB1

Bit	Name	Function
7	XCLKVLD	**External Oscillator Valid Flag.** Provides External Oscillator status and is valid at all times for all modes of operation except External CMOS Clock Mode and External CMOS Clock Mode with divide by 2. In these modes, XCLKVLD always returns 0. 0: External Oscillator is unused or not yet stable. 1: External Oscillator is running and stable.
6:4	XOSCMD	**External Oscillator Mode Bits.** Configures the external oscillator circuit to the selected mode. 00x: External Oscillator circuit disabled. 010: External CMOS Clock Mode. 011: External CMOS Clock Mode with divide by 2 stage. 100: RC Oscillator Mode. 101: Capacitor Oscillator Mode. 110: Crystal Oscillator Mode. 111: Crystal Oscillator Mode with divide by 2 stage.
3	Reserved	**Reserved.** Read = 0b. Must Write 0b.
2:0	XFCN	**External Oscillator Frequency Control Bits.** Controls the external oscillator bias current. 000-111: See Table 19.1 on page 181 (Crystal Mode) or Table 19.2 on page 182 (RC or C Mode) for recommended settings.

Table 20.3. SmaRTClock Bias Settings

Mode	Setting	Power Consumption
Crystal	Bias Double Off, AGC On	Lowest 600 nA
	Bias Double Off, AGC Off	Low 800 nA
	Bias Double On, AGC On	High
	Bias Double On, AGC Off	Highest
Self-Oscillate	Bias Double Off	Low
	Bias Double On	High

22.4.1. SMBus Configuration Register

The SMBus Configuration register (SMB0CF) is used to enable the SMBus Master and/or Slave modes, select the SMBus clock source, and select the SMBus timing and timeout options. When the ENSMB bit is set, the SMBus is enabled for all master and slave events. Slave events may be disabled by setting the INH bit. With slave events inhibited, the SMBus interface will still monitor the SCL and SDA pins; however, the interface will NACK all received addresses and will not generate any slave interrupts. When the INH bit is set, all slave events will be inhibited following the next START (interrupts will continue for the duration of the current transfer).

Table 22.1. SMBus Clock Source Selection

SMBCS1	SMBCS0	SMBus Clock Source
0	0	Timer 0 Overflow
0	1	Timer 1 Overflow
1	0	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow

The SMBCS1–0 bits select the SMBus clock source, which is used only when operating as a master or when the Free Timeout detection is enabled. When operating as a master, overflows from the selected source determine the absolute minimum SCL low and high times as defined in Equation 22.1. Note that the selected clock source may be shared by other peripherals so long as the timer is left running at all times. For example, Timer 1 overflows may generate the SMBus and UART baud rates simultaneously. Timer configuration is covered in Section “25. Timers” on page 270.

$$T_{HighMin} = T_{LowMin} = \frac{1}{f_{ClockSourceOverflow}}$$

Equation 22.1. Minimum SCL High and Low Times

The selected clock source should be configured to establish the minimum SCL High and Low times as per Equation 22.1. When the interface is operating as a master (and SCL is not driven or extended by any other devices on the bus), the typical SMBus bit rate is approximated by Equation 22.2.

$$BitRate = \frac{f_{ClockSourceOverflow}}{3}$$

Equation 22.2. Typical SMBus Bit Rate

Figure 22.4 shows the typical SCL generation described by Equation 22.2. Notice that T_{HIGH} is typically twice as large as T_{LOW}. The actual SCL output may vary due to other devices on the bus (SCL may be extended low by slower slave devices, or driven low by contending master devices). The bit rate when operating as a master will never exceed the limits defined by equation Equation 22.1.

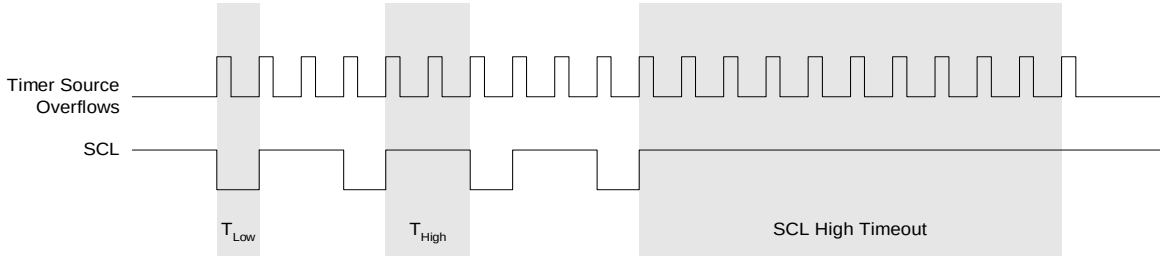


Figure 22.4. Typical SMBus SCL Generation

Table 22.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	-
Slave Receiver	0010	1	0	X	A slave address + R/W was received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	-
		1	1	X	Lost arbitration as master; slave address + R/W received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	-
						Reschedule failed transfer; NACK received address.	1	0	0	1110
	0001	0	0	X	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X	-
		1	1	X	Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0	-
	0000	1	0	X	A slave byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000
						NACK received byte.	0	0	0	-
Bus Error Condition	0010	0	1	X	Lost arbitration while attempting a repeated START.	Abort failed transfer.	0	0	X	-
						Reschedule failed transfer.	1	0	X	1110
	0001	0	1	X	Lost arbitration due to a detected STOP.	Abort failed transfer.	0	0	X	-
						Reschedule failed transfer.	1	0	X	1110
	0000	1	1	X	Lost arbitration while transmitting a data byte as master.	Abort failed transfer.	0	0	0	-
						Reschedule failed transfer.	1	0	0	1110

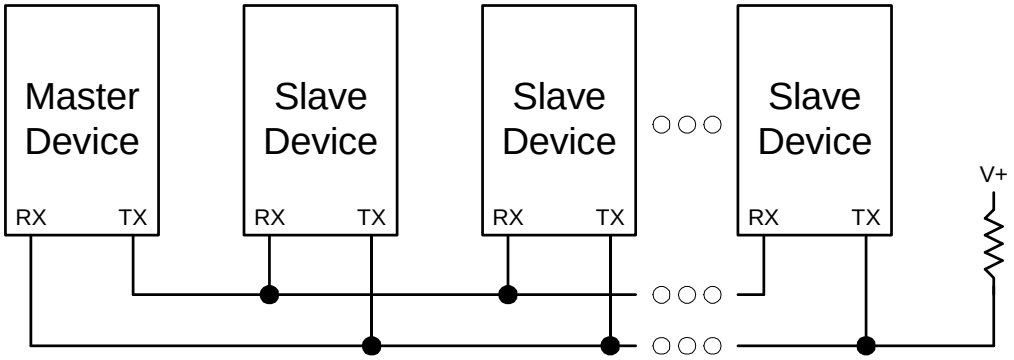


Figure 23.6. UART Multi-Processor Mode Interconnect Diagram

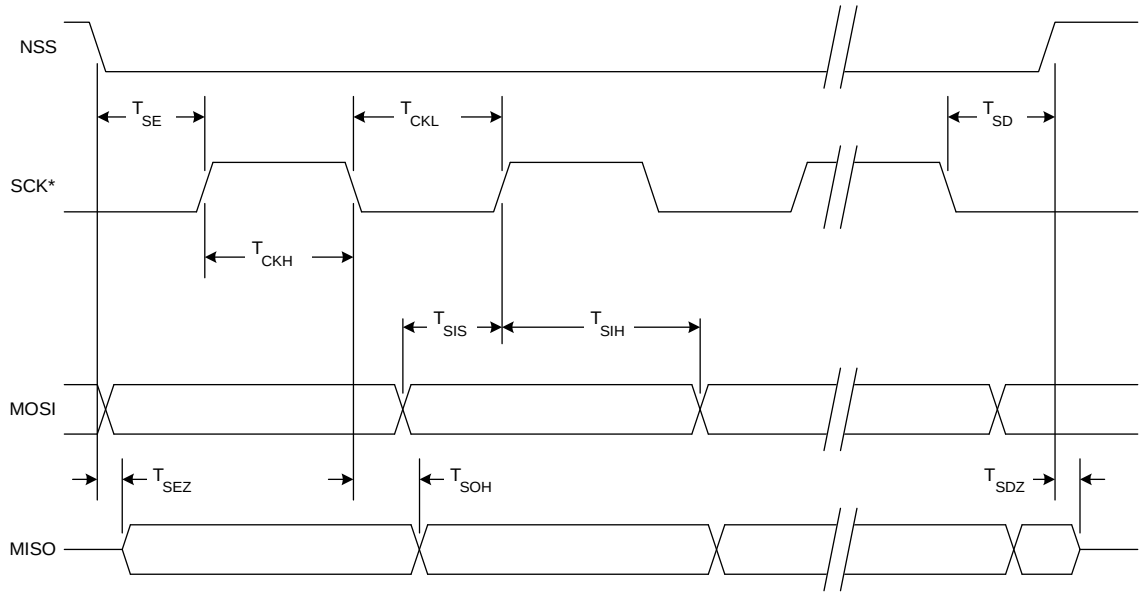
SFR Definition 24.1. SPInCFG: SPI Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Addresses: SPI0CFG = 0xA1, SPI1CFG = 0x84
SFR Pages: SPI0CFG = 0x0, SPI1CFG = 0x0

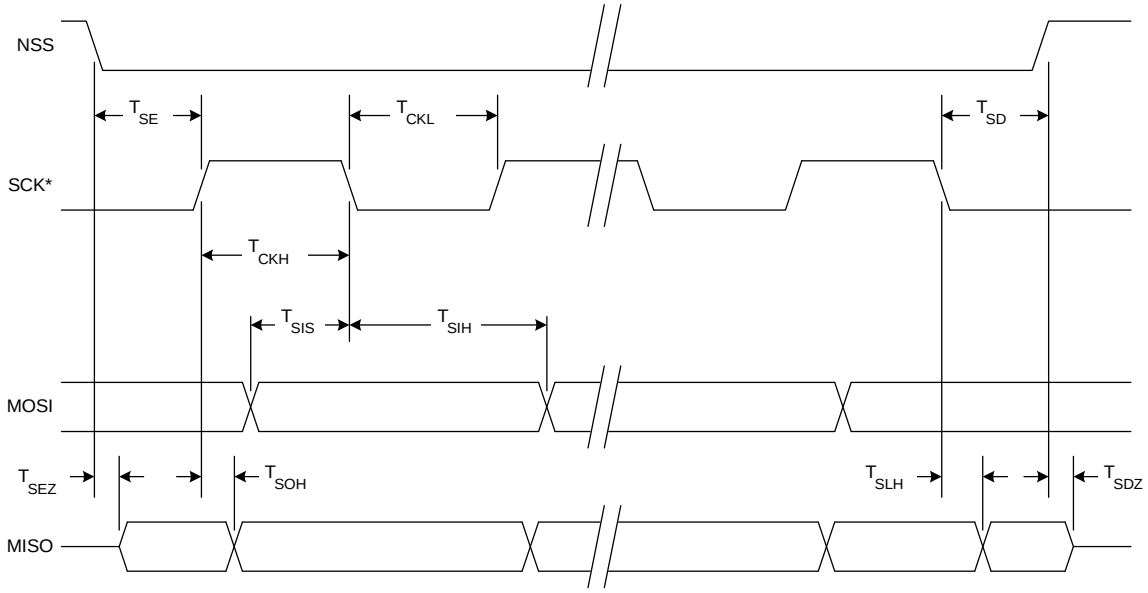
Bit	Name	Function
7	SPIBSY	**SPI Busy.** This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	**Master Mode Enable.** 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	**SPI Clock Phase.** 0: Data centered on first edge of SCK period.* 1: Data centered on second edge of SCK period.*
4	CKPOL	**SPI Clock Polarity.** 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	**Slave Selected Flag.** Set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	**NSS Instantaneous Pin Input.** This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	**Shift Register Empty (valid in slave mode only).** Set to logic 1 when data has been transferred in/out of the shift register, and there is no data is available to read from the transmit buffer or write to the receive buffer. Set to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. Note: SRMT = 1 in Master Mode.
0	RXBMT	**Receive Buffer Empty (valid in slave mode only).** Set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. Note: RXBMT = 1 in Master Mode.

***Note:** In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 24.1 for timing parameters.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.10. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.11. SPI Slave Timing (CKPHA = 1)

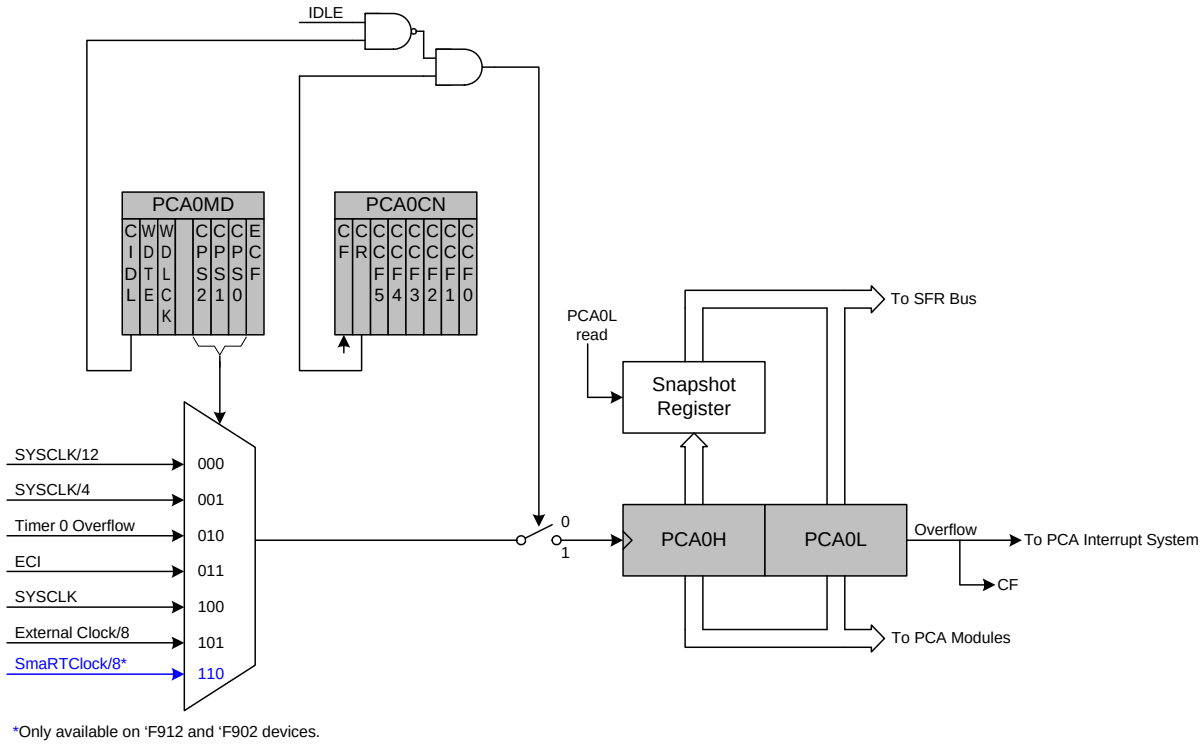


Figure 26.2. PCA Counter/Timer Block Diagram

26.2. PCA0 Interrupt Sources

Figure 26.3 shows a diagram of the PCA interrupt tree. There are eight independent event flags that can be used to generate a PCA0 interrupt. They are: the main PCA counter overflow flag (CF), which is set upon a 16-bit overflow of the PCA0 counter, an intermediate overflow flag (COVF), which can be set on an overflow from the 8th, 9th, 10th, or 11th bit of the PCA0 counter, and the individual flags for each PCA channel (CCF0, CCF1, CCF2, CCF3, CCF4, and CCF5), which are set according to the operation mode of that module. These event flags are always set when the trigger condition occurs. Each of these flags can be individually selected to generate a PCA0 interrupt, using the corresponding interrupt enable flag (ECF for CF, ECOV for COVF, and ECCFn for each CCFn). PCA0 interrupts must be globally enabled before any individual interrupt sources are recognized by the processor. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1.

SFR Definition 26.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD9

Bit	Name	Function
7	CIDL	**PCA Counter/Timer Idle Control.** Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.
6	WDTE	**Watchdog Timer Enable.** If this bit is set, PCA Module 2 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 2 enabled as Watchdog Timer.
5	WDLCK	**Watchdog Timer Lock.** This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.
4	Unused	Read = 0b, Write = don't care.
3:1	CPS[2:0]	**PCA Counter/Timer Pulse Select.** These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) **110: SmaRTClock divided by 8** (synchronized with the system clock and only available on ‘F912 and ‘F902 devices -- this setting is reserved on all other devices) 111: Reserved
0	ECF	**PCA Counter/Timer Overflow Interrupt Enable.** This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.
Note: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.		