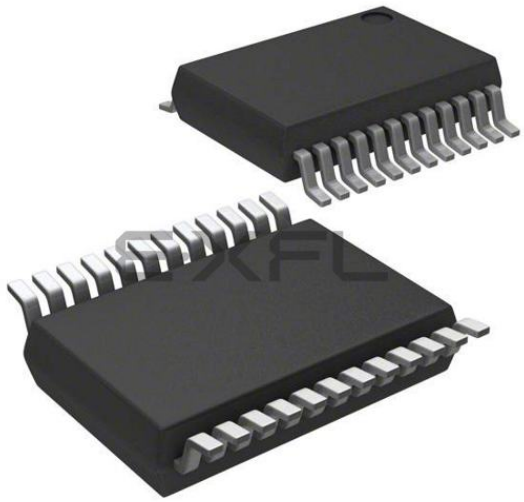

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f912-d-gur

3. Pinout and Package Definitions

Table 3.1. Pin Definitions for the C8051F91x-C8051F90x

Name	Pin Numbers		Type	Description
	'F912-GM 'F902-GM 'F911-GM 'F901-GM	**'F912-GU 'F902-GU 'F911-GU 'F901-GU**		
VBAT	5	8	P In	Battery Supply Voltage. C8051F911/01 devices: Must be 0.9 to 1.8 V in single-cell battery mode and 1.8 to 3.6 V in dual-cell battery mode. C8051F912/02 devices: Must be 0.9 to 3.6 V in single-cell battery mode and 1.8 to 3.6 V in dual-cell battery mode.
V_{DD} / DC+	3	6	P In P Out	Power Supply Voltage. Must be 1.8 to 3.6 V. This supply voltage is not required in low power sleep mode. This voltage must always be $\geq$ VBAT. Positive output of the dc-dc converter. In single-cell battery mode, a 1uF ceramic capacitor is required between DC+ and DC–. This pin can supply power to external devices when operating in single-cell battery mode.
DC– / GND	1	4	P In G	DC-DC converter return current path. In single-cell battery mode, this pin is typically not connected to ground. In dual-cell battery mode, this pin must be connected directly to ground.
GND	2	5	G	Required Ground.
DCEN	4	7	P In G	DC-DC Enable Pin. In single-cell battery mode, this pin must be connected to VBAT through a 0.68 µH inductor. In dual-cell battery mode, this pin must be connected directly to ground.
$\overline{RST}$/ C2CK	6	9	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. A 1 kΩ to 5 kΩ pullup to V_{DD} is recommended. See Section “18. Reset Sources” on page 171 Section for a complete description. Clock signal for the C2 Debug Interface.
P2.7/ C2D	7	10	D I/O D I/O	Port 2.7. This pin can only be used as GPIO. The Crossbar cannot route signals to this pin and it cannot be configured as an analog input. See Port I/O Section for a complete description. Bi-directional data signal for the C2 Debug Interface.

***Note:** Available only on the C8051F912/02.

Table 4.2. Global Electrical Characteristics (Continued)

–40 to +85 °C, 25 MHz system clock unless otherwise specified. See "AN358: Optimizing Low Power Operation of the ‘F9xx" for details on how to achieve the supply current specifications listed in this table.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD} [3, 4, 5, 6]	V_{DD} = 1.8–3.6 V, F = 24.5 MHz (includes precision oscillator current)	—	4.0	5.0	mA
	V_{DD} = 1.8–3.6 V, F = 20 MHz (includes low power oscillator current)	—	3.4	—	mA
	V_{DD} = 1.8 V, F = 1 MHz V_{DD} = 3.6 V, F = 1 MHz (includes external oscillator/GPIO current)	— —	265 305	— —	µA µA
	V_{DD} = 1.8–3.6 V, F = 32.768 kHz (includes SmaRTClock oscillator current)	—	84	—	µA
I_{DD} Frequency Sensitivity[3, 5, 6]	V_{DD} = 1.8–3.6 V, T = 25 °C, F < 14 MHz (Flash oneshot active, see Section 13.6)	—	191	—	µA/MHz
	V_{DD} = 1.8–3.6 V, T = 25 °C, F > 14 MHz (Flash oneshot bypassed, see Section 13.6)	—	102	—	µA/MHz
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
I_{DD} [4, 6, 7]	V_{DD} = 1.8–3.6 V, F = 24.5 MHz (includes precision oscillator current)	—	2.1	3.0	mA
	V_{DD} = 1.8–3.6 V, F = 20 MHz (includes low power oscillator current)	—	1.6	—	mA
	V_{DD} = 1.8 V, F = 1 MHz V_{DD} = 3.6 V, F = 1 MHz (includes external oscillator/GPIO current)	— —	160 185	— —	µA µA
	V_{DD} = 1.8–3.6 V, F = 32.768 kHz (includes SmaRTClock oscillator current)	—	82	—	µA
I_{DD} Frequency Sensitivity[1,6,7]	V_{DD} = 1.8–3.6 V, T = 25 °C	—	79	—	µA/MHz

SFR Definition 5.13. TOFFH: ADC0 Data Word High Byte

Bit	7	6	5	4	3	2	1	0
Name	TOFF[9:2]							
Type	R	R	R	R	R	R	R	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Page = 0xF; SFR Address = 0x86

Bit	Name	Function
7:0	TOFF[9:2]	**Temperature Sensor Offset High Bits.** Most Significant Bits of the 10-bit temperature sensor offset measurement.

SFR Definition 5.14. TOFFL: ADC0 Data Word Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TOFF[1:0]							
Type	R	R						
Reset	Varies	Varies	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0x85

Bit	Name	Function
7:6	TOFF[1:0]	**Temperature Sensor Offset Low Bits.** Least Significant Bits of the 10-bit temperature sensor offset measurement.
5:0	Unused	**Unused.** Read = 0; Write = Don't Care.

10. On-Chip XRAM

The C8051F91x-C8051F90x MCUs include on-chip RAM mapped into the external data memory space (XRAM). The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either the data pointer (DPTR), or with the target address low byte in R0 or R1 and the target address high byte in the External Memory Interface Control Register (EMI0CN, shown in SFR Definition 10.1).

When using the MOVX instruction to access on-chip RAM, no additional initialization is required and the MOVX instruction execution time is as specified in the CIP-51 chapter.

Important Note: MOVX write operations can be configured to target Flash memory, instead of XRAM. See Section “13. Flash Memory” on page 132 for more details. The MOVX instruction accesses XRAM by default.

10.1. Accessing XRAM

The XRAM memory space is accessed using the MOVX instruction. The MOVX instruction has two forms, both of which use an indirect addressing method. The first method uses the Data Pointer, DPTR, a 16-bit register which contains the effective address of the XRAM location to be read from or written to. The second method uses R0 or R1 in combination with the EMI0CN register to generate the effective XRAM address. Examples of both of these methods are given below.

10.1.1. 16-Bit MOVX Example

The 16-bit form of the MOVX instruction accesses the memory location pointed to by the contents of the DPTR register. The following series of instructions reads the value of the byte at address 0x1234 into the accumulator A:

```
MOV    DPTR, #1234h        ; load DPTR with 16-bit address to read (0x1234)
MOVX   A, @DPTR            ; load contents of 0x1234 into accumulator A
```

The above example uses the 16-bit immediate MOV instruction to set the contents of DPTR. Alternately, the DPTR can be accessed through the SFR registers DPH, which contains the upper 8-bits of DPTR, and DPL, which contains the lower 8-bits of DPTR.

10.1.2. 8-Bit MOVX Example

The 8-bit form of the MOVX instruction uses the contents of the EMI0CN SFR to determine the upper 8-bits of the effective address to be accessed and the contents of R0 or R1 to determine the lower 8-bits of the effective address to be accessed. The following series of instructions read the contents of the byte at address 0x1234 into the accumulator A.

```
MOV    EMI0CN, #12h        ; load high byte of address into EMI0CN
MOV    R0, #34h            ; load low byte of address into R0 (or R1)
MOVX   a, @R0              ; load contents of 0x1234 into accumulator A
```

SFR Definition 12.6. EIP2: Extended Interrupt Priority 2

Bit	7	6	5	4	3	2	1	0
Name					PSPI1	PRTC0F	PMAT	PWARN
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xF7

Bit	Name	Function
7:4	Unused	**Unused.** Read = 0000b. Write = Don't care.
3	PSPI1	**Serial Peripheral Interface (SPI1) Interrupt Priority Control.** This bit sets the priority of the SPI1 interrupt. 0: SP1 interrupt set to low priority level. 1: SPI1 interrupt set to high priority level.
2	PRTC0F	**SmaRTClock Oscillator Fail Interrupt Priority Control.** This bit sets the priority of the SmaRTClock Alarm interrupt. 0: SmaRTClock Alarm interrupt set to low priority level. 1: SmaRTClock Alarm interrupt set to high priority level.
1	PMAT	**Port Match Interrupt Priority Control.** This bit sets the priority of the Port Match Event interrupt. 0: Port Match interrupt set to low priority level. 1: Port Match interrupt set to high priority level.
0	PWARN	**Supply Monitor Early Warning Interrupt Priority Control.** This bit sets the priority of the VDD/DC+ Supply Monitor Early Warning interrupt. 0: Supply Monitor Early Warning interrupt set to low priority level. 1: Supply Monitor Early Warning interrupt set to high priority level.

SFR Definition 14.3. PCON: Power Management Control Register

Bit	7	6	5	4	3	2	1	0
Name	GF[5:0]						STOP	IDLE
Type	R/W						W	W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0x87

Bit	Name	Description	Write	Read
7:2	GF[5:0]	**General Purpose Flags**	Sets the logic value.	Returns the logic value.
1	STOP	**Stop Mode Select**	Writing 1 places the device in Stop Mode.	N/A
0	IDLE	**Idle Mode Select**	Writing 1 places the device in Idle Mode.	N/A

14.8. Power Management Specifications

See Table 4.5 on page 53 for detailed Power Management Specifications.

16.4. Enabling the DC-DC Converter

On power-on reset, the state of the DCEN pin is sampled to determine if the device will power up in one-cell or two-cell mode. In two-cell mode, the dc-dc converter always remains disabled. In one-cell mode, the dc-dc converter remains disabled in Sleep Mode, and enabled in all other power modes. See Section “14. Power Management” on page 143 for complete details on available power modes.

The dc-dc converter is enabled (one-cell mode) in hardware by placing a 0.68 µH inductor between DCEN and VBAT. The dc-dc converter is disabled (two-cell mode) by shorting DCEN directly to GND. The DCEN pin should never be left floating. The device can only switch between one-cell and two-cell mode during a power-on reset. See Section “18. Reset Sources” on page 171 for more information regarding reset behavior.

Figure 16.2 shows the two dc-dc converter configuration options.

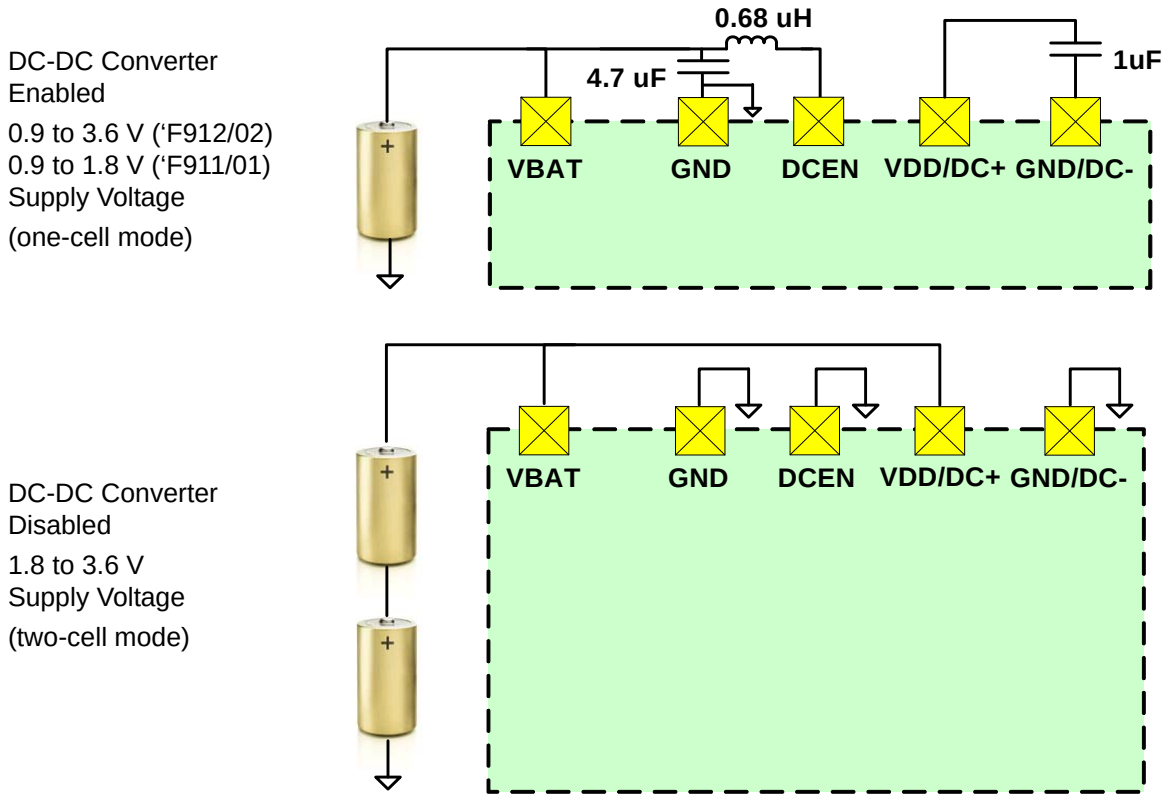

Figure 16.2. DC-DC Converter Configuration Options

When the dc-dc converter “Enabled” configuration (one-cell mode) is chosen, the following guidelines apply:

- In most cases, the GND/DC– pin should not be externally connected to GND.
- The 0.68 µH inductor should be placed as close as possible to the DCEN pin for maximum efficiency.
- The 4.7 µF capacitor should be placed as close as possible to the inductor.
- The current loop including GND, the 4.7 µF capacitor, the 0.68 µH inductor and the DCEN pin should be made as short as possible.
- The PCB traces connecting VDD/DC+ to the output capacitor and the output capacitor to GND/DC– should be as short and as thick as possible in order to minimize parasitic inductance.

17. Voltage Regulator (VREG0)

C8051F91x-C8051F90x devices include an internal voltage regulator (VREG0) to regulate the internal core supply to 1.8 V from a VDD/DC+ supply of 1.8 to 3.6 V. Electrical characteristics for the on-chip regulator are specified in the Electrical Specifications chapter.

The REG0CN register allows the Precision Oscillator Bias to be disabled, reducing supply current in all non-Sleep power modes. This bias should only be disabled when the precision oscillator is not being used.

The internal regulator (VREG0) is disabled when the device enters Sleep Mode and remains enabled when the device enters Suspend Mode. See Section “14. Power Management” on page 143 for complete details about low power modes.

SFR Definition 17.1. REG0CN: Voltage Regulator Control

Bit	7	6	5	4	3	2	1	0
Name		Reserved	Reserved	OSCBIAS				Reserved
Type	R	R/W	R/W	R/W	R	R	R	R/W
Reset	0	0	0	1	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC9

Bit	Name	Function
7	Unused	**Unused.** Read = 0b. Write = Don’t care.
6	Reserved	**Reserved.** Read = 0b. Must Write 0b.
5	Reserved	**Reserved.** Read = 0b. Must Write 0b.
4	OSCBIAS	**Precision Oscillator Bias.** When set to 1, the bias used by the precision oscillator is forced on. If the precision oscillator is not being used, this bit may be cleared to 0 to save approximately 80 µA of supply current in all non-Sleep power modes. If disabled then re-enabled, the precision oscillator bias requires 4 µs of settling time.
3:1	Unused	**Unused.** Read = 000b. Write = Don’t care.
0	Reserved	**Reserved.** Read = 0b. Must Write 0b.

17.1. Voltage Regulator Electrical Specifications

See Table 4.15 on page 59 for detailed Voltage Regulator Electrical Specifications.

18. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled

All SFRs are reset to the predefined values noted in the SFR descriptions. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. Since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For V_{DD} Monitor and power-on resets, the $\overline{RST}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. Refer to Section “19. Clocking Sources” on page 179 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source (Section “26.4. Watchdog Timer Mode” on page 304 details the use of the Watchdog Timer). Program execution begins at location 0x0000.

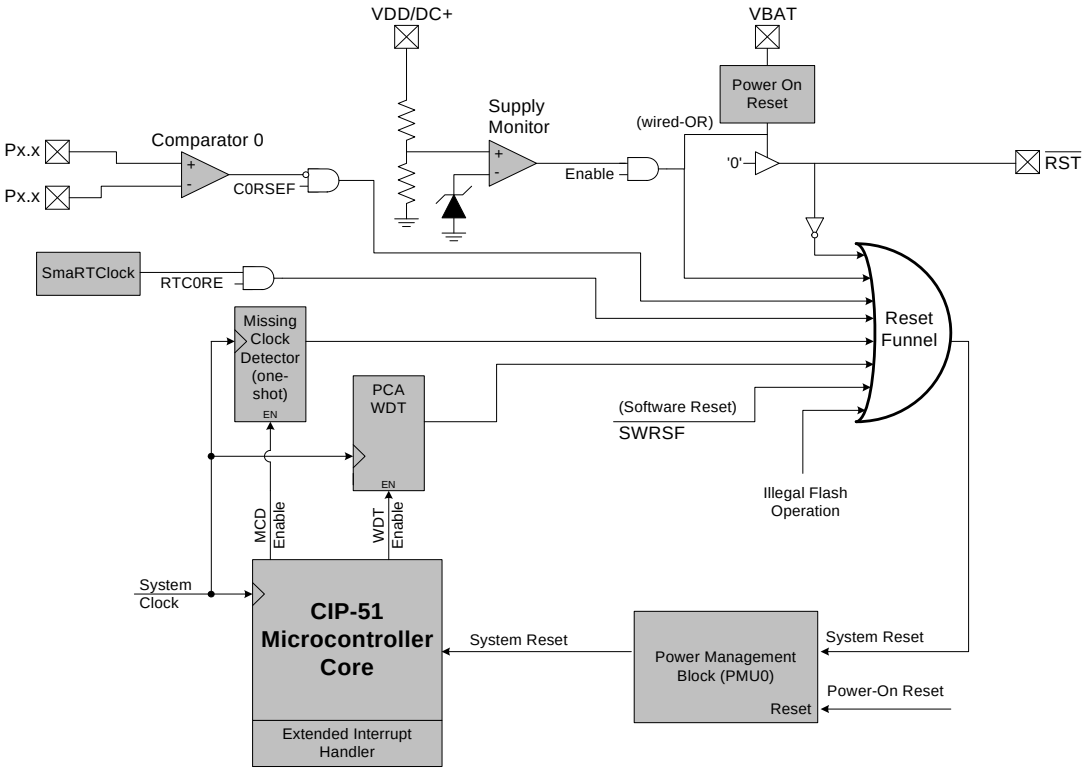

Figure 18.1. Reset Sources

Internal Register Definition 20.6. RTC0XCF: SmaRTClock Oscillator Configuration

Bit	7	6	5	4	3	2	1	0
Name	AUTOSTP	LOADRDY			LOADCAP			
Type	R/W	R	R	R	R/W			
Reset	0	0	0	0	Varies	Varies	Varies	Varies

SmaRTClock Address = 0x06

Bit	Name	Function
7	AUTOSTP	**Automatic Load Capacitance Stepping Enable.** Enables/disables automatic load capacitance stepping. 0: Load capacitance stepping disabled. 1: Load capacitance stepping enabled.
6	LOADRDY	**Load Capacitance Ready Indicator.** Set by hardware when the load capacitance matches the programmed value. 0: Load capacitance is currently stepping. 1: Load capacitance has reached it programmed value.
5:4	Unused	**Unused.** Read = 00b; Write = Don't Care.
3:0	LOADCAP	**Load Capacitance Programmed Value.** Holds the user's desired value of the load capacitance. See Table 20.2 on page 196.

Internal Register Definition 20.7. RTC0PIN: SmaRTClock Pin Configuration

Bit	7	6	5	4	3	2	1	0
Name	RTC0PIN							
Type	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SmaRTClock Address = 0x07

Bit	Name	Function
7	RTC0PIN	**SmaRTClock Pin Configuration.** 0: XTAL3 and XTAL4 in their normal configuration. 1: XTAL3 and XTAL4 internally shorted for use with Self Oscillate Mode.
6:0	Reserved	**Reserved.** Read = Varies. Software should not modify the value of these bits. To change the RTC0PIN setting, the entire register contents should be read, modified, then rewritten.

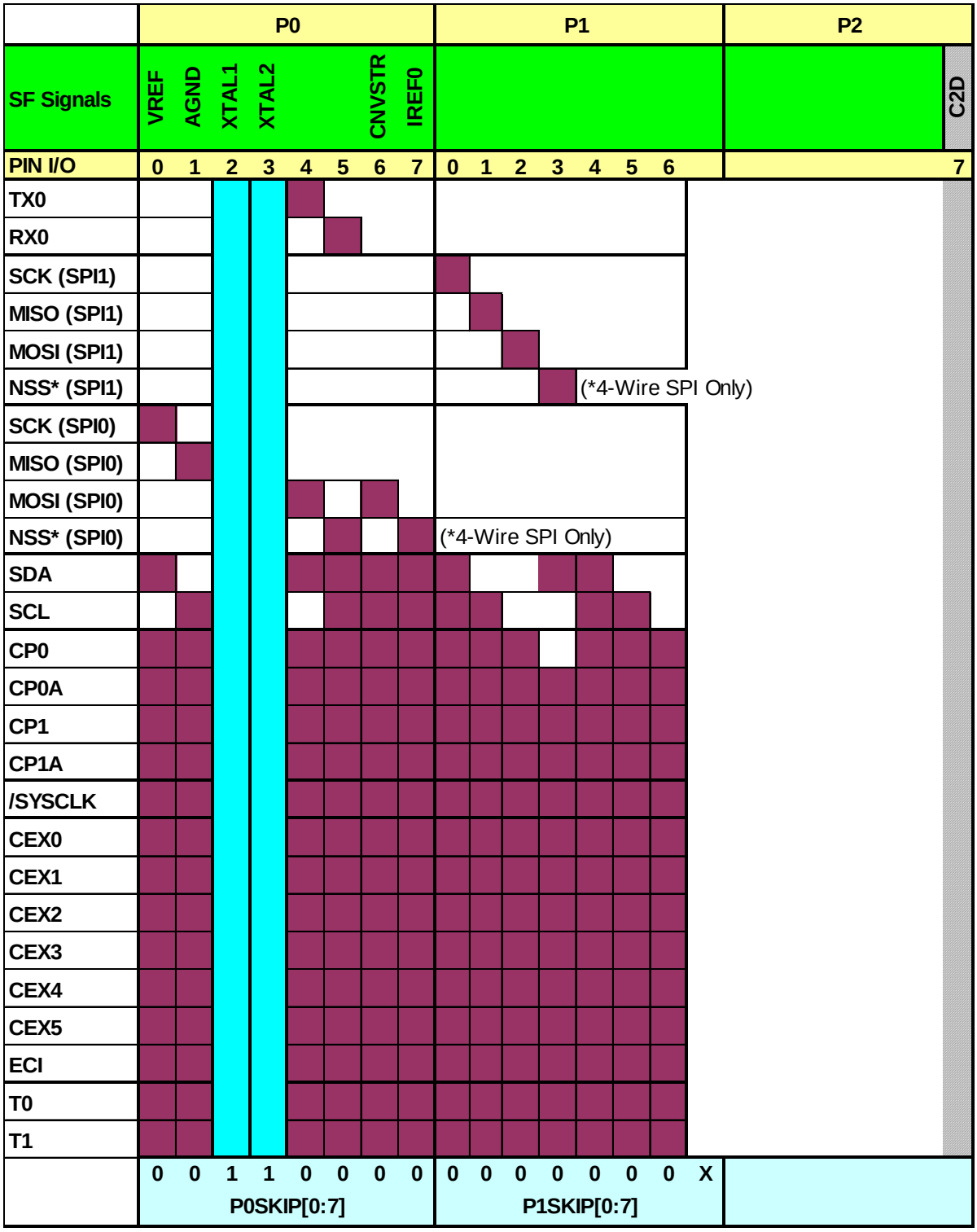

Figure 21.4. Crossbar Priority Decoder with Crystal Pins Skipped

SFR Definition 21.8. P0: Port0

Bit	7	6	5	4	3	2	1	0
Name	P0[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = All Pages; SFR Address = 0x80; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P0[7:0]	**Port 0 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P0.n Port pin is logic LOW. 1: P0.n Port pin is logic HIGH.

SFR Definition 21.9. P0SKIP: Port0 Skip

Bit	7	6	5	4	3	2	1	0
Name	P0SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0xD4

Bit	Name	Function
7:0	P0SKIP[7:0]	**Port 0 Crossbar Skip Enable Bits.** These bits select Port 0 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P0.n pin is not skipped by the Crossbar. 1: Corresponding P0.n pin is skipped by the Crossbar.

SFR Definition 21.17. P1DRV: Port1 Drive Strength

Bit	7	6	5	4	3	2	1	0
Name		P1DRV[6:0]						
Type		R/W						
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xA5

Bit	Name	Function
7	Unused	**Unused.** Read =0b; Write = Don't Care.
6:0	P1DRV[6:0]	**Drive Strength Configuration Bits for P1.6–P1.0 (respectively).** Configures digital I/O Port cells to high or low output drive strength. 0: Corresponding P1.n Output has low output drive strength. 1: Corresponding P1.n Output has high output drive strength.

SFR Definition 21.18. P2: Port2

Bit	7	6	5	4	3	2	1	0
Name	P2							
Type	R/W							
Reset	1	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xA0; Bit-Addressable

Bit	Name	Description	Read	Write
7	P2	**Port 2 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P2.7 Port pin is logic LOW. 1: P2.7 Port pin is logic HIGH.
6:0	Unused	**Unused.** Read = 0000000b; Write = Don't Care.		

22.4.3. Hardware Slave Address Recognition

The SMBus hardware has the capability to automatically recognize incoming slave addresses and send an ACK without software intervention. Automatic slave address recognition is enabled by setting the EHACK bit in register SMB0ADM to 1. This will enable both automatic slave address recognition and automatic hardware ACK generation for received bytes (as a master or slave). More detail on automatic hardware ACK generation can be found in Section 22.4.2.2.

The registers used to define which address(es) are recognized by the hardware are the SMBus Slave Address register (SFR Definition 22.3) and the SMBus Slave Address Mask register (SFR Definition 22.4). A single address or range of addresses (including the General Call Address 0x00) can be specified using these two registers. The most-significant seven bits of the two registers are used to define which addresses will be ACKed. A 1 in bit positions of the slave address mask SLVM[6:0] enable a comparison between the received slave address and the hardware's slave address SLV[6:0] for those bits. A 0 in a bit of the slave address mask means that bit will be treated as a "don't care" for comparison purposes. In this case, either a 1 or a 0 value are acceptable on the incoming slave address. Additionally, if the GC bit in register SMB0ADR is set to 1, hardware will recognize the General Call Address (0x00). Table 22.4 shows some example parameter settings and the slave addresses that will be recognized by hardware under those conditions.

Table 22.4. Hardware Address Recognition Examples (EHACK = 1)

Hardware Slave Address SLV[6:0]	Slave Address Mask SLVM[6:0]	GC bit	Slave Addresses Recognized by Hardware
0x34	0x7F	0	0x34
0x34	0x7F	1	0x34, 0x00 (General Call)
0x34	0x7E	0	0x34, 0x35
0x34	0x7E	1	0x34, 0x35, 0x00 (General Call)
0x70	0x73	0	0x70, 0x74, 0x78, 0x7C

SFR Definition 22.3. SMB0ADR: SMBus Slave Address

Bit	7	6	5	4	3	2	1	0
Name	SLV[6:0]							GC
Type	R/W							R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xF4

Bit	Name	Function
7:1	SLV[6:0]	**SMBus Hardware Slave Address.** Defines the SMBus Slave Address(es) for automatic hardware acknowledgement. Only address bits which have a 1 in the corresponding bit position in SLVM[6:0] are checked against the incoming address. This allows multiple addresses to be recognized.
0	GC	**General Call Address Enable.** When hardware address recognition is enabled (EHACK = 1), this bit will determine whether the General Call Address (0x00) is also recognized by hardware. 0: General Call Address is ignored. 1: General Call Address is recognized.

SFR Definition 22.4. SMB0ADM: SMBus Slave Address Mask

Bit	7	6	5	4	3	2	1	0
Name	SLVM[6:0]							EHACK
Type	R/W							R/W
Reset	1	1	1	1	1	1	1	0

SFR Page = 0x0; SFR Address = 0xF5

Bit	Name	Function
7:1	SLVM[6:0]	**SMBus Slave Address Mask.** Defines which bits of register SMB0ADR are compared with an incoming address byte, and which bits are ignored. Any bit set to 1 in SLVM[6:0] enables comparisons with the corresponding bit in SLV[6:0]. Bits set to 0 are ignored (can be either 0 or 1 in the incoming address).
0	EHACK	**Hardware Acknowledge Enable.** Enables hardware acknowledgement of slave address and received data bytes. 0: Firmware must manually acknowledge all incoming address and data bytes. 1: Automatic Slave Address Recognition and Hardware Acknowledge is Enabled.

22.4.4. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 22.5. SMB0DAT: SMBus Data

Bit	7	6	5	4	3	2	1	0
Name	SMB0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC2

Bit	Name	Function
7:0	SMB0DAT[7:0]	**SMBus Data.** The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

23.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown below.

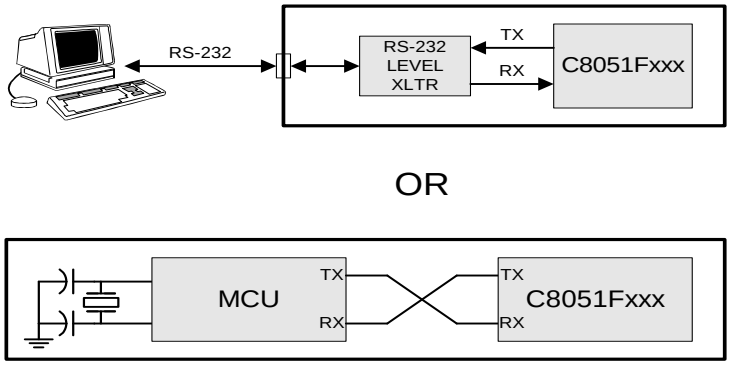

Figure 23.3. UART Interconnect Diagram

23.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 is set.

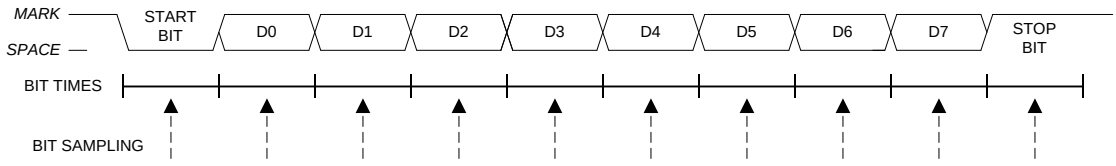

Figure 23.4. 8-Bit UART Timing Diagram

SFR Definition 24.4. SPInDAT: SPI Data

Bit	7	6	5	4	3	2	1	0
Name	SPInDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Addresses: SPI0DAT = 0xA3, SPI1DAT = 0x86
SFR Pages: SPI0DAT = 0x0, SPI1DAT = 0x0

Bit	Name	Function
7:0	SPInDAT	**SPIn Transmit and Receive Data.** The SPInDAT register is used to transmit and receive SPIn data. Writing data to SPInDAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPInDAT returns the contents of the receive buffer.

25.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section “12.5. Interrupt Register Descriptions” on page 123); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section “12.5. Interrupt Register Descriptions” on page 123). Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

25.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “21.3. Priority Crossbar Decoder” on page 209 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit (CKCON.3). When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 25.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 12.7). Setting GATE0 to 1 allows the timer to be controlled by the external input signal $\overline{\text{INT0}}$ (see Section “12.5. Interrupt Register Descriptions” on page 123), facilitating pulse width measurements

Table 25.1. Timer 0 Running Modes

TR0	GATE0	$\overline{\text{INT0}}$	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
Note: X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal $\overline{\text{INT1}}$ is used with Timer 1; the $\overline{\text{INT1}}$ polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 12.7).

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