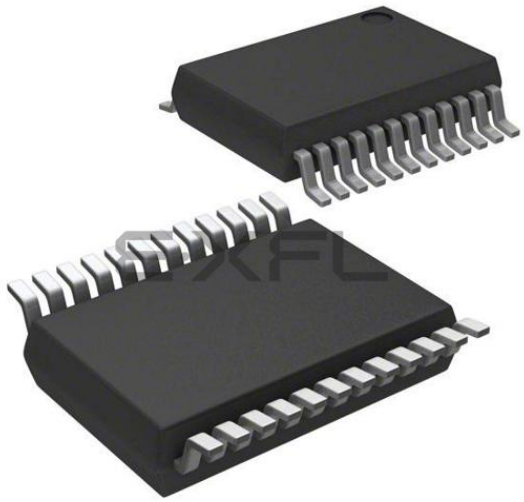

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 15x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f912-gur

1. System Overview

C8051F91x-C8051F90x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- Single/Dual Battery operation with on-chip dc-dc boost converter.
- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- 10-bit 300 ksps or 12-bit 75 ksps single-ended ADC with analog multiplexer
- 6-Bit Programmable Current Reference. Resolution can be increased with PWM.
- Precision programmable 24.5 MHz internal oscillator with spread spectrum technology.
- 16 kB or 8 kB of on-chip Flash memory
- 768 bytes of on-chip RAM
- SMBus/I^2C, Enhanced UART, and two Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- Two On-chip Voltage Comparators with 15 Capacitive Touch Sense inputs.
- 16 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F91x-C8051F90x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 0.9 to 1.8 V, 0.9 to 3.6 V or 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The C8051F91x-C8051F90x devices are available in 24-pin QFN or QSOP packages. Both package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 through Figure 1.4.

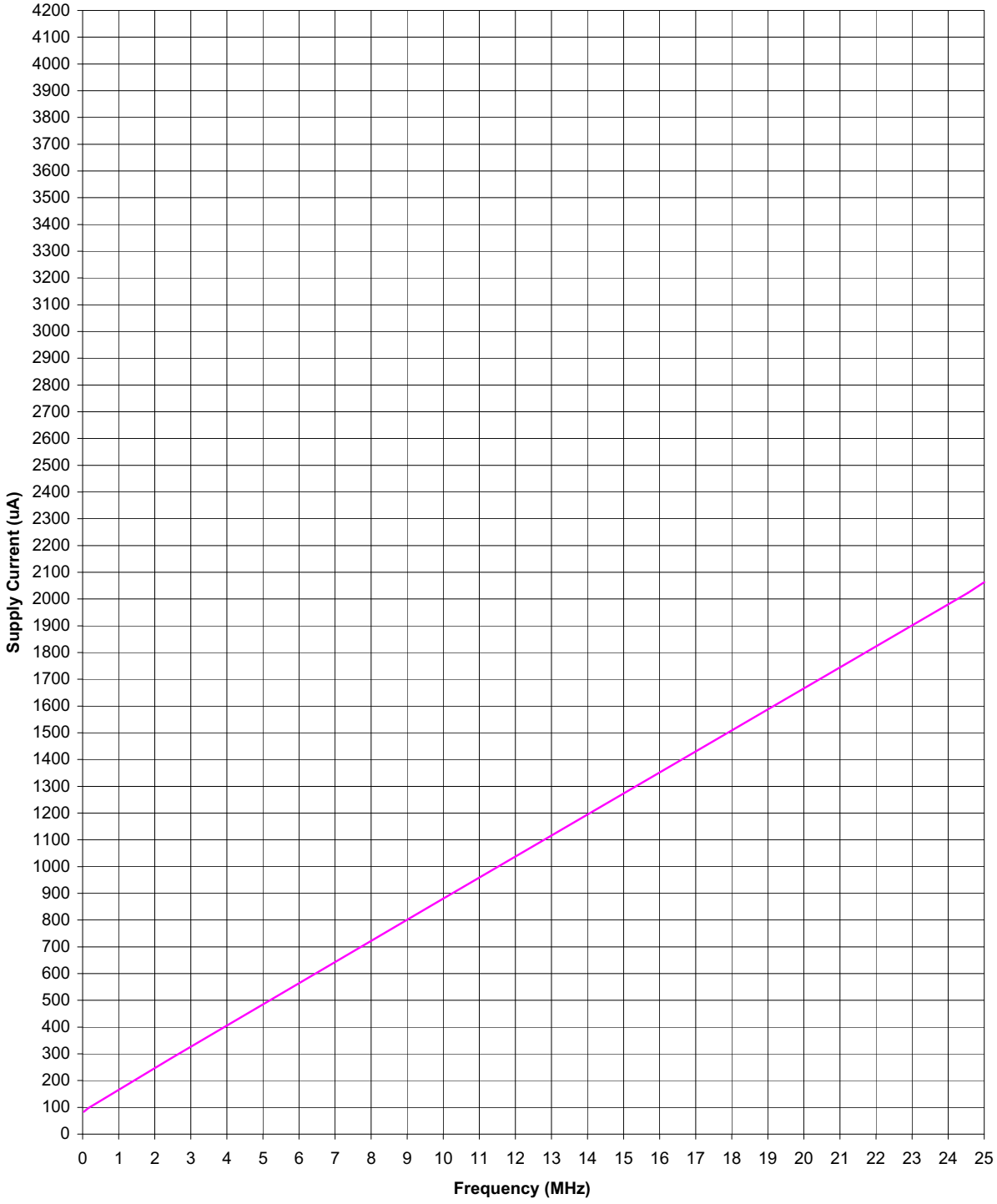

Figure 4.2. Idle Mode Current (External CMOS Clock)

Table 4.9. SmaRTClock Characteristics

V_{DD} = 1.8 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency (LFO)		**13.1**	**16.4**	**19.7**	kHz

Note: **Blue** indicates a feature only available on ‘F912 and ‘F902 devices.

Table 4.10. ADC0 Electrical Characteristics

V_{DD} = 1.8 to 3.6V V, VREF = 1.65 V (REFSL[1:0] = 11), –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution	**12-bit mode** 10-bit mode		**12** 10		bits
Integral Nonlinearity	**12-bit mode** [2] 10-bit mode	— —	**±1** ±0.5	**±1.5** ±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	**12-bit mode**[2] 10-bit mode	— —	**±0.8** ±0.5	**±1** ±1	LSB
Offset Error	**12-bit mode** 10-bit mode	— —	**±<1** ±<1	**±2** ±2	LSB
Full Scale Error	**12-bit mode**[3] 10-bit mode	— —	**±1** ±1	**±4** ±2.5	LSB
Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, maximum sampling rate)					
Signal-to-Noise Plus Distortion[4]	**12-bit mode** 10-bit mode	**62** 54	**65** 58	— —	dB
Signal-to-Distortion[4]	**12-bit mode** 10-bit mode	— —	**76** 73	— —	dB
Spurious-Free Dynamic Range[4]	**12-bit mode** 10-bit mode	— —	**82** 75	— —	dB
Conversion Rate					
SAR Conversion Clock	Normal Mode **Low Power Mode**	— —	— —	8.33 **4.4**	MHz
Conversion Time in SAR Clocks	10-bit Mode 8-bit Mode	13 11	— —	— —	clocks
Track/Hold Acquisition Time	Initial Acquisition Subsequent Acquisitions (DC input, burst mode)	1.5 1.1	—	—	us
Throughput Rate	**12-bit mode** 10-bit mode	— —	— —	**75** 300	ksps

Notes:

1. **Blue** indicates a feature only available on ‘F912 and ‘F902 devices.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code.
4. Performance in 8-bit mode is similar to 10-bit mode.

Notes on Registers, Operands and Addressing Modes:

Rn—Register R0–R7 of the currently selected register bank.

@Ri—Data RAM location addressed indirectly through R0 or R1.

rel—8-bit, signed (twos complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps.

direct—8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF).

#data—8-bit constant

#data16—16-bit constant

bit—Direct-accessed bit in Data RAM or SFR

addr11—11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction.

addr16—16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space.

There is one unused opcode (0xA5) that performs the same function as NOP.

SFR Definition 8.6. PSW: Program Status Word

Bit	7	6	5	4	3	2	1	0
Name	CY	AC	F0	RS[1:0]		OV	F1	PARITY
Type	R/W	R/W	R/W	R/W		R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xD0; Bit-Addressable

Bit	Name	Function
7	CY	**Carry Flag.** This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to logic 0 by all other arithmetic operations.
6	AC	**Auxiliary Carry Flag.** This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to logic 0 by all other arithmetic operations.
5	F0	**User Flag 0.** This is a bit-addressable, general purpose flag for use under software control.
4:3	RS[1:0]	**Register Bank Select.** These bits select which register bank is used during register accesses. 00: Bank 0, Addresses 0x00-0x07 01: Bank 1, Addresses 0x08-0x0F 10: Bank 2, Addresses 0x10-0x17 11: Bank 3, Addresses 0x18-0x1F
2	OV	**Overflow Flag.** This bit is set to 1 under the following circumstances: • An ADD, ADDC, or SUBB instruction causes a sign-change overflow. • A MUL instruction results in an overflow (result is greater than 255). • A DIV instruction causes a divide-by-zero condition. The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.
1	F1	**User Flag 1.** This is a bit-addressable, general purpose flag for use under software control.
0	PARITY	**Parity Flag.** This bit is set to logic 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

Table 12.1. Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit addressable?	Cleared by HW?	Enable Flag	Priority Control
Reset	0x0000	Top	None	N/A	N/A	Always Enabled	Always Highest
External Interrupt 0 ($\overline{INT0}$)	0x0003	0	IE0 (TCON.1)	Y	Y	EX0 (IE.0)	PX0 (IP.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	Y	Y	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1 ($\overline{INT1}$)	0x0013	2	IE1 (TCON.3)	Y	Y	EX1 (IE.2)	PX1 (IP.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	Y	Y	ET1 (IE.3)	PT1 (IP.3)
UART0	0x0023	4	RI0 (SCON0.0) TI0 (SCON0.1)	Y	N	ES0 (IE.4)	PS0 (IP.4)
Timer 2 Overflow	0x002B	5	TF2H (TMR2CN.7) TF2L (TMR2CN.6)	Y	N	ET2 (IE.5)	PT2 (IP.5)
SPI0	0x0033	6	SPIF (SPI0CN.7) WCOL (SPI0CN.6) MODF (SPI0CN.5) RXOVRN (SPI0CN.4)	Y	N	ESPI0 (IE.6)	PSPI0 (IP.6)
SMB0	0x003B	7	SI (SMB0CN.0)	Y	N	ESMB0 (EIE1.0)	PSMB0 (EIP1.0)
SmaRTClock Alarm	0x0043	8	ALRM (RTC0CN.2)[2]	N	N	EARTC0 (EIE1.1)	PARTC0 (EIP1.1)
ADC0 Window Comparator	0x004B	9	AD0WINT (ADC0CN.3)	Y	N	EWADC0 (EIE1.2)	PWADC0 (EIP1.2)
ADC0 End of Conversion	0x0053	10	AD0INT (ADC0STA.5)	Y	N	EADC0 (EIE1.3)	PADC0 (EIP1.3)
Programmable Counter Array	0x005B	11	CF (PCA0CN.7) CCFn (PCA0CN.n)	Y	N	EPCA0 (EIE1.4)	PPCA0 (EIP1.4)
Comparator0	0x0063	12	CP0FIF (CPT0CN.4) CP0RIF (CPT0CN.5)	N	N	ECP0 (EIE1.5)	PCP0 (EIP1.5)
Comparator1	0x006B	13	CP1FIF (CPT1CN.4) CP1RIF (CPT1CN.5)	N	N	ECP1 (EIE1.6)	PCP1 (EIP1.6)
Timer 3 Overflow	0x0073	14	TF3H (TMR3CN.7) TF3L (TMR3CN.6)	N	N	ET3 (EIE1.7)	PT3 (EIP1.7)
Supply Monitor Early Warning	0x007B	15	VDDOK (VDM0CN.5)[1] **VBATOK (VDM0CN.4)**[1, 3]			EWARN (EIE2.0)	PWARN (EIP2.0)
Port Match	0x0083	16	None			EMAT (EIE2.1)	PMAT (EIP2.1)
SmaRTClock Oscillator Fail	0x008B	17	OSCFAIL (RTC0CN.5)[2]	N	N	ERTC0F (EIE2.2)	PFRTC0F (EIP2.2)
SPI1	0x0093	18	SPIF (SPI1CN.7) WCOL (SPI1CN.6) MODF (SPI1CN.5) RXOVRN (SPI1CN.4)	N	N	ESPI1 (EIE2.3)	PSPI1 (EIP2.3)

Notes:

1. Indicates a read-only interrupt pending flag. The interrupt enable may be used to prevent software from vectoring to the associated interrupt service routine.
2. Indicates a register located in an indirect memory space.
3. **8Blue** text Indicates a bit only available on ‘F912 and ‘F902 devices.

SFR Definition 12.6. EIP2: Extended Interrupt Priority 2

Bit	7	6	5	4	3	2	1	0
Name					PSPI1	PRTC0F	PMAT	PWARN
Type	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xF7

Bit	Name	Function
7:4	Unused	**Unused.** Read = 0000b. Write = Don't care.
3	PSPI1	**Serial Peripheral Interface (SPI1) Interrupt Priority Control.** This bit sets the priority of the SPI1 interrupt. 0: SP1 interrupt set to low priority level. 1: SPI1 interrupt set to high priority level.
2	PRTC0F	**SmaRTClock Oscillator Fail Interrupt Priority Control.** This bit sets the priority of the SmaRTClock Alarm interrupt. 0: SmaRTClock Alarm interrupt set to low priority level. 1: SmaRTClock Alarm interrupt set to high priority level.
1	PMAT	**Port Match Interrupt Priority Control.** This bit sets the priority of the Port Match Event interrupt. 0: Port Match interrupt set to low priority level. 1: Port Match interrupt set to high priority level.
0	PWARN	**Supply Monitor Early Warning Interrupt Priority Control.** This bit sets the priority of the VDD/DC+ Supply Monitor Early Warning interrupt. 0: Supply Monitor Early Warning interrupt set to low priority level. 1: Supply Monitor Early Warning interrupt set to high priority level.

13.4. Determining the Device Part Number at Run Time

In many applications, user software may need to determine the MCU part number at run time in order to determine the hardware capabilities. The part number can be determined by reading the value of the Flash byte at address 0x3FFE.

The value of the Flash byte at address 0x3FFE can be decoded as follows:

0xD0—C8051F901
0xD1—C8051F902
0xD2—C8051F911
0xD3—C8051F912

15. Cyclic Redundancy Check Unit (CRC0)

C8051F91x-C8051F90x devices include a cyclic redundancy check unit (CRC0) that can perform a CRC using a 16-bit or 32-bit polynomial. CRC0 accepts a stream of 8-bit data written to the CRC0IN register. CRC0 posts the 16-bit or 32-bit result to an internal register. The internal result register may be accessed indirectly using the CRC0PNT bits and CRC0DAT register, as shown in Figure 15.1. CRC0 also has a bit reverse register for quick data manipulation.

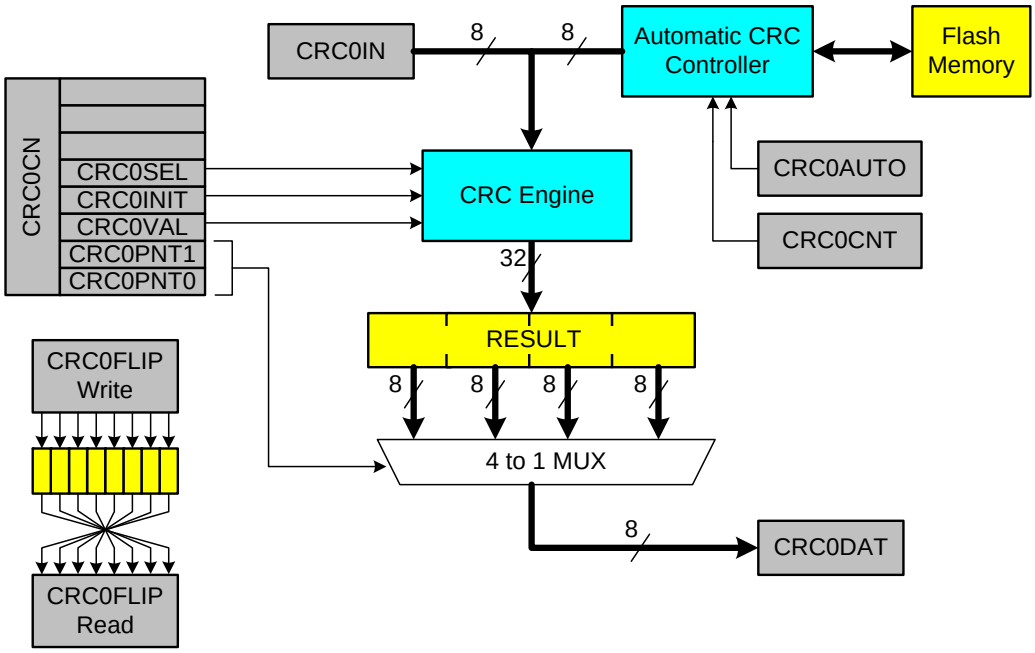

Figure 15.1. CRC0 Block Diagram

15.1. CRC Algorithm

The C8051F91x-C8051F90x CRC unit generates a CRC result equivalent to the following algorithm:

1. XOR the input with the most-significant bits of the current CRC result. If this is the first iteration of the CRC unit, the current CRC result will be the set initial value (0x00000000 or 0xFFFFFFFF).

2a. If the MSB of the CRC result is set, shift the CRC result and XOR the result with the selected polynomial.

2b. If the MSB of the CRC result is not set, shift the CRC result.

Repeat Steps 2a/2b for the number of input bits (8). The algorithm is also described in the following example.

The 16-bit C8051F91x-C8051F90x CRC algorithm can be described by the following code:

```
unsigned short UpdateCRC (unsigned short CRC_acc, unsigned char CRC_input)
{
   unsigned char i;                    // loop counter

   #define POLY 0x1021

   // Create the CRC "dividend" for polynomial arithmetic (binary arithmetic
```

16.5. Minimizing Power Supply Noise

To minimize noise on the power supply lines, the GND and GND/DC- pins should be kept separate, as shown in Figure 16.2; one or the other should be connected to the pc board ground plane. For applications in which the dc-dc converter is used only to power internal circuits, the GND pin is normally connected to the board ground.

The large decoupling capacitors in the input and output circuits ensure that each supply is relatively quiet with respect to its own ground. However, connecting a circuit element "diagonally" (e.g. connecting an external chip between VDD/DC+ and GND, or between VBAT and GND/DC-) can result in high supply noise across that circuit element. For applications in which the dc-dc converter is used to power external analog circuitry, it is recommended to connect the GND/DC– pin to the board ground and connect the battery's negative terminal to the GND pin only, which is not connected to board ground.

To accommodate situations in which ADC0 is sampling a signal that is referenced to one of the external grounds, we recommend using the Analog Ground Reference (P0.1/AGND) option described in Section 5.12. This option prevents any voltage differences between the internal chip ground and the external grounds from modulating the ADC input signal. If this option is enabled, the P0.1 pin should be tied to the ground reference of the external analog input signal. When using the ADC with the dc-dc converter, we also recommend enabling the SYNC bit in the DC0CN register to minimize interference.

These general guidelines provide the best performance in most applications, though some situations may benefit from experimentation to eliminate any residual noise issues. Examples might include tying the grounds together, using additional low-inductance decoupling caps in parallel with the recommended ones, investigating the effects of different dc-dc converter settings, etc.

16.6. Selecting the Optimum Switch Size

The dc-dc converter has two built-in switches (the diode bypass switch and duty cycle control switch). To maximize efficiency, one of two switch sizes may be selected. The large switches are ideal for carrying high currents and the small switches are ideal for low current applications. The ideal switchover point to switch from the small switches to the large switches varies with the programmed output voltage. At an output voltage of 2 V, the ideal switchover point is at approximately 4 mA total output current. At an output voltage of 3 V, the ideal switchover point is at approximately 8 mA total output current.

16.7. DC-DC Converter Clocking Options

The dc-dc converter may be clocked from its internal oscillator, or from any system clock source, selectable by the CLKSEL bit (DC0CF.0). The dc-dc converter internal oscillator frequency is approximately 2.4 MHz. For a more accurate clock source, the system clock, or a divided version of the system clock may be used as the dc-dc clock source. The dc-dc converter has a built in clock divider (configured using DC0CF[6:5]) which allows any system clock frequency over 1.6 MHz to generate a valid clock in the range of 1.6 to 3.2 MHz.

When the precision internal oscillator is selected as the system clock source, the OSCICL register may be used to fine tune the oscillator frequency and the dc-dc converter clock. The oscillator frequency should only be decreased since it is factory calibrated at its maximum frequency. The minimum frequency which can be reached by the oscillator after taking into account process variations is approximately 16 MHz. The system clock routed to the dc-dc converter clock divider also may be inverted by setting the CLKINV bit (DC0CF.3) to logic 1. These options can be used to minimize interference in noise sensitive applications.

16.8. DC-DC Converter Behavior in Sleep Mode

When the C8051F91x-C8051F90x devices are placed in Sleep mode, the dc-dc converter is disabled, and the VDD/DC+ output is internally connected to VBAT by default. This behavior ensures that the GPIO pins are powered from a low-impedance source during sleep mode. If the GPIO pins are not used as inputs or

16.11. Passive Diode Mode (C8051F912/02 only)

Setting the EXTDEN bit in DC0MD enables the Passive Diode Mode. In this mode, the control circuits for the Diode Bypass switch are disabled, which reduces the converter's quiescent operating current. An external Schottky diode may be connected between the DCEN (anode) and VDD/DC+ (cathode) pins. Under light load conditions, an external diode is typically not required. There are two situations in which this mode can prove beneficial. First is with very light load currents, where the efficiency is dominated by the converter's quiescent current. The converter will use an internal p-n junction diode to transfer current from the inductor to the output capacitor; although there is a larger voltage drop (and power loss) across a passive diode, the overall efficiency may be improved due to the reduction in quiescent current. The second situation is when output power is very high. In that case, efficiency can suffer because some reverse current can flow in the Diode Bypass switch before the control circuitry turns the switch off. Putting the device in Passive Diode Mode and optionally connecting an external Schottky diode between the DCEN and VDD/DC+ pins (parallel to the internal diode) may provide higher efficiency in some applications than using the internal Diode Bypass switch.

16.12. DC-DC Converter Register Descriptions

The SFRs used to configure the dc-dc converter are described in the following register descriptions. The reset values for these registers can be used as-is in most systems; therefore, no software intervention or initialization is required.

SFR Definition 16.1. DC0CN: DC-DC Converter Control

Bit	7	6	5	4	3	2	1	0
Name	MINPW		SWSEL	Reserved	SYNC	VSEL		
Type	R/W		R/W	R/W	R/W	R/W		
Reset	0	0	1	0	0	0	0	1

SFR Page = 0x0; SFR Address = 0x97

Bit	Name	Function
7:6	MINPW[1:0]	**DC-DC Converter Minimum Pulse Width.** Specifies the minimum pulse width. 00: No minimum duty cycle. 01: Minimum pulse width is 20 ns. 10: Minimum pulse width is 40 ns. 11: Minimum pulse width is 80 ns.
5	SWSEL	**DC-DC Converter Switch Select.** Selects one of two possible converter switch sizes to maximize efficiency. 0: The large switches are selected (best efficiency for high output currents). 1: The small switches are selected (best efficiency for low output currents).
4	Reserved	Reserved. Always Write to 0.
3	SYNC	**ADC0 Synchronization Enable.** When synchronization is enabled, the ADC0SC[4:0] bits in the ADC0CF register must be set to 00000b. 0: The ADC is not synchronized to the dc-dc converter. 1: The ADC is synchronized to the dc-dc converter. ADC0 tracking is performed during the longest quiet time of the dc-dc converter switching cycle and ADC0 SAR clock is also synchronized to the dc-dc converter switching cycle.
2:0	VSEL[2:0]	**DC-DC Converter Output Voltage Select.** Specifies the target output voltage. 000: Target output voltage is 1.8 V. 001: Target output voltage is 1.9 V. 010: Target output voltage is 2.0 V. 011: Target output voltage is 2.1 V. 100: Target output voltage is 2.4 V. 101: Target output voltage is 2.7 V. 110: Target output voltage is 3.0 V. 111: Target output voltage is 3.3 V.

20. SmaRTClock (Real Time Clock)

C8051F91x-C8051F90x devices include an ultra low power 32-bit SmaRTClock Peripheral (Real Time Clock) with alarm. The SmaRTClock has a dedicated 32 kHz oscillator that can be configured for use with or without a crystal. No external resistor or loading capacitors are required. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals. The SmaRTClock can operate directly from a 0.9–3.6 V battery voltage and remains operational even when the device goes into its lowest power down mode. On ‘F912 and ‘F902 devices, the SmaRTClock output can be buffered and routed to a GPIO pin to provide an accurate, low frequency clock to other devices while the MCU is in its lowest power down mode (see “PMU0MD: Power Management Unit Mode” on page 150 for more details). ‘F912 and ‘F902 devices also support an ultra low power internal LFO that reduces sleep mode current.

The SmaRTClock allows a maximum of 36 hour 32-bit independent time-keeping when used with a 32.768 kHz Watch Crystal. The SmaRTClock provides an Alarm and Missing SmaRTClock events, which could be used as reset or wakeup sources. See Section “18. Reset Sources” on page 171 and Section “14. Power Management” on page 143 for details on reset sources and low power mode wake-up sources, respectively.

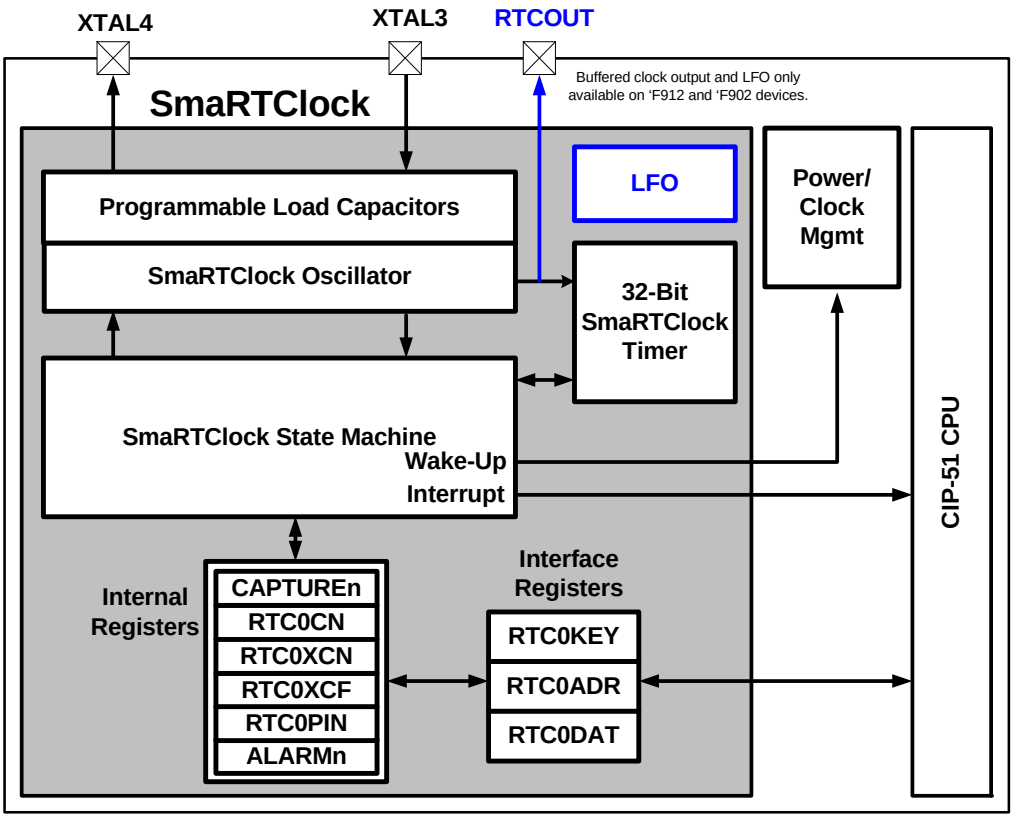

Figure 20.1. SmaRTClock Block Diagram

20.2.2. Using the SmaRTClock Oscillator in Self-Oscillate Mode

When using Self-Oscillate Mode, the XTAL3 and XTAL4 pins should be shorted together. The RTC0PIN register can be used to internally short XTAL3 and XTAL4. The following steps show how to configure SmaRTClock for use in Self-Oscillate Mode:

1. Set SmaRTClock to Self-Oscillate Mode (XMODE = 0).
2. Set the desired oscillation frequency:
   For oscillation at about 20 kHz, set BIASX2 = 0.
   For oscillation at about 40 kHz, set BIASX2 = 1.
3. The oscillator starts oscillating instantaneously.
4. Fine tune the oscillation frequency by adjusting the load capacitance (RTC0XCF).

20.2.3. Using the Low Frequency Oscillator (LFO)

The low frequency oscillator provides an ultra low power, on-chip clock source to the SmaRTClock. The typical frequency of oscillation is 16.4 kHz ±20%. No external components are required to use the LFO and the XTAL3 and XTAL4 pins do not need to be shorted together. The LFO is only available on ‘F912 and ‘F902 devices.

The following steps show how to configure SmaRTClock for use with the LFO:

1. Enable and select the Low Frequency Oscillator (LFOEN = 1).
2. The LFO starts oscillating instantaneously.

When the LFO is enabled, the SmaRTClock oscillator increments bit 1 of the 32-bit timer (instead of bit 0). This effectively multiplies the LFO frequency by 2, making the RTC timebase behave as if a 32.768 kHz crystal is connected at the output.

21.1.3. Interfacing Port I/O to 5 V and 3.3 V Logic

All Port I/O configured for digital, open-drain operation are capable of interfacing to digital logic operating at a supply voltage higher than 4.5 V and less than 5.25 V. When the supply voltage is in the range of 1.8 to 2.2 V, the I/O may also interface to digital logic operating between 3.0 to 3.6 V if the input signal frequency is less than 12.5 MHz or less than 25 MHz if the signal rise time (10% to 90%) is less than 1.2 ns. When operating at a supply voltage above 2.2 V, the device should not interface to 3.3 V logic; however, interfacing to 5 V logic is permitted. An external pull-up resistor to the higher supply voltage is typically required for most systems.

Important Note:

- When interfacing to a signal that is between 4.5 and 5.25 V, the maximum clock frequency that may be input on a GPIO pin is 12.5 MHz. The exception to this rule is when routing an external CMOS clock to P0.3, in which case, a signal up to 25 MHz is valid as long as the rise time (10% to 90%) is shorter than 1.8 ns.
- When the supply voltage is less than 2.2 V and interfacing to a signal that is between 3.0 and 3.6 V, the maximum clock frequency that may be input on a GPIO pin is 3.125 MHz. The exception to this rule is when routing an external CMOS clock to P0.3, in which case, a signal up to 25 MHz is valid as long as the rise time (10% to 90%) is shorter than 1.2 ns.
- In a multi-voltage interface, the external pull-up resistor should be sized to allow a current of at least 150 µA to flow into the Port pin when the supply voltage is between (VDD/DC+ plus 0.4 V) and (VDD/DC+ plus 1.0 V). Once the Port pad voltage increases beyond this range, the current flowing into the Port pin is minimal.
- These guidelines only apply to multi-voltage interfaces. Port I/Os may always interface to digital logic operating at the same supply voltage.

21.1.4. Increasing Port I/O Drive Strength

Port I/O output drivers support a high and low drive strength; the default is low drive strength. The drive strength of a Port I/O can be configured using the PnDRV registers. See Section “4. Electrical Characteristics” on page 36 for the difference in output drive strength between the two modes.

21.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins P0.0–P1.6 can be assigned to various analog, digital, and external interrupt functions. The Port pins assuaged to analog functions should be configured for analog I/O and Port pins assuaged to digital or external interrupt functions should be configured for digital I/O.

21.2.1. Assigning Port I/O Pins to Analog Functions

Table 21.1 shows all available analog functions that need Port I/O assignments. **Port pins selected for these analog functions should have their digital drivers disabled (PnMDOUT.n = 0 and Port Latch = 1) and their corresponding bit in PnSKIP set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the Crossbar. Table 21.1 shows the potential mapping of Port I/O to each analog function.

Table 21.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P1.6	ADC0MX, PnSKIP
Comparator0 Input	P0.0–P1.6	CPT0MX, PnSKIP
Comparator1 Input	P0.0–P1.6	CPT1MX, PnSKIP

SFR Definition 21.19. P2MDOUT: Port2 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P2MDOUT							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xA6

Bit	Name	Function
7	P2MDOUT	**Output Configuration Bits for P2.7.** These bits control the digital driver. 0: P2.7 Output is open-drain. 1: P2.7 Output is push-pull.
6:0	Unused	**Unused.** Read = 0000000b; Write = Don't Care.

SFR Definition 21.20. P2DRV: Port2 Drive Strength

Bit	7	6	5	4	3	2	1	0
Name	P2DRV							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0F; SFR Address = 0xA6

Bit	Name	Function
7	P2DRV	**Drive Strength Configuration Bits for P2.7.** Configures digital I/O Port cells to high or low output drive strength. 0: P2.7 Output has low output drive strength. 1: P2.7 Output has high output drive strength.
6:0	Unused	**Unused.** Read = 0000000b; Write = Don't Care.

22.4.4. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 22.5. SMB0DAT: SMBus Data

Bit	7	6	5	4	3	2	1	0
Name	SMB0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC2

Bit	Name	Function
7:0	SMB0DAT[7:0]	**SMBus Data.** The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

22.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. Note that the position of the ACK interrupt when operating as a receiver depends on whether hardware ACK generation is enabled. As a receiver, the interrupt for an ACK occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled. As a transmitter, interrupts occur **after** the ACK, regardless of whether hardware ACK generation is enabled or not.

22.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 22.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the ‘data byte transferred’ interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.

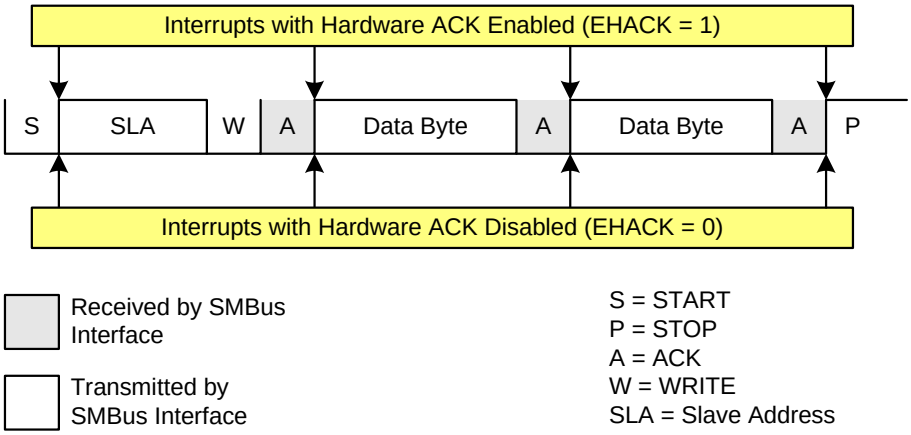

Figure 22.5. Typical Master Write Sequence

Table 22.6. SMBus Status Decoding With Hardware ACK Generation Enabled (EHACK = 1)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X	1100
	1100	0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X	1110
						Abort transfer.	0	1	X	-
		0	0	1	A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0DAT.	0	0	X	1100
						End transfer with STOP.	0	1	X	-
						End transfer with STOP and start another transfer.	1	1	X	-
						Send repeated START.	1	0	X	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT). Set ACK for initial data byte.	0	0	1	1000
Master Receiver	1000	0	0	1	A master data byte was received; ACK sent.	Set ACK for next data byte; Read SMB0DAT.	0	0	1	1000
						Set NACK to indicate next data byte as the last data byte; Read SMB0DAT.	0	0	0	1000
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
		0	0	0	A master data byte was received; NACK sent (last byte).	Read SMB0DAT; send STOP.	0	1	0	-
						Read SMB0DAT; Send STOP followed by START.	1	1	0	1110
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100

26.3.4. Frequency Output Mode

Frequency Output Mode produces a programmable-frequency square wave on the module's associated CEXn pin. The capture/compare module high byte holds the number of PCA clocks to count before the output is toggled. The frequency of the square wave is then defined by Equation 26.1.

$$F_{CEXn} = \frac{F_{PCA}}{2 \times PCA0CPHn}$$

Note: A value of 0x00 in the PCA0CPHn register is equal to 256 for this equation.

Equation 26.1. Square Wave Frequency Output

Where F_{PCA} is the frequency of the clock selected by the CPS2–0 bits in the PCA mode register, PCA0MD. The lower byte of the capture/compare module is compared to the PCA counter low byte; on a match, CEXn is toggled and the offset held in the high byte is added to the matched value in PCA0CPLn. Frequency Output Mode is enabled by setting the ECOMn, TOGn, and PWMn bits in the PCA0CPMn register. Note that the MATn bit should normally be set to 0 in this mode. If the MATn bit is set to 1, the CCFn flag for the channel will be set when the 16-bit PCA0 counter and the 16-bit capture/compare register for the channel are equal.

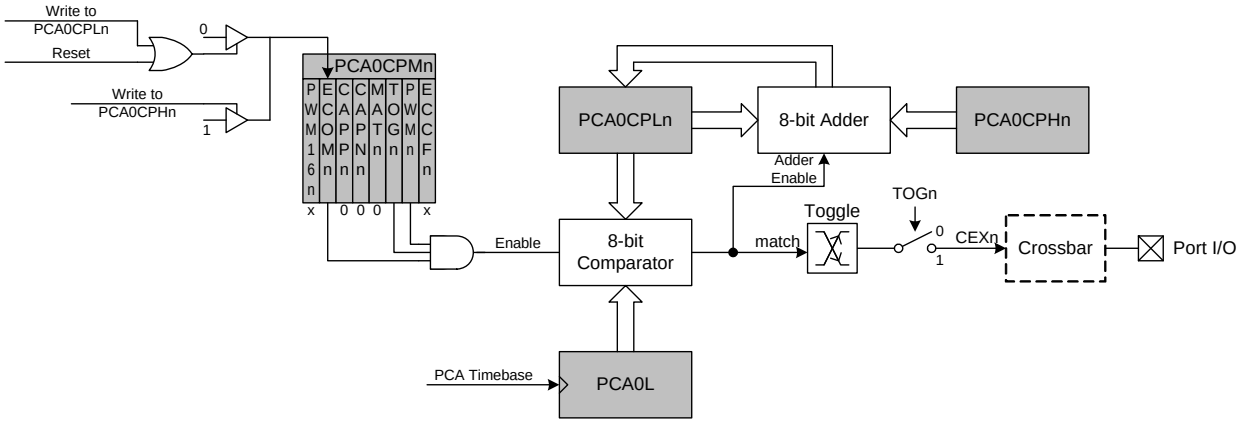

Figure 26.7. PCA Frequency Output Mode