Infineon Technologies - MB96F326RSBPMC-GSE2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

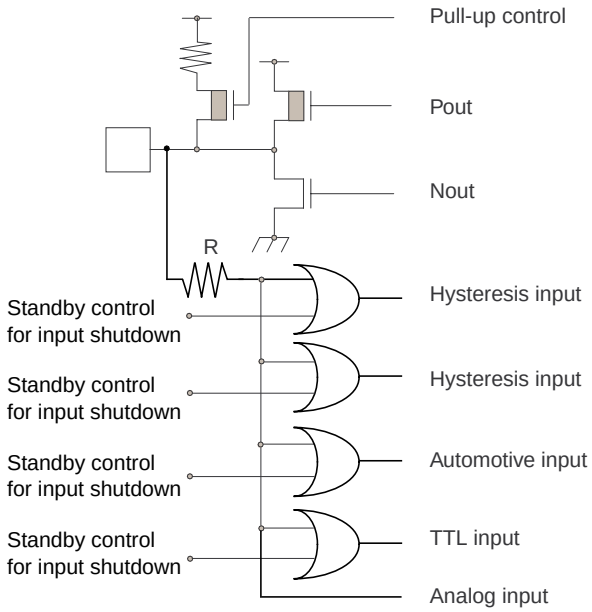
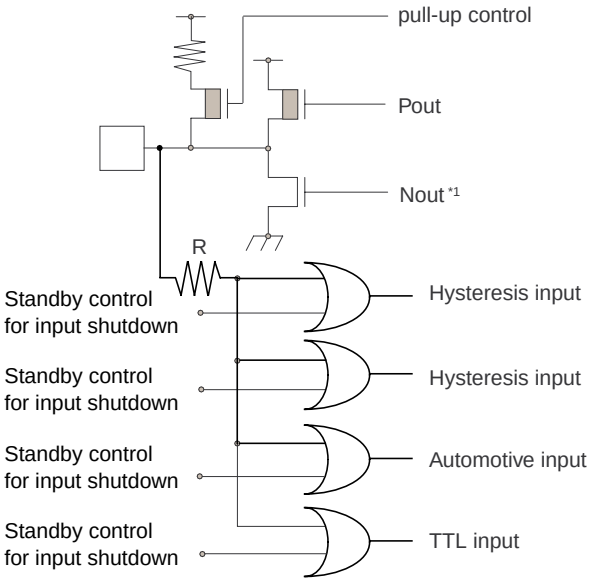
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	66
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 18x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f326rsbpmc-gse2

■ FEATURES

Feature	Description
Technology	• 0.18µm CMOS
CPU	• F²MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) • 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). • Up to 56 MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
CAN	• Supports CAN protocol version 2.0 part A and B • ISO16845 certified • Bit rates up to 1 Mbit/s • 32 message objects • Each message object has its own identifier mask • Programmable FIFO mode (concatenation of message objects) • Maskable interrupt • Disabled Automatic Retransmission mode for Time Triggered CAN applications • Programmable loop-back mode for self-test operation
USART	• Full duplex USARTs (SCI/LIN) • Wide range of baud rate settings using a dedicated reload timer • Special synchronous options for adapting to different synchronous serial protocols • LIN functionality working either as master or slave LIN device
I^2C	• Up to 400 kbps • Master and Slave functionality, 7-bit and 10-bit addressing
A/D converter	• SAR-type • 10-bit resolution • Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
Reload Timers	• 16-bit wide • Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency • Event count function
Free Running Timers	• Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency
Input Capture Units	• 16-bit wide • Signals an interrupt upon external event • Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	• 16-bit wide • Signals an interrupt when a match with 16-bit I/O Timer occurs • A pair of compare registers can be used to generate an output signal.
Programmable Pulse Generator	• 16-bit down counter, cycle and duty setting registers • Interrupt at trigger, counter borrow and/or duty match • PWM operation and one-shot operation • Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer underflow as clock input • Can be triggered by software or reload timer

Type	Circuit	Remarks
I		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50kΩ approx. • Analog input
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. *1: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage

■ I/O MAP

I/O map MB96(F)32x (1 of 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000H	I/O Port P00 - Port Data Register	PDR00		R/W
000001H	I/O Port P01 - Port Data Register	PDR01		R/W
000002H	I/O Port P02 - Port Data Register	PDR02		R/W
000003H	I/O Port P03 - Port Data Register	PDR03		R/W
000004H	I/O Port P04 - Port Data Register	PDR04		R/W
000005H	I/O Port P05 - Port Data Register	PDR05		R/W
000006H	I/O Port P06 - Port Data Register	PDR06		R/W
000007H	I/O Port P07 - Port Data Register	PDR07		R/W
000008H	Reserved			-
000009H	I/O Port P09 - Port Data Register	PDR09		R/W
00000AH-00000CH	Reserved			-
00000DH	I/O Port P13 - Port Data Register	PDR13		R/W
00000EH-000010H	Reserved			-
000011H	I/O Port P17 - Port Data Register	PDR17		R/W
000012H-000017H	Reserved			-
000018H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019H	ADC0 - Control Status register High	ADCSH		R/W
00001AH	ADC0 - Data Register Low	ADCRL	ADCR	R
00001BH	ADC0 - Data Register High	ADCRH		R
00001CH	ADC0 - Setting Register		ADSR	R/W
00001DH	ADC0 - Setting Register			R/W
00001EH	ADC0 - Extended Configuration Register	ADECR		R/W
00001FH	Reserved			-
000020H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021H	FRT0 - Data register of free-running timer			R/W
000022H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W

I/O map MB96(F)32x (2 of 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000023H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025H	FRT1 - Data register of free-running timer			R/W
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028H-000033H	Reserved			-
000034H	OCU4 - Output Compare Control Status	OCS4		R/W
000035H	OCU5 - Output Compare Control Status	OCS5		R/W
000036H	OCU4 - Compare Register		OCCP4	R/W
000037H	OCU4 - Compare Register			R/W
000038H	OCU5 - Compare Register		OCCP5	R/W
000039H	OCU5 - Compare Register			R/W
00003AH	OCU6 - Output Compare Control Status	OCS6		R/W
00003BH	OCU7 - Output Compare Control Status	OCS7		R/W
00003CH	OCU6 - Compare Register		OCCP6	R/W
00003DH	OCU6 - Compare Register			R/W
00003EH	OCU7 - Compare Register		OCCP7	R/W
00003FH	OCU7 - Compare Register			R/W
000040H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041H	ICU0/ICU1 - Edge register	ICE01		R/W
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043H	ICU0 - Capture Register High	IPCPH0		R
000044H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045H	ICU1 - Capture Register High	IPCPH1		R
000046H	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047H	ICU2/ICU3 - Edge register	ICE23		R/W
000048H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R

I/O map MB96(F)32x (9 of 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00011E$_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F$_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120$_H$-00017F$_H$	Reserved			-
000180$_H$-00037F$_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380$_H$	DMA0 - Interrupt select	DISEL0		R/W
000381$_H$	DMA1 - Interrupt select	DISEL1		R/W
000382$_H$	DMA2 - Interrupt select	DISEL2		R/W
000383$_H$	DMA3 - Interrupt select	DISEL3		R/W
000384$_H$-00038F$_H$	Reserved			-
000390$_H$	DMA - Status register low byte	DSRL	DSR	R/W
000391$_H$	DMA - Status register high byte	DSRH		R/W
000392$_H$	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393$_H$	DMA - Stop status register high byte	DSSRH		R/W
000394$_H$	DMA - Enable register low byte	DERL	DER	R/W
000395$_H$	DMA - Enable register high byte	DERH		R/W
000396$_H$-00039F$_H$	Reserved			-
0003A0$_H$	Interrupt level register	ILR	ICR	R/W
0003A1$_H$	Interrupt index register	IDX		R/W
0003A2$_H$	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3$_H$	Interrupt vector table base register High	TBRH		R/W
0003A4$_H$	Delayed Interrupt register	DIRR		R/W
0003A5$_H$	Non Maskable Interrupt register	NMI		R/W
0003A6$_H$-0003AB$_H$	Reserved			-
0003AC$_H$	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003AD$_H$	EDSU communication interrupt selection High	EDSU2H		R/W
0003AE$_H$	ROM mirror control register	ROMM		R/W
0003AF$_H$	EDSU configuration register	EDSU		R/W

I/O map MB96(F)32x (13 of 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00042D$_H$	Clock Input and LVD Control Register	CILCR		R/W
00042E$_H$-00042F$_H$	Reserved			-
000430$_H$	I/O Port P00 - Data Direction Register	DDR00		R/W
000431$_H$	I/O Port P01 - Data Direction Register	DDR01		R/W
000432$_H$	I/O Port P02 - Data Direction Register	DDR02		R/W
000433$_H$	I/O Port P03 - Data Direction Register	DDR03		R/W
000434$_H$	I/O Port P04 - Data Direction Register	DDR04		R/W
000435$_H$	I/O Port P05 - Data Direction Register	DDR05		R/W
000436$_H$	I/O Port P06 - Data Direction Register	DDR06		R/W
000437$_H$	I/O Port P07 - Data Direction Register	DDR07		R/W
000438$_H$	Reserved			-
000439$_H$	I/O Port P09 - Data Direction Register	DDR09		R/W
00043A$_H$-00043C$_H$	Reserved			-
00043D$_H$	I/O Port P13 - Data Direction Register	DDR13		R/W
00043E$_H$-000440$_H$	Reserved			-
000441$_H$	I/O Port P17 - Data Direction Register	DDR17		R/W
000442$_H$-000443$_H$	Reserved			-
000444$_H$	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445$_H$	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446$_H$	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447$_H$	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448$_H$	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449$_H$	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044A$_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044B$_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
00044C$_H$	Reserved			-
00044D$_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W

I/O map MB96(F)32x (16 of 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004AA$_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004AB$_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004AC$_H$	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
0004AD$_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AE$_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AF$_H$	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
0004B0$_H$	Reserved			-
0004B1$_H$	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
0004B2$_H$-0004B4$_H$	Reserved			-
0004B5$_H$	I/O Port P13 - Pull-Up resistor Control Register	PUCR13		R/W
0004B6$_H$-0004B8$_H$	Reserved			-
0004B9$_H$	I/O Port P17 - Pull-Up resistor Control Register	PUCR17		R/W
0004BA$_H$-0004BB$_H$	Reserved			-
0004BC$_H$	I/O Port P00 - External Pin State Register	EPSR00		R
0004BD$_H$	I/O Port P01 - External Pin State Register	EPSR01		R
0004BE$_H$	I/O Port P02 - External Pin State Register	EPSR02		R
0004BF$_H$	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0$_H$	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1$_H$	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2$_H$	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3$_H$	I/O Port P07 - External Pin State Register	EPSR07		R
0004C4$_H$	Reserved			-
0004C5$_H$	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6$_H$-0004C8$_H$	Reserved			-
0004C9$_H$	I/O Port P13 - External Pin State Register	EPSR13		R
0004CA$_H$-0004CC$_H$	Reserved			-
0004CD$_H$	I/O Port P17 - External Pin State Register	EPSR17		R

I/O map MB96(F)32x (17 of 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004CE$_H$-0004CF$_H$	Reserved			-
0004D0$_H$	ADC analog input enable register 0	ADER0		R/W
0004D1$_H$	ADC analog input enable register 1	ADER1		R/W
0004D2$_H$	ADC analog input enable register 2	ADER2		R/W
0004D3$_H$	ADC analog input enable register 3	ADER3		R/W
0004D4$_H$	ADC analog input enable register 4	ADER4		R/W
0004D5$_H$	Reserved			-
0004D6$_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7$_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8$_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9$_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DA$_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB$_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC$_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD$_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE$_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF$_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0$_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1$_H$	RTC - Sub Second Register M	WTBRH0		R/W
0004E2$_H$	RTC - Sub-Second Register H	WTBR1		R/W
0004E3$_H$	RTC - Second Register	WTSR		R/W
0004E4$_H$	RTC - Minutes	WTMR		R/W
0004E5$_H$	RTC - Hour	WTHR		R/W
0004E6$_H$	RTC - Timer Control Extended Register	WTCER		R/W
0004E7$_H$	RTC - Clock select register	WTCKSR		R/W
0004E8$_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9$_H$	RTC - Timer Control Register High	WTCRH		R/W
0004EA$_H$	CAL - Calibration unit Control register	CUCR		R/W
0004EB$_H$	Reserved			-

I/O map MB96(F)32x (21 of 31)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00057D$_H$	PPG8 - Duty cycle register			W
00057E$_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057F$_H$	PPG8 - Control status register High	PCNH8		R/W
000580$_H$	PPG9 - Timer register		PTMR9	R
000581$_H$	PPG9 - Timer register			R
000582$_H$	PPG9 - Period setting register		PCSR9	W
000583$_H$	PPG9 - Period setting register			W
000584$_H$	PPG9 - Duty cycle register		PDUT9	W
000585$_H$	PPG9 - Duty cycle register			W
000586$_H$	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587$_H$	PPG9 - Control status register High	PCNH9		R/W
000588$_H$	PPG10 - Timer register		PTMR10	R
000589$_H$	PPG10 - Timer register			R
00058A$_H$	PPG10 - Period setting register		PCSR10	W
00058B$_H$	PPG10 - Period setting register			W
00058C$_H$	PPG10 - Duty cycle register		PDUT10	W
00058D$_H$	PPG10 - Duty cycle register			W
00058E$_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
00058F$_H$	PPG10 - Control status register High	PCNH10		R/W
000590$_H$	PPG11 - Timer register		PTMR11	R
000591$_H$	PPG11 - Timer register			R
000592$_H$	PPG11 - Period setting register		PCSR11	W
000593$_H$	PPG11 - Period setting register			W
000594$_H$	PPG11 - Duty cycle register		PDUT11	W
000595$_H$	PPG11 - Duty cycle register			W
000596$_H$	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597$_H$	PPG11 - Control status register High	PCNH11		R/W
000598$_H$	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599$_H$	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A$_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 16MHz, CLKP2 = 8MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped)	+25˚C	15	20	mA	
			+125˚C	16.5	23.5		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 32MHz, CLKP2 = 16MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25˚C	24	30	mA	
			+125˚C	26	34		
		PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz 0 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25˚C	28	40	mA	
			+125˚C	30	44		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz, CLKP2 = 28MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	41	52	mA	
			+125˚C	43	56		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	44	58	mA	
			+125˚C	46	62		

Internal Clock timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	88	0	96	MHz	MB96F326
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	

I²C Timing

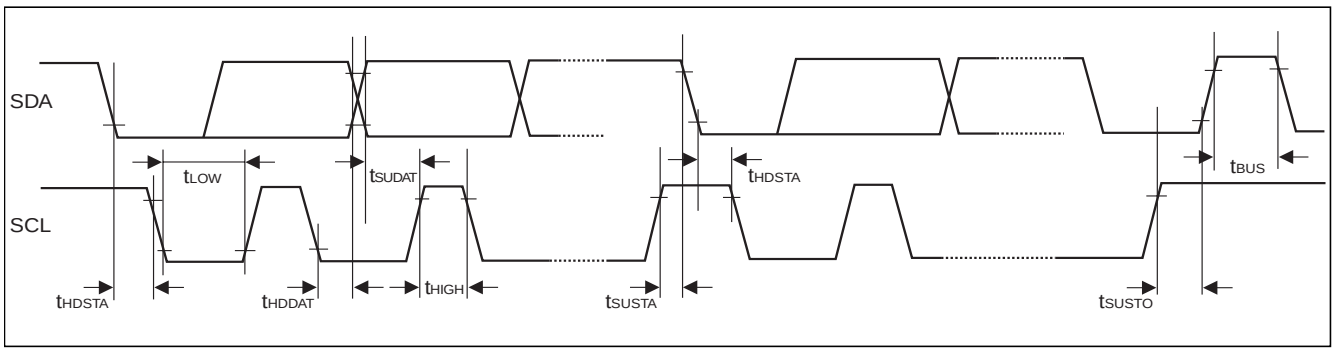
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} =0V)

Parameter	Symbol	Standard-mode		Fast-mode*1		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	—	0.6	—	µs
“L” width of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
“H” width of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	—	1.3	—	µs
Output fall time from 0.7*Vcc to 0.3*Vcc with a bus capacitance from 10 pF to 400 pF	t_{of}	20 + 0.1*C_b *2	250	20 + 0.1*C_b *2	250	ns
Capacitive load for each bus line	C_b	—	400	—	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	n/a	n/a	0	1*t_{CLKP1}*3	ns

*1 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

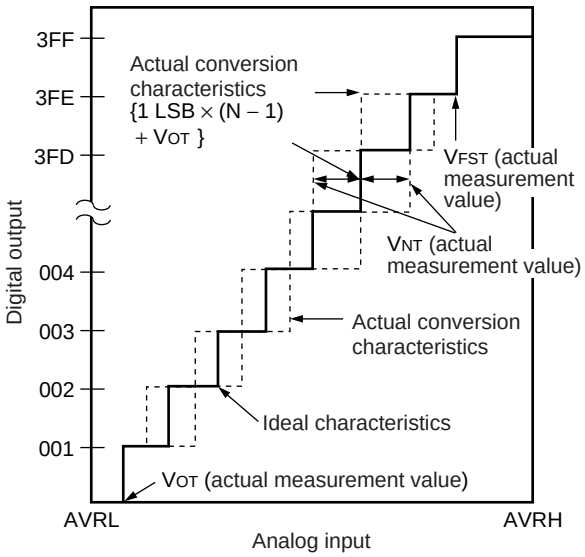
*2 : C_b = capacitance of one bus line in pF.

*3 : t_{CLKP1} is the cycle time of the periperal clock CLKP1.

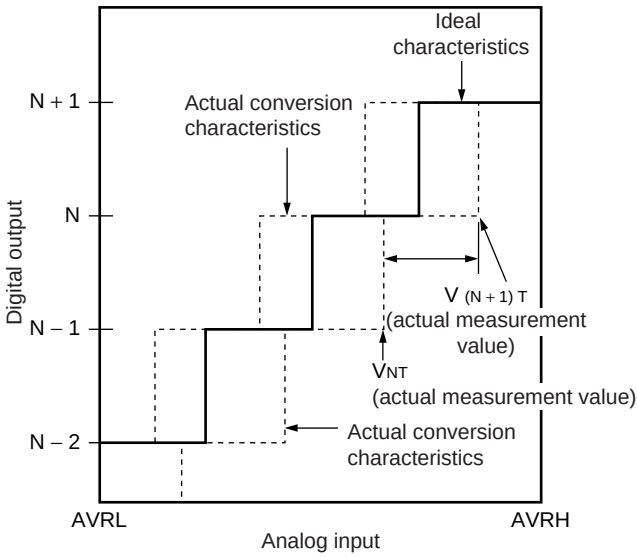


- V_{OH} = 0.7 * V_{CC}
- V_{OL} = 0.3 * V_{CC}
- CMOS Hysteresis 0.7/0.3 input selected

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times\ (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

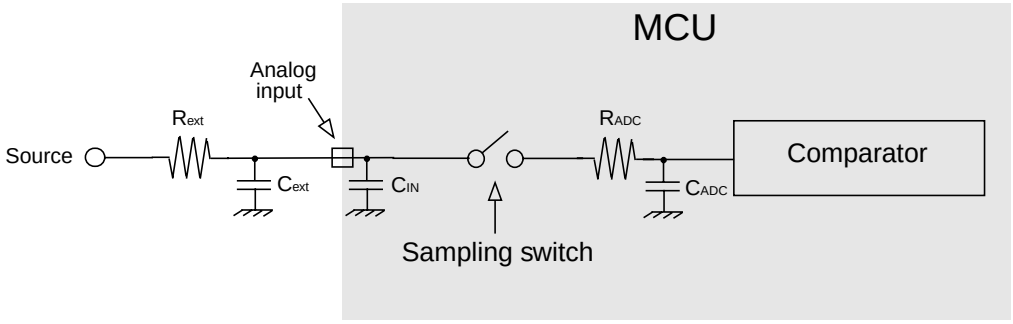
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{cc} voltage level. The following replacement model can be used for the calculation:



R_{ext}: external driving impedance
C_{ext}: capacitance of PCB at A/D converter input
C_{IN}: capacitance of MCU input pin: 15pF (max)
R_{ADC}: resistance within MCU: 2.6kΩ (max) for $4.5V \le AV_{cc} \le 5.5V$
12kΩ (max) for $3.0V \le AV_{cc} < 4.5V$
C_{ADC}: sampling capacitance within MCU: 10pF (max)

The sampling time should be set to minimum “7τ“. The following approximation formula for the replacement model above can be used:

$$T_{samp}\ [min] = 7 \times (R_{ext} \times (C_{ext} + C_{IN}) + (R_{ext} + R_{ADC}) \times C_{ADC})$$

- Do not select a sampling time below the absolute minimum permitted value (0.5µs for $4.5V \le AV_{cc} \le 5.5V$; 1.2 µs for $3.0V \le AV_{cc} < 4.5V$).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin. In this case the internal sampling capacitance C_{ADC} will be charged out of this external capacitance.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

6. Low Voltage Detector characteristics

(T_A = -40 ˚C to +125 ˚C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	V	CILCR:LVL[3:0]=”0000”
Level 1	V_{DL1}	2.9	3.1	V	CILCR:LVL[3:0]=”0001”
Level 2	V_{DL2}	3.1	3.3	V	CILCR:LVL[3:0]=”0010”
Level 3	V_{DL3}	3.5	3.75	V	CILCR:LVL[3:0]=”0011”
Level 4	V_{DL4}	3.6	3.85	V	CILCR:LVL[3:0]=”0100”
Level 5	V_{DL5}	3.7	3.95	V	CILCR:LVL[3:0]=”0101”
Level 6	V_{DL6}	3.8	4.05	V	CILCR:LVL[3:0]=”0110”
Level 7	V_{DL7}	3.9	4.15	V	CILCR:LVL[3:0]=”0111”
Level 8	V_{DL8}	4.0	4.25	V	CILCR:LVL[3:0]=”1000”
Level 9	V_{DL9}	4.1	4.35	V	CILCR:LVL[3:0]=”1001”
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	not used			
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of “Level 0” (V_{DL0_MIN}). The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

7. FLASH memory program/erase characteristics

(T_A = -40˚C to 105˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10 000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85ºC)

■ EXAMPLE CHARACTERISTICS

1. Temperature dependency of power supply currents

The following diagrams show the current consumption of samples with typical wafer process parameters in different operation modes.

Common condition for all operation modes:
- V_{CC} = AV_{CC} = 5.0V
- Main clock = 4MHz external clock
- Sub clock = 32kHz external clock

Operation mode details:

Mode name	Details
PLL Run 56	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = 56MHz • f_{CLKP2} = 28MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 2 Flash/ROM wait states (MTCRA=$233A_H$) • RC oscillator and Sub oscillator stopped
PLL Run 48	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 96MHz • f_{CLKB} = f_{CLKP1} = 48MHz • f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 1 Flash/ROM wait states (MTCRA=$6B09_H$) • RC oscillator and Sub oscillator stopped
PLL Run 24	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 48MHz • f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 0 Flash/ROM wait states (MTCRA=2208_H) • RC oscillator and Sub oscillator stopped
Main Run	Main Run mode current I_{CCMAIN} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 4MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, RC oscillator and Sub oscillator stopped

Mode name	Details
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 2MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Sleep	Sub Sleep mode current I_{CCSSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 4MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2}$ = 2MHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMSS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • PLL, RC oscillator and Main oscillator stopped