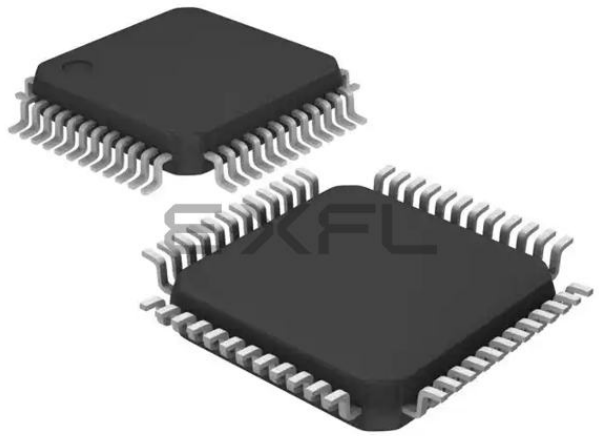

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano103ld3an

LIST OF TABLES

2 FEATURES

- Low Supply Voltage Range: 1.8V to 3.6V
- Operating Temperature: -40℃~105℃
- Four power modes
  - Normal mode
  - Idle mode
  - Power-down mode with RTC on and RAM retention
  - RTC domain only
- Wake-up sources
  - RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- Fast wake-up from power-down mode: less than 3.5 μs when using HIRC0
- Brown-out
  - Built-in 1.7~3.1V BOD for wide operating voltage range operation
  - Built-in low power 2.0/2.5V BOD
- Core
  - ARM® Cortex®-M0 core running up to 36 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - 64 Kbytes application program memory (APROM)
  - 4 Kbytes in system programming (ISP) loader program memory (LDROM)
  - 512 bytes security protection memory (SPROM)
  - 1 Kbytes key protection memory (KPROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 16 Kbytes embedded SRAM
  - Supports DMA mode
- DMA: Supports Five channels includingfour PDMA channels and one CRC channel
  - PDMA
    - Three modes: peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Source address and destination address must be word alignment in all modes.

- Memory-to-memory mode: transfer length must be word alignment.
- Peripheral-to-memory and memory-to-peripheral mode: transfer length could be word/half-word/byte alignment.
- Peripheral-to-memory and memory-to-peripheral mode: transfer data width could be word/half-word/byte alignment
- Supports source and destination address direction: increment, fixed, and wrap around

- CRC
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Built-in 12/16MHz OSC (HIRC0) has 2 % deviation within all temperarure range. Deviation could be reduced to 1% if turning on auto-trim function.
  - Built-in 36MHz OSC(HIRC1)
  - Built-in 4MHz OSC(MIRC)
  - Supports one PLL, up to 36 MHz, for high performance system operation
  - External 4~24 MHz(HXT) crystal input for precise timing operation
  - Low power 10 kHz OSC(LIRC) for watchdog and low power system operation
  - External 32.768 kHz(LXT) crystal input for RTC and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports input 5V tolerance, except
    - PA.0 ~ PA.7 (sharing pin with ADC),
    - PA.12~ PA.13 (sharing pin with comparator),
    - PF.0~ PF.1 and PF.6 ~ PF.7(sharing pin with HXT and LXT)
    - PA.8, PB.4 and PB.5
- Timer
  - Supports 4 sets of 32-bit timers, each timer with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Each timer could have independent clock source selection

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12/16 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NTC	Negative Temperature Coefficient
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PT1000	Thermal Resistance
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 4.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® Nano103 Series Selection Code

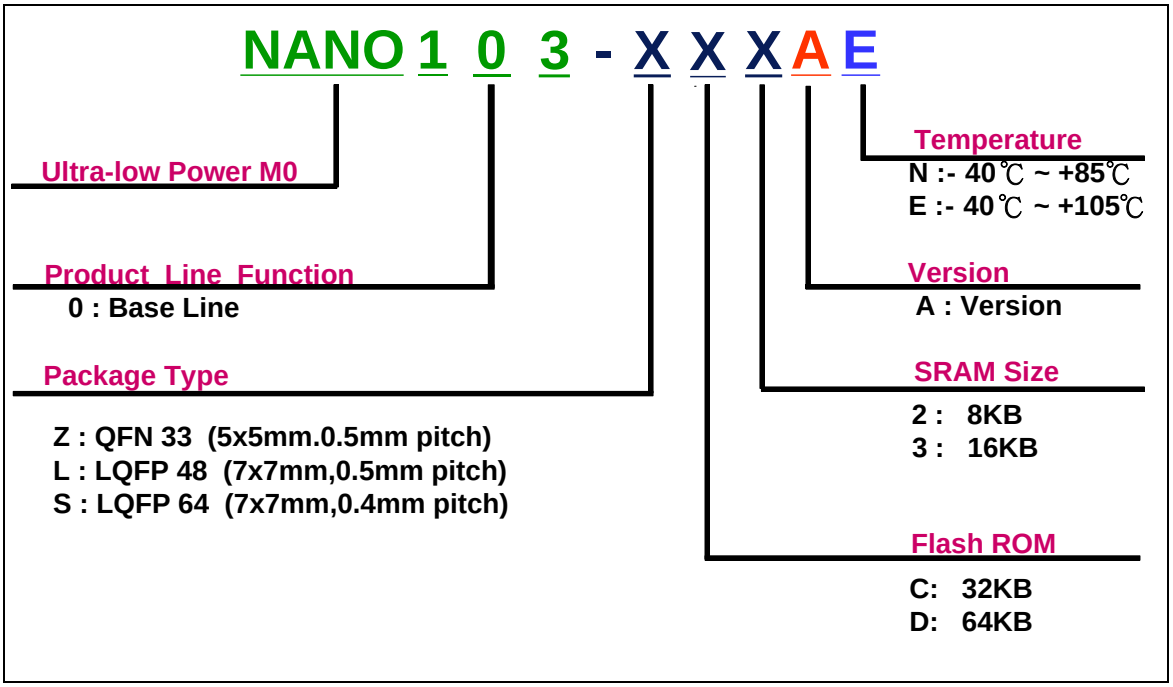


Figure 4.1-1 NuMicro® Nano103 Series Selection Code

4.2 NuMicro® Nano103 Products Selection Guide

Part No.	Flash	SRAM	Data Flash Shared AP ROM	SPROM (Security Protection)	KPROM (Key Protection)	LDROM (ISP Loader)	I/O	Timer	Connectivity			I²S	PWM	12-Bit ADC	ACMP	RTC	IRC 10KHz 4MHz 12/16MHz 36MHz	PDMA	Smart Card	ISP/ICP	Package
									UART	SPI	I²C										
NANO103ZD3AE	64K	16K	Configurable	0.5K	1K	4K	26	4x32-bit	2	4	2	-	2	6	1	V	V	4	2	V	QFN33
NANO103LD3AE	64K	16K	Configurable	0.5K	1K	4K	39	4x32-bit	2	4	2	-	6	8	1	V	V	4	2	V	LQFP48
NANO103SD3AE	64K	16K	Configurable	0.5K	1K	4K	53	4x32-bit	2	4	2	-	6	8	1	V	V	4	2	V	LQFP64

4.3.1.2 NuMicro® Nano103 LQFP 48-pin

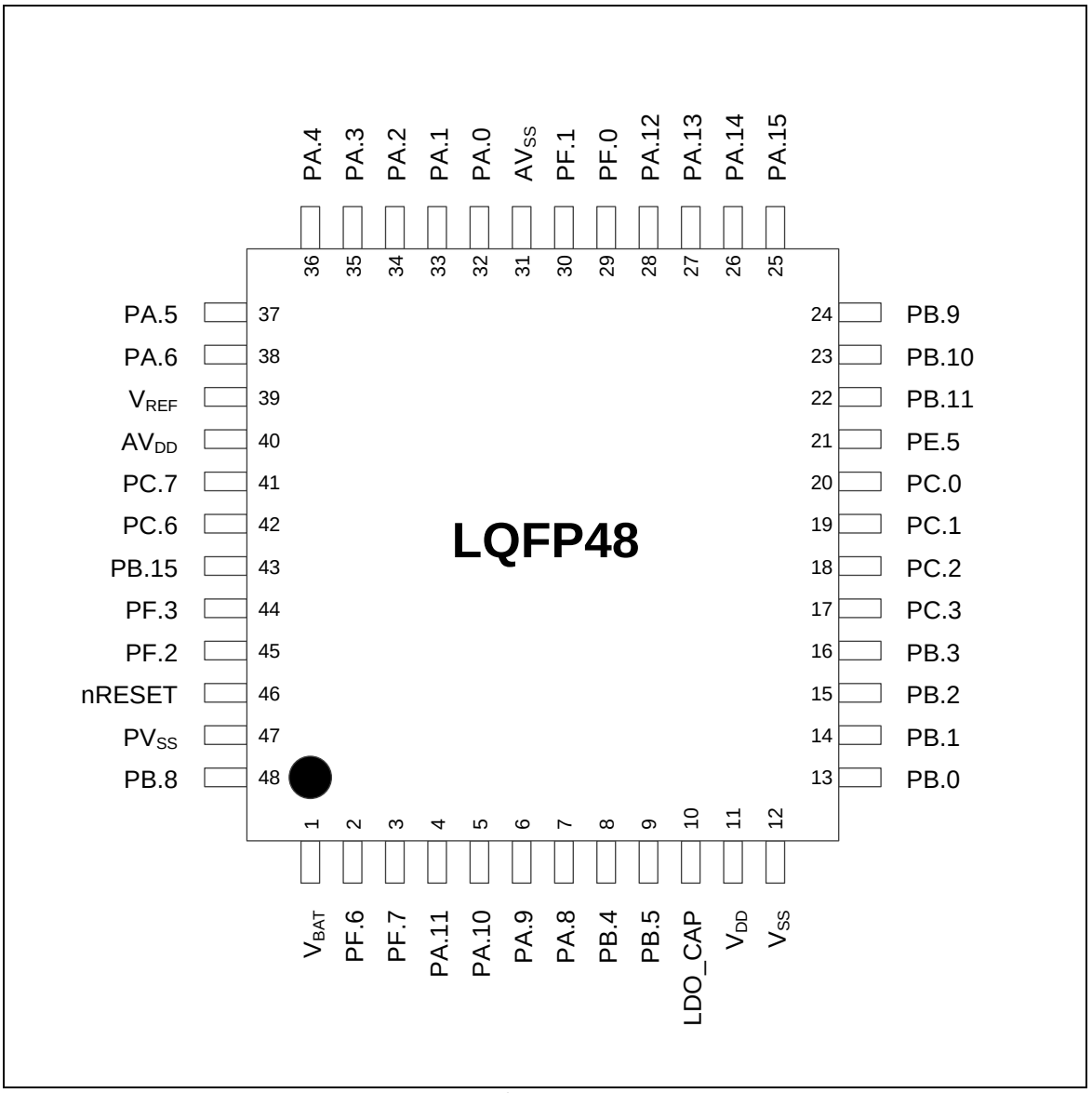


Figure 4.3-2 NuMicro® Nano103 LQFP 48-pin Diagram

- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of power modes, wake-up sources, power architecture, reset sources, scalable LDO, system memory map, product ID and multi-function pin control.

6.2.2 Features

- Power modes and wake-up sources
- System power architecture
- Reset sources
- Scalable LDO
- HIRC0, HIRC1, and MIRC Auto-trim
- System memory map
- System manager Control registers map
- System timer (SysTick)
- System control register
- Nested vectored interrupt controller(NVIC)

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[6]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), 12~16 MHz internal high speed RC oscillator (HIRC0), 36 MHzinternal high speed RC oscillator (HIRC1), and 4 MHz internal medium speed RC oscillator (MIRC) to reduce the overall system power consumption. The following figure shows the clock generator and the overview of the clock source control.

The clock controller consists of 7 sources as listed below:

- 32768 Hz external low speedcrystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- 12~16 MHz internal high speed RC oscillator (HIRC0)
- 36 MHz internal high speed RC oscillator (HIRC1)
- 4 MHz internal medium speed RC oscillator (MIRC)
- One programmable PLL FOUT (PLL source can be selected from HXT, HIRC0,HIRC1 or MIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

6.3.2 Features

- Generates clocks for system clocks and all peripheral module clocks.
- Each peripheral module clock can be turned on/off.
- In Power-down mode, the clock controller turns off the external high speed crystal (HXT) and internal high speed RC oscillator (HIRC0,HIRC1 and MIRC) to reduce the overall system power consumption.

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controllerin the Nano103 series contains a four-channel DMA controller and a cyclic redundancy check (CRC) generator.

The PDMA controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 4 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

The PDMA controller also contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU mode and DMA transfer mode.

6.6.2 Features

- Supports 4 independently configurable channels and 1 CRC channel
- Supports hardware round robin priority scheme. PDMA channel 1 has the highest priority and channel 4 has the lowest priority
- PDMA
  - Supports transfer data width of 8, 16, or 32 bits
  - Supports software and SPI, UART, TIMER and ADC request
  - Supports source and destination address increment size can be byte, half-word, word, no increment or wrap around
  - Supports periodic transfer count interrupt
  - Supports time-out function for each channel
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8:$X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - Programmable seed value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum
  - Supports CPU mode or DMA transfer mode
  - Supports transfer data width of 8, 16, or 32 bits in CRC CPU mode
    - 8-bit write mode: 1-AHB clock cycle operation
    - 16-bit write mode: 2-AHB clock cycle operation
    - 32-bit write mode: 4-AHB clock cycle operation
  - Supports transfer data width of 8 bits in CRC DMA mode

6.11 Real Time Clock (RTC)

6.11.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick andalarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

The RTC controller also offers 20 bytes spare registers to store user's important information. The spare registers content is cleared when specified event on tamper pin is detected.

6.11.2 Features

- Supportsreal time counterin RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year,month, day) for RTC time and calendar check
- Supportsalarm time (hour, minute, second) and calendar (year,month, day) settings in RTC_TALM and RTC_CALM
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counterin RTC_WEEKDAY register
- Frequency of RTC clock source compensateby RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated
- Supports 20 bytes spare registers and a tamper pin detection to clear the content of these spare registers
- Support independent V_{BAT} power domain to provide for PF.6~PF.7 (sharing pin with LXT) and tamper pins (LQFP64: PB.13/LQFP48: PA.9/QFN32: PB.8)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
V_{LDO}=1.8 V	I_{DD56}	-	6.8	-	mA	1.8 V	X	4 MHz	V	V
	I_{DD57}	-	3.4	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD58}	-	6.5	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	16 MHz	X	X	V
	I_{DD59}	-	3.3	-	mA	3.6 V	16 MHz	X	X	X
	I_{DD60}	-	6.3	-	mA	1.8 V	16 MHz	X	X	V
	I_{DD61}	-	3.3	-	mA	1.8 V	16 MHz	X	X	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.8 V	I_{DD62}	-	6.5	-	mA	3.6 V	12 MHz	X	V	V
	I_{DD63}	-	3.4	-	mA	3.6 V	12 MHz	X	V	X
	I_{DD64}	-	6.4	-	mA	1.8 V	12 MHz	X	V	V
	I_{DD65}	-	3.4	-	mA	1.8 V	12 MHz	X	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.8 V	I_{DD66}	-	6.3	-	mA	3.6 V	4 MHz	X	V	V
	I_{DD67}	-	3.1	-	mA	3.6 V	4 MHz	X	V	X
	I_{DD68}	-	6.3	-	mA	1.8 V	4 MHz	X	V	V
	I_{DD69}	-	3.1	-	mA	1.8 V	4 MHz	X	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD70}	-	6.8	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	X	16 MHz	X	V
	I_{DD71}	-	3.1	-	mA	3.6 V	X	16 MHz	X	X
	I_{DD72}	-	6.7	-	mA	1.8 V	X	16 MHz	X	V
	I_{DD73}	-	3.1	-	mA	1.8 V	X	16 MHz	X	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.8 V	I_{DD74}	-	7	-	mA	3.6 V	X	12 MHz	V	V
	I_{DD75}	-	3.3	-	mA	3.6 V	X	12 MHz	V	X
	I_{DD76}	-	6.8	-	mA	1.8 V	X	12 MHz	V	V
	I_{DD77}	-	3.2	-	mA	1.8 V	X	12 MHz	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD78}	-	6.2	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	X	4 MHz	V	V
	I_{DD79}	-	3.1	-	mA	3.6 V	X	4 MHz	V	X
	I_{DD80}	-	6.1	-	mA	1.8 V	X	4 MHz	V	V
	I_{DD81}	-	3.1	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash	I_{DD82}	-	4.9	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	12 MHz	X	X	V
	I_{DD83}	-	2.5	-	mA	3.6 V	12 MHz	X	X	X

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	$I_{IDLE179}$	-	2.9	-	mA	1.8 V	X	4 MHz	V	V
	$I_{IDLE180}$	-	0.9	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Idle Mode HCLK =4 MHz V_{LDO}=1.6 V	$I_{IDLE181}$	-	0.8	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	4 MHz	X	X	V
	$I_{IDLE182}$	-	0.4	-	mA	3.6 V	4 MHz	X	X	X
	$I_{IDLE183}$	-	0.8	-	mA	1.8 V	4 MHz	X	X	V
	$I_{IDLE184}$	-	0.4	-	mA	1.8 V	4 MHz	X	X	X
Operating Current Idle Mode HCLK =4 MHz V_{LDO}=1.6 V	$I_{IDLE185}$	-	1.1	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	X	4 MHz	V	V
	$I_{IDLE186}$	-	0.4	-	mA	3.6 V	X	4 MHz	V	X
	$I_{IDLE187}$	-	1.1	-	mA	1.8 V	X	4 MHz	V	V
	$I_{IDLE188}$	-	0.4	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Idle Mode HCLK =32.768 kHz V_{LDO}=1.6 V	$I_{IDLE189}$	-	143	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module
						3.6 V	32.768 kHz	X	X	V
	$I_{IDLE190}$	-	138	-	uA	3.6 V	32.768 kHz	X	X	X
	$I_{IDLE191}$	-	120	-	uA	1.8 V	32.768 kHz	X	X	V
	$I_{IDLE192}$	-	115	-	uA	1.8 V	32.768 kHz	X	X	X
Operating Current Idle Mode HCLK =10 kHz V_{LDO}=1.6 V	$I_{IDLE193}$	-	138	-	uA	3.6 V	X	10 kHz	X	V
	$I_{IDLE194}$	-	136	-	uA	3.6 V	X	10 kHz	X	X
	$I_{IDLE195}$	-	116	-	uA	1.8 V	X	10 kHz	X	V
	$I_{IDLE196}$	-	114	-	uA	1.8 V	X	10 kHz	X	X
Operating Current Idle Mode HCLK =2 MHz V_{LDO}=1.2 V	$I_{IDLE197}$	-	0.7	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	4 MHz	X	X	V
	$I_{IDLE198}$	-	0.4	-	mA	3.6 V	4 MHz	X	X	X
	$I_{IDLE199}$	-	0.7	-	mA	1.8 V	4 MHz	X	X	V
	$I_{IDLE200}$	-	0.4	-	mA	1.8 V	4 MHz	X	X	X
Operating Current Idle Mode HCLK =2 MHz V_{LDO}=1.2 V	$I_{IDLE201}$	-	0.7	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	X	4 MHz	X	V
	$I_{IDLE202}$	-	0.3	-	mA	3.6 V	X	4 MHz	X	X
	$I_{IDLE203}$	-	0.7	-	mA	1.8 V	X	4 MHz	X	V
	$I_{IDLE204}$	-	0.3	-	mA	1.8 V	X	4 MHz	X	X
Operating Current	$I_{IDLE205}$	-	215	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module

Hysteresis voltage of PA~PF (Schmitt input)	V_{HY}	-	$0.4*V_{DD}$	-	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-	-	$0.3*V_{DD}$	V	V_{DD} = 3.3V
Positive going threshold (Schmitt Input), /RESET	V_{IHS}	$0.7*V_{DD}$	-	-	V	V_{DD} = 3.3V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-	-18	-	mA	V_{DD} = 3.3V, V_S = 2.4V
	I_{SR22}	-	-2.5	-	mA	V_{DD} = 1.8V, V_S = 1.6V
Sink Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SK21}	-	12	-	mA	V_{DD} = 3.3V, V_S = 0.45V
	I_{SK22}	-	6	-	mA	V_{DD} = 1.8V, V_S = 0.45V

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
4. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.
5. All peripherals' clock source is from HXT (12 MHz), except SPI from HCLK.
6. The Operating Current (Normal Run Mode and Idle Mode) test condition is enable LVR and Clock filter.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-	-	nS	
Clock Low Time	t_{CLCX}	10	-	-	nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	

9.4 Analog Characteristics

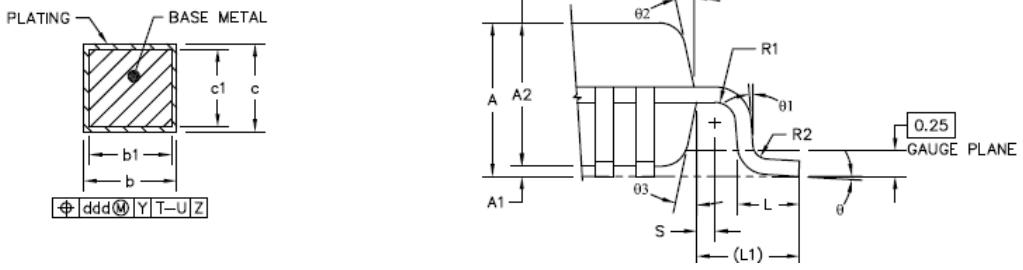
9.4.1 12-bit ADC

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	1.8	-	3.6	V	$AV_{DD} = V_{DD}$
Operating current (AV_{DD} current)	I_{ADC32}	-	125	-	μA	$AV_{DD} = V_{DD} = 3.6V$ $ADC\_VREF = AV_{DD}$ ADC Clock Rate = 36 MHz
(Enable ADC and disable all other analog modules)	I_{ADC2}	-	20	-	μA	$AV_{DD} = V_{DD} = 3.6V$ $ADC\_VREF = AV_{DD}$ ADC Clock Rate = 6 MHz
Resolution	R_{ADC}	-	-	12	Bit	
Reference voltage	V_{REF}	1.8	-	A_{VDD}	V	
Reference input current (Avg.)	I_{REF}	-	-	1	μA	
ADC input voltage	V_{IN}	0	-	V_{REF}	V	
Conversion time	T_{CONV}	1	-	-	μS	
Conversion Rate	F_{SPS}	-	-	1.8M	Hz	$V_{DD} = 3.6V$
Integral Non-Linearity Error	INL	-	±1	-	LSB	V_{REF} is external Vref pin
Differential Non-Linearity	DNL	-	±0.8	-	LSB	V_{REF} is external Vref pin
Gain error	E_G	-	±2	-	LSB	V_{REF} is external Vref pin
Offset error	E_{OFFSET}	-	±1.5	-	LSB	V_{REF} is external Vref pin
Absolute error	E_{ABS}	-	-	±6	LSB	V_{REF} is external Vref pin
ADC Clock frequency	F_{ADC}	0.25	-	36	MHz	
Clock cycle	AD_{CYC}	20	-	-	Cycle	
Internal Capacitance	C_{IN}	-	5	-	pF	
Monotonic	-	Guaranteed			-	

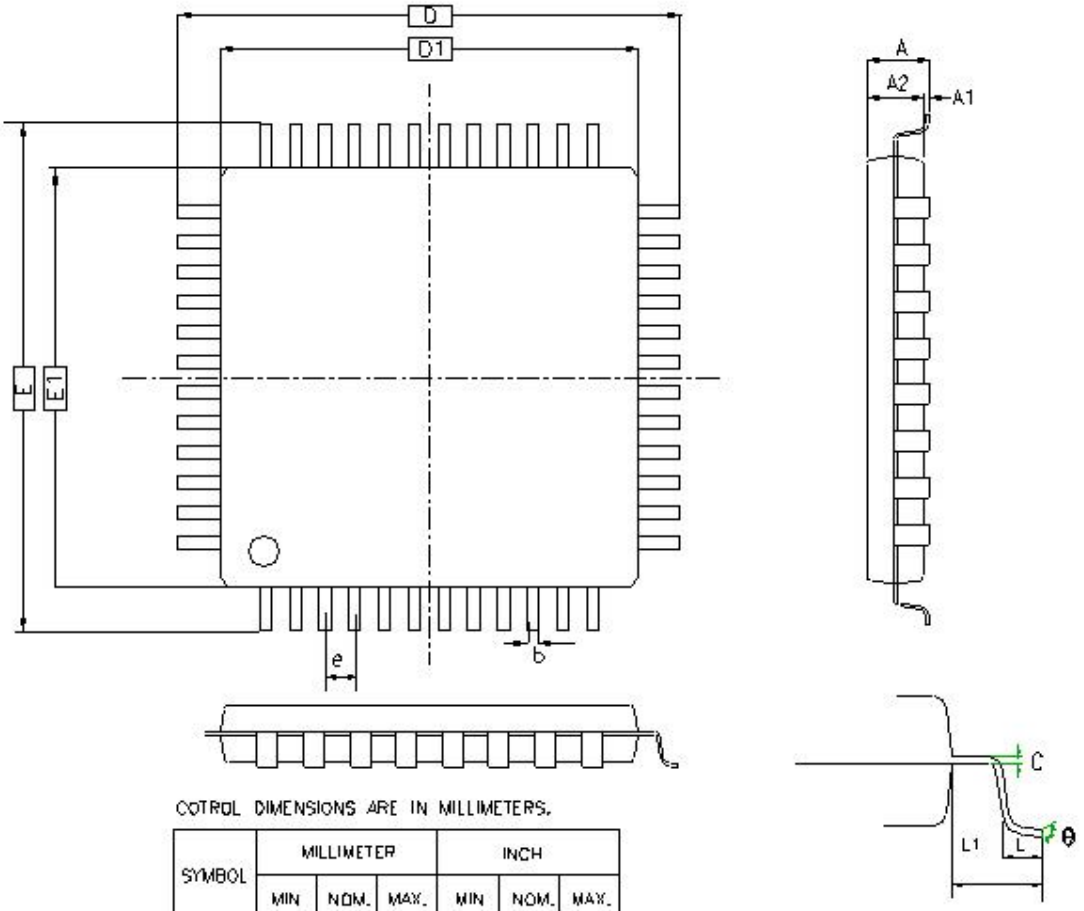
9.4.2 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	3.6	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	40	-	μA	AV_{DD} = 3.6V
I_{LPBOD}	Quiescent Current	-	0.5	-	μA	AV_{DD} = 3.6V
V_{BOD}	Brown-out Voltage 25℃	1.75	1.8	1.79	V	BODCTL[15:12] = 0001
		1.84	1.9	1.89	V	BODCTL[15:12] = 0010
		1.94	2.0	1.99	V	BODCTL[15:12] = 0011
		2.04	2.1	2.09	V	BODCTL[15:12] = 0100
		2.14	2.2	2.19	V	BODCTL[15:12] = 0101
		2.23	2.3	2.29	V	BODCTL[15:12] = 0110
		2.33	2.4	2.39	V	BODCTL[15:12] = 0111
		2.43	2.5	2.49	V	BODCTL[15:12] = 1000
		2.53	2.6	2.59	V	BODCTL[15:12] = 1001
		2.62	2.7	2.69	V	BODCTL[15:12] = 1010
		2.72	2.8	2.79	V	BODCTL[15:12] = 1011
		2.82	2.9	2.89	V	BODCTL[15:12] = 1100
		2.92	3	2.99	V	BODCTL[15:12] = 1101
		3.02	3.1	3.09	V	BODCTL[15:12] = 1110
V_{LPBOD}	Low Power Mode Brown-out Voltage 25℃	2.01	2.0	2.07	V	BODCTL[9] = 0
		2.42	2.5	2.79	V	BODCTL[9] = 1

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



10.2 48L LQFP (7x7x1.4 mm footprint 2.0 mm)



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

10.3 33L QFN (5x5x1.4 mm footprint 2.0 mm)