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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano103sd3an

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1 GENERAL DESCRIPTION

The Nano103 series ultra-low-power 32-bit microcontroller embeded with ARM® Cortex®-M0 core operates at low voltage ranged from 1.8V to 3.6V and runs up to 36 MHz frequency with 64 Kbytes embedded Flash(APROM) and 16 Kbytes embedded SRAM and 4 Kbytes Flash loader memory(LDROM) for In-System Programming (ISP). In additon, Nano103 include special 512 bytes security protection memory (SPROM) and 1 Kbytes key protection memory (KPROM) to enhance the security and protection of customer application.

The Nano103 series integrates RTC with independent V_{BAT} pin, 12-bit SAR ADC, comparator and provides high performance connectivity peripheral interfaces such as UART, SPI, I^2C, GPIOs, and ISO-7816-3 for Smart card.

The Nano103 series supports main power off with only V_{BAT} and RTC on less than 1.0 uA and Deep Power-down mode with RAM retention is less than 1.6 uA and fast wake-up via many peripheral interfaces.

The Nano103 series provides low voltage, low operating power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano103 series is suitable for a wide range of battery device applications such as:

- Hand-Held Medical Device
- Wearable Device & Smart Watch
- Wireless Gaming Control, Thermostats, Sensors Node Device (WSND)
- Wireless Auto Meter Reading (AMR)
- RFID Reader
- Portable Wireless Data Collector
- Mobile Payment Smart Card Reader
- Security Alarm System
- Smart Home Appliance
- Smart Water, Gas, Heat Meters

Product Line	SPROM	KPROM	UART	SPI	I^2C	ADC	ACMP	RTC/V_{bat}	SC	Timer
Nano103	●	●	●	●	●	●	●	●	●	●

Table 4.1-1 Connectivity Support Table

- Memory-to-memory mode: transfer length must be word alignment.
- Peripheral-to-memory and memory-to-peripheral mode: transfer length could be word/half-word/byte alignment.
- Peripheral-to-memory and memory-to-peripheral mode: transfer data width could be word/half-word/byte alignment
- Supports source and destination address direction: increment, fixed, and wrap around

- CRC
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Built-in 12/16MHz OSC (HIRC0) has 2 % deviation within all temperarure range. Deviation could be reduced to 1% if turning on auto-trim function.
  - Built-in 36MHz OSC(HIRC1)
  - Built-in 4MHz OSC(MIRC)
  - Supports one PLL, up to 36 MHz, for high performance system operation
  - External 4~24 MHz(HXT) crystal input for precise timing operation
  - Low power 10 kHz OSC(LIRC) for watchdog and low power system operation
  - External 32.768 kHz(LXT) crystal input for RTC and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports input 5V tolerance, except
    - PA.0 ~ PA.7 (sharing pin with ADC),
    - PA.12~ PA.13 (sharing pin with comparator),
    - PF.0~ PF.1 and PF.6 ~ PF.7(sharing pin with HXT and LXT)
    - PA.8, PB.4 and PB.5
- Timer
  - Supports 4 sets of 32-bit timers, each timer with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Each timer could have independent clock source selection

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® Nano103 Series Selection Code

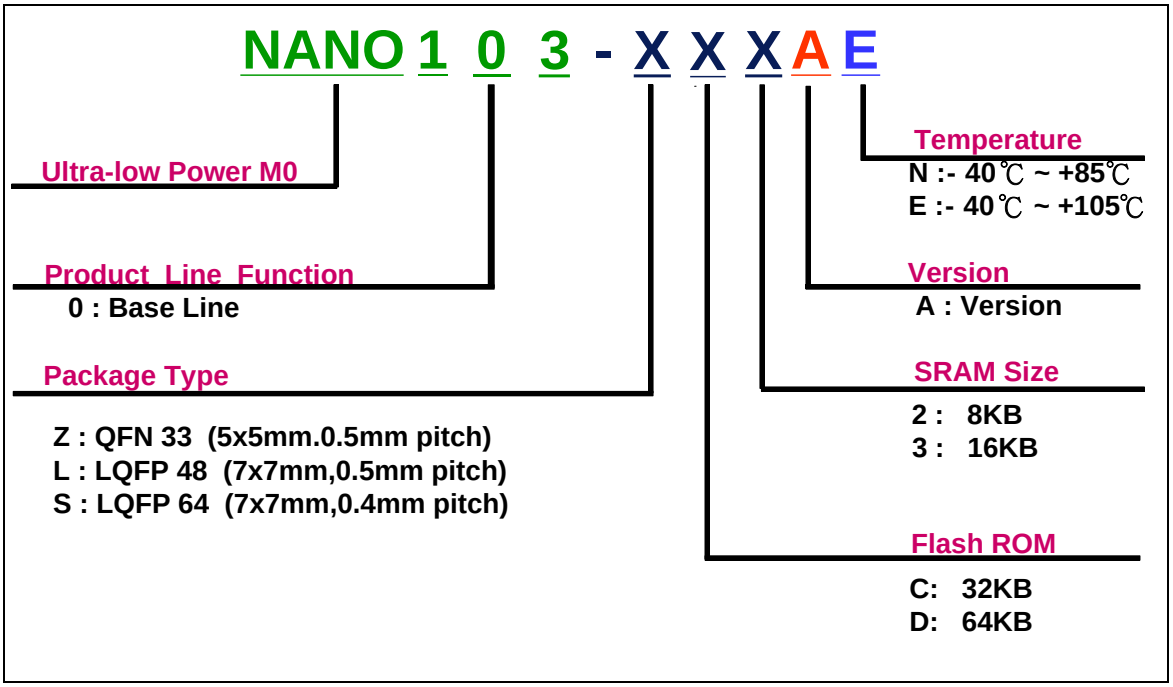

Figure 4.1-1 NuMicro® Nano103 Series Selection Code

4.2 NuMicro® Nano103 Products Selection Guide

Part No.	Flash	SRAM	Data Flash Shared AP ROM	SPROM (Security Protection)	KPROM (Key Protection)	LDROM (ISP Loader)	I/O	Timer	Connectivity			I²S	PWM	12-Bit ADC	ACMP	RTC	IRC 10KHz 4MHz 12/16MHz 36MHz	PDMA	Smart Card	ISP/ICP	Package
									UART	SPI	I²C										
NANO103ZD3AE	64K	16K	Configurable	0.5K	1K	4K	26	4x32-bit	2	4	2	-	2	6	1	V	V	4	2	V	QFN33
NANO103LD3AE	64K	16K	Configurable	0.5K	1K	4K	39	4x32-bit	2	4	2	-	6	8	1	V	V	4	2	V	LQFP48
NANO103SD3AE	64K	16K	Configurable	0.5K	1K	4K	53	4x32-bit	2	4	2	-	6	8	1	V	V	4	2	V	LQFP64

4.3.1.2 NuMicro® Nano103 LQFP 48-pin

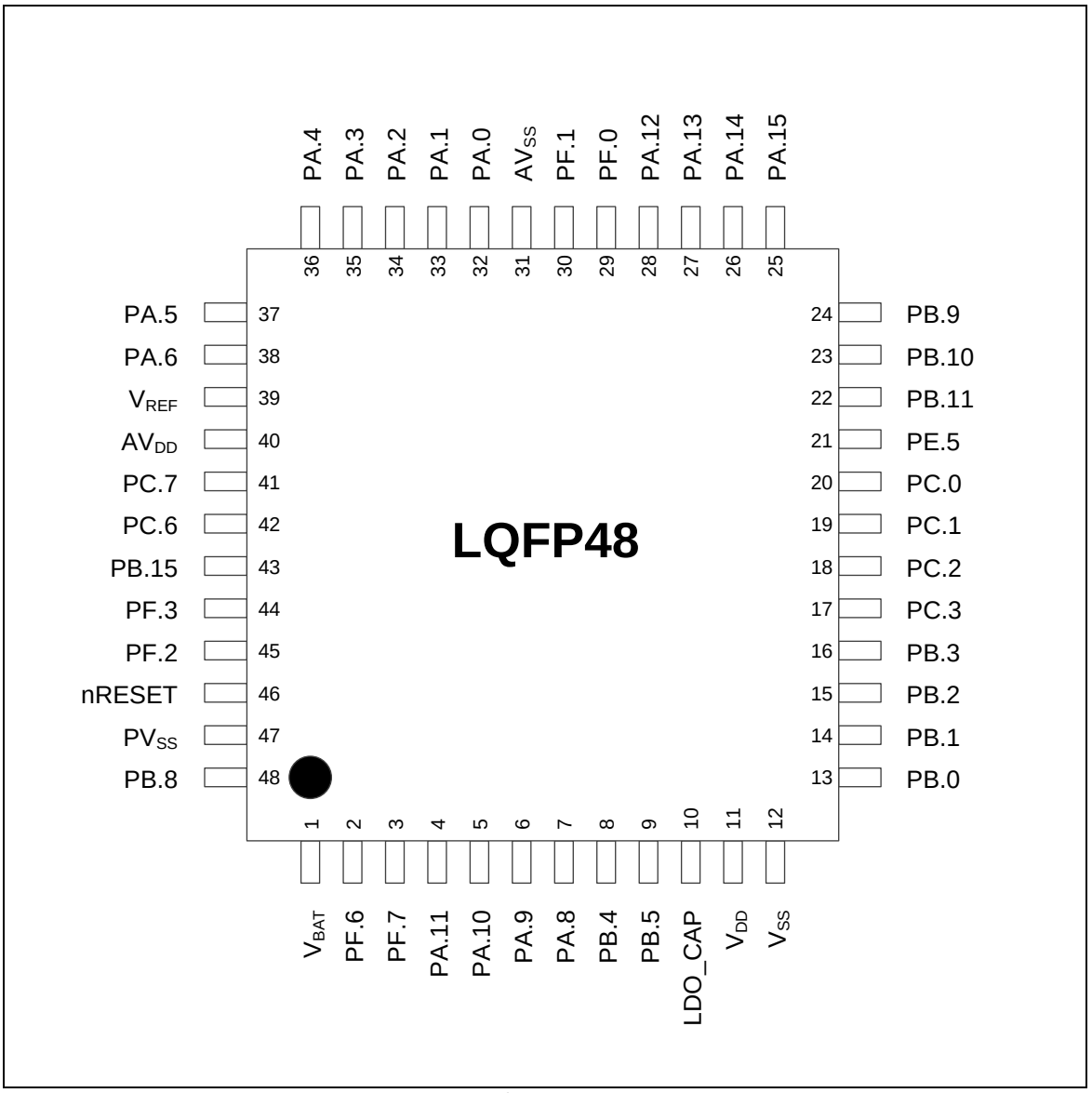

Figure 4.3-2 NuMicro® Nano103 LQFP 48-pin Diagram

4.3.1.3 NuMicro® Nano103 QFN33-pin

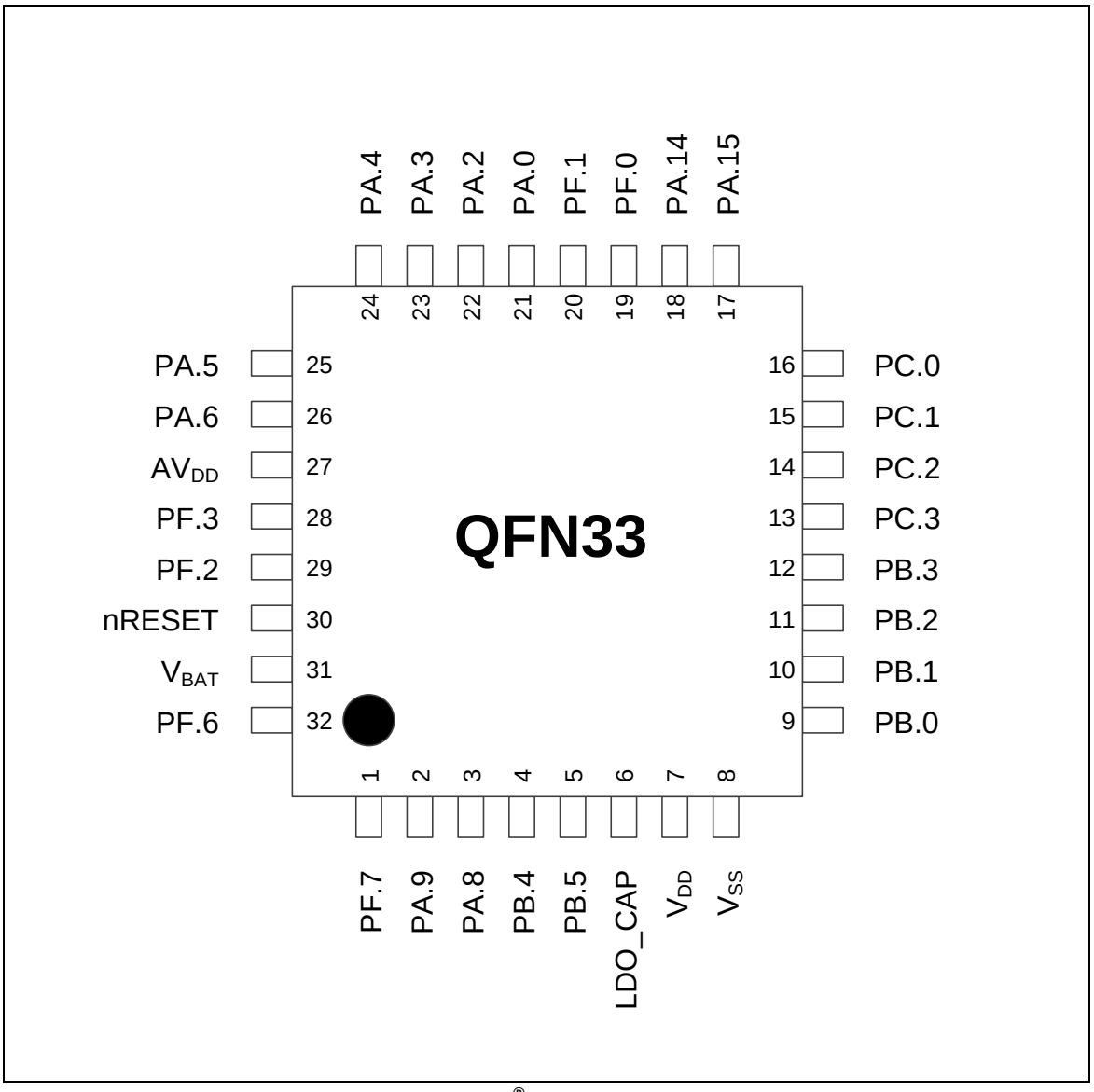

Figure 4.3-3 NuMicro® Nano103 QFN33-pin Diagram

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
			SPI0_MOSI0	I/O	MFP1	SPI0 1st MOSI (Master Out, Slave In) pin.
			SC1_RST	O	MFP4	SmartCard1 reset pin.
			PWM0_BRAKE0	I	MFP5	PWM0 Brake0 input pin .
26	18	14	PC.2	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO0	I/O	MFP1	SPI0 1st MISO (Master In, Slave Out) pin.
			SC1_PWR	O	MFP4	SmartCard1 power pin.
			PWM0_BRAKE1	I	MFP5	PWM0 Brake1 input pin.
27	19	15	PC.1	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.
			SC1_DAT	I/O	MFP4	SmartCard1 data pin.
			PWM0_BRAKE0	I	MFP5	PWM0 Brake0 input pin.
28	20	16	PC.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS0	I/O	MFP1	SPI0 1st slave select pin.
			SC1_CLK	O	MFP4	SmartCard1 clock pin.
			PWM0_BRAKE1	I	MFP5	PWM0 Brake1 input pin..
29	21	-	PE.5	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH5	I/O	MFP1	PWM0 channel5 output/capture input.
			RTC_HZ	O	MFP6	RTC 1Hz output.
30	22	-	PB.11	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH4	I/O	MFP1	PWM0 channel4 output/capture input.
			TM3_CNT	I	MFP2	Timer3 event counter input.
			TM3_OUT	O	MFP4	Timer3 toggle output.
			SPI0_MISO0	I/O	MFP5	SPI0 1st MISO (Master In, Slave Out) pin.
31	23	-	PB.10	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	MFP1	SPI0 1st MOSI (Master Out, Slave In) pin.
			TM2_CNT	I	MFP2	Timer2 event counter input.
			TM2_OUT	O	MFP4	Timer2 toggle output.
			SPI0_SS1	I/O	MFP5	SPI0 2nd slave select pin.
32	24	-	PB.9	I/O	MFP0	General purpose digital I/O pin.
			SPI1_SS1	I/O	MFP1	SPI1 1st slave select pin.
			TM1_CNT	I	MFP2	Timer1 event counter input.
			TM1_OUT	O	MFP4	Timer1 toggle output.
			INT0	I	MFP5	External interrupt0 input pin.

Pin No.			Pin Name	Pin Type	MFP*	Description
64-pin	48-pin	32-pin				
59	45	29	PF.2	I/O	MFP0	General purpose digital I/O pin.
			XT1_OUT	O	MFP7	External 4~24 MHz (high speed) crystal output pin.
60	46	30	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
61	-	-	V_{SS}	G	MFP0	Ground pin for digital circuit.
62	-	-	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital function.
63	47	-	V_{SS}	G	MFP0	Ground pin for digital circuit.
64	48	-	PB.8	I/O	MFP0	General purpose digital I/O pin.
			STADC	I	MFP1	ADC external trigger input.
			TM0_CNT	I	MFP2	Timer0 event counter input.
			INT0	I	MFP3	External interrupt0 input pin.
			TM0_OUT	O	MFP4	Timer0 toggle output.
			TAMPER	I	MFP7	Tamper pin.

Note: Pin Type: I = Digital Input, O=Digital Output; AI=Analog Input; AO= Analog Output; P=Power Pin; AP=Analog Power.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[6]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), 12~16 MHz internal high speed RC oscillator (HIRC0), 36 MHzinternal high speed RC oscillator (HIRC1), and 4 MHz internal medium speed RC oscillator (MIRC) to reduce the overall system power consumption. The following figure shows the clock generator and the overview of the clock source control.

The clock controller consists of 7 sources as listed below:

- 32768 Hz external low speedcrystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- 12~16 MHz internal high speed RC oscillator (HIRC0)
- 36 MHz internal high speed RC oscillator (HIRC1)
- 4 MHz internal medium speed RC oscillator (MIRC)
- One programmable PLL FOUT (PLL source can be selected from HXT, HIRC0,HIRC1 or MIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

6.3.2 Features

- Generates clocks for system clocks and all peripheral module clocks.
- Each peripheral module clock can be turned on/off.
- In Power-down mode, the clock controller turns off the external high speed crystal (HXT) and internal high speed RC oscillator (HIRC0,HIRC1 and MIRC) to reduce the overall system power consumption.

8 POWER COMSUMPTION

Part No	Test Condition	VDD	CPU clock	Current
Nano103 series	Operating Mode: CPU run while(1) in FLASH ROM Clock = 36MHz (from PLL and its clock source is 12 MHz Crystal Oscillator) Disable all peripheral Set LDO output = 1.8V	3.6V	36 MHz	6.7mA 186uA/MHz
	Idle Mode: CPU stop Clock = 36MHz (from PLL and its clock source is 12 MHz Crystal Oscillator) Disable all peripheral Set LDO output = 1.8V	3.6V	36 MHz	2.2mA 61uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 36MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.8V	3.6V	36 MHz	6.7mA 186uA/MHz
	Idle Mode: CPU stop Clock = 36MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.8V	3.6V	36 MHz	1.9mA 53uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 16MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V	3.6V	16 MHz	2.9mA 181uA/MHz
	Idle Mode: CPU stop Clock = 16MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V	3.6V	16 MHz	1.2mA 75uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 36MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V	3.6V	16 MHz	2.8mA 175uA/MHz
	Idle Mode: CPU stop Clock = 36MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V	3.6V	16 MHz	1.1mA 69uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V	3.6V	12 MHz	2.2mA 183uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Crystal Oscillator	3.6V	12 MHz	900uA 75uA/MHz

9 ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}-V_{SS}	-0.3	+3.6	V
Battery Power Supply	V_{BAT}-V_{SS}	-0.3	+3.6	V
Input Voltage on 5V Tolerance Pin	V_{IN}	V_{SS} -0.3	5.5	V
Input Voltage on Any Other Pin without 5V Tolerance Pin	VI_N	V_{SS} -0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}		-	150	mA
Maximum Current out of V_{SS}		-	150	mA
Maximum Current sunk by a I/O Pin		-	25	mA
Maximum Current Sourced by a I/O Pin		-	25	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

Note: Output voltage for ADC/ACMP/HXT/LXT/PA.8/PB.4/PB.5 shared pins cannot be higher than V_{DD} because these pins are without 5V tolerance.

9.2 Nano103 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 36 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation Voltage	V_{DD}	1.8	-	3.6	V	V_{DD} = 1.8V up to 36 MHz
Power Ground	V_{SS} AV_{SS}	-0.3	-	-	V	
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	MCU operating in Run, Idle or Power-down mode
		1.44	1.6	1.76	V	Set LDO_LEVEL(LDO_CTL[3:2]) = 0x1
		1.08	1.2	1.32	V	Set LDO_LEVEL(LDO_CTL[3:2]) = 0x0
	C_{LDO}	1	-	1	uF	Connect to LDO_CAP pin

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
V_{LDO}=1.8 V	I_{DD56}	-	6.8	-	mA	1.8 V	X	4 MHz	V	V
	I_{DD57}	-	3.4	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD58}	-	6.5	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	16 MHz	X	X	V
	I_{DD59}	-	3.3	-	mA	3.6 V	16 MHz	X	X	X
	I_{DD60}	-	6.3	-	mA	1.8 V	16 MHz	X	X	V
	I_{DD61}	-	3.3	-	mA	1.8 V	16 MHz	X	X	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.8 V	I_{DD62}	-	6.5	-	mA	3.6 V	12 MHz	X	V	V
	I_{DD63}	-	3.4	-	mA	3.6 V	12 MHz	X	V	X
	I_{DD64}	-	6.4	-	mA	1.8 V	12 MHz	X	V	V
	I_{DD65}	-	3.4	-	mA	1.8 V	12 MHz	X	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.8 V	I_{DD66}	-	6.3	-	mA	3.6 V	4 MHz	X	V	V
	I_{DD67}	-	3.1	-	mA	3.6 V	4 MHz	X	V	X
	I_{DD68}	-	6.3	-	mA	1.8 V	4 MHz	X	V	V
	I_{DD69}	-	3.1	-	mA	1.8 V	4 MHz	X	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD70}	-	6.8	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	X	16 MHz	X	V
	I_{DD71}	-	3.1	-	mA	3.6 V	X	16 MHz	X	X
	I_{DD72}	-	6.7	-	mA	1.8 V	X	16 MHz	X	V
	I_{DD73}	-	3.1	-	mA	1.8 V	X	16 MHz	X	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.8 V	I_{DD74}	-	7	-	mA	3.6 V	X	12 MHz	V	V
	I_{DD75}	-	3.3	-	mA	3.6 V	X	12 MHz	V	X
	I_{DD76}	-	6.8	-	mA	1.8 V	X	12 MHz	V	V
	I_{DD77}	-	3.2	-	mA	1.8 V	X	12 MHz	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD78}	-	6.2	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	X	4 MHz	V	V
	I_{DD79}	-	3.1	-	mA	3.6 V	X	4 MHz	V	X
	I_{DD80}	-	6.1	-	mA	1.8 V	X	4 MHz	V	V
	I_{DD81}	-	3.1	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash	I_{DD82}	-	4.9	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	12 MHz	X	X	V
	I_{DD83}	-	2.5	-	mA	3.6 V	12 MHz	X	X	X

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
while(1){}executed from flash V_{LDO}=1.8 V	I_{DD112}	-	118	-	uA	1.8 V	X	10 kHz	X	V
	I_{DD113}	-	116	-	uA	1.8 V	X	10 kHz	X	X
Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD114}	-	6.5	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	18 MHz	X	X	V
	I_{DD115}	-	3.4	-	mA	3.6 V	18 MHz	X	X	X
	I_{DD116}	-	6.4	-	mA	1.8 V	18 MHz	X	X	V
	I_{DD117}	-	3.3	-	mA	1.8 V	18 MHz	X	X	X
Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD118}	-	6.6	-	mA	3.6 V	16 MHz	X	V	V
	I_{DD119}	-	3.5	-	mA	3.6 V	16 MHz	X	V	X
	I_{DD120}	-	6.6	-	mA	1.8 V	16 MHz	X	V	V
	I_{DD121}	-	3.4	-	mA	1.8 V	16 MHz	X	V	X
Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD122}	-	6.5	-	mA	3.6 V	12 MHz	X	V	V
	I_{DD123}	-	3.3	-	mA	3.6 V	12 MHz	X	V	X
	I_{DD124}	-	6.4	-	mA	1.8 V	12 MHz	X	V	V
	I_{DD125}	-	3.3	-	mA	1.8 V	12 MHz	X	V	X
Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD126}	-	6.2	-	mA	3.6 V	4 MHz	X	V	V
	I_{DD127}	-	3.1	-	mA	3.6 V	4 MHz	X	V	X
	I_{DD128}	-	6.2	-	mA	1.8 V	4 MHz	X	V	V
	I_{DD129}	-	3.1	-	mA	1.8 V	4 MHz	X	V	X
Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD130}	-	7	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	X	16 MHz	V	V
	I_{DD131}	-	3.3	-	mA	3.6 V	X	16 MHz	V	X
	I_{DD132}	-	7	-	mA	1.8 V	X	16 MHz	V	V
	I_{DD133}	-	3.3	-	mA	1.8 V	X	16 MHz	V	X
Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD134}	-	6.9	-	mA	3.6 V	X	12 MHz	V	V
	I_{DD135}	-	3.3	-	mA	3.6 V	X	12 MHz	V	X
	I_{DD136}	-	6.8	-	mA	1.8 V	X	12 MHz	V	V
	I_{DD137}	-	3.3	-	mA	1.8 V	X	12 MHz	V	X
Operating Current Normal Run Mode HCLK =18 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD138}	-	6.2	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	X	4 MHz	V	V
	I_{DD139}	-	3.1	-	mA	3.6 V	X	4 MHz	V	X
	I_{DD140}	-	6.1	-	mA	1.8 V	X	4 MHz	V	V

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{DD141}	-	3	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD142}	-	5.7	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	16 MHz	X	X	V
	I_{DD143}	-	2.9	-	mA	3.6 V	16 MHz	X	X	X
	I_{DD144}	-	5.7	-	mA	1.8 V	16 MHz	X	X	V
	I_{DD145}	-	2.9	-	mA	1.8 V	16 MHz	X	X	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD146}	-	5.8	-	mA	3.6 V	12 MHz	X	V	V
	I_{DD147}	-	3	-	mA	3.6 V	12 MHz	X	V	X
	I_{DD148}	-	5.7	-	mA	1.8 V	12 MHz	X	V	V
	I_{DD149}	-	3	-	mA	1.8 V	12 MHz	X	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD150}	-	5.6	-	mA	3.6 V	4 MHz	X	V	V
	I_{DD151}	-	2.8	-	mA	3.6 V	4 MHz	X	V	X
	I_{DD152}	-	5.6	-	mA	1.8 V	4 MHz	X	V	V
	I_{DD153}	-	2.8	-	mA	1.8 V	4 MHz	X	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD154}	-	6	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	X	16 MHz	X	V
	I_{DD155}	-	2.8	-	mA	3.6 V	X	16 MHz	X	X
	I_{DD156}	-	5.9	-	mA	1.8 V	X	16 MHz	X	V
	I_{DD157}	-	2.8	-	mA	1.8 V	X	16 MHz	X	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD158}	-	6.2	-	mA	3.6 V	X	12 MHz	V	V
	I_{DD159}	-	3	-	mA	3.6 V	X	12 MHz	V	X
	I_{DD160}	-	6.2	-	mA	1.8 V	X	12 MHz	V	V
	I_{DD161}	-	3	-	mA	1.8 V	X	12 MHz	V	X
Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD162}	-	5.5	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	X	4 MHz	V	V
	I_{DD163}	-	2.8	-	mA	3.6 V	X	4 MHz	V	X
	I_{DD164}	-	5.5	-	mA	1.8 V	X	4 MHz	V	V
	I_{DD165}	-	2.8	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash V_{LDO}=1.6 V	I_{DD166}	-	4.3	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	12 MHz	X	X	V
	I_{DD167}	-	2.2	-	mA	3.6 V	12 MHz	X	X	X
	I_{DD168}	-	4.3	-	mA	1.8 V	12 MHz	X	X	V

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Idle Mode HCLK =36 MHz V_{LDO}=1.8 V	I_{IDLE10}	-	2	-	mA	3.6 V	4 MHz	X	V	X
	I_{IDLE11}	-	8.8	-	mA	1.8 V	4 MHz	X	V	V
	I_{IDLE12}	-	2	-	mA	1.8 V	4 MHz	X	V	X
Operating Current Idle Mode HCLK =36 MHz V_{LDO}=1.8 V	I_{IDLE13}	-	9	-	mA	V_{DD}	HXT	HIRC1	PLL	All digital module
						3.6 V	X	36 MHz	X	V
	I_{IDLE14}	-	1.9	-	mA	3.6 V	X	36 MHz	X	X
	I_{IDLE15}	-	8.8	-	mA	1.8 V	X	36 MHz	X	V
	I_{IDLE16}	-	1.9	-	mA	1.8 V	X	36 MHz	X	X
Operating Current Idle Mode HCLK =36 MHz V_{LDO}=1.8 V	I_{IDLE17}	-	10.1	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	X	16 MHz	V	V
	I_{IDLE18}	-	2.3	-	mA	3.6 V	X	16 MHz	V	X
	I_{IDLE19}	-	9.7	-	mA	1.8 V	X	16 MHz	V	V
	I_{IDLE20}	-	2.2	-	mA	1.8 V	X	16 MHz	V	X
Operating Current Idle Mode HCLK =36 MHz V_{LDO}=1.8 V	I_{IDLE21}	-	10	-	mA	3.6 V	X	12 MHz	V	V
	I_{IDLE22}	-	2.2	-	mA	3.6 V	X	12 MHz	V	X
	I_{IDLE23}	-	9.6	-	mA	1.8 V	X	12 MHz	V	V
	I_{IDLE24}	-	2.2	-	mA	1.8 V	X	12 MHz	V	X
Operating Current Idle Mode HCLK =36 MHz V_{LDO}=1.8 V	I_{IDLE25}	-	9	-	mA	V_{DD}	HXT	MIRC	PLL	All digital module
						3.6 V	X	4 MHz	V	V
	I_{IDLE26}	-	6.3	-	mA	3.6 V	X	4 MHz	V	X
	I_{IDLE27}	-	8.7	-	mA	1.8 V	X	4 MHz	V	V
	I_{IDLE28}	-	6.2	-	mA	1.8 V	X	4 MHz	V	X
Operating Current Idle Mode HCLK =18 MHz V_{LDO}=1.8 V	I_{IDLE29}	-	5	-	mA	V_{DD}	HXT	HIRC0	PLL	All digital module
						3.6 V	18 MHz	X	X	V
	I_{IDLE30}	-	1.5	-	mA	3.6 V	18 MHz	X	X	X
	I_{IDLE31}	-	5	-	mA	1.8 V	18 MHz	X	X	V
	I_{IDLE32}	-	1.5	-	mA	1.8 V	18 MHz	X	X	X
Operating Current Idle Mode HCLK =18 MHz V_{LDO}=1.8 V	I_{IDLE33}	-	5.2	-	mA	3.6 V	16 MHz	X	V	V
	I_{IDLE34}	-	1.7	-	mA	3.6 V	16 MHz	X	V	X
	I_{IDLE35}	-	5.1	-	mA	1.8 V	16 MHz	X	V	V
	I_{IDLE36}	-	1.6	-	mA	1.8 V	16 MHz	X	V	X
Operating Current	I_{IDLE37}	-	5.1	-	mA	3.6 V	12 MHz	X	V	V

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Idle Mode HCLK =32.768 kHz V_{LDO}=1.2 V						3.6 V	32.768 kHz	X	X	V
	$I_{IDLE206}$	-	211	-	uA	3.6 V	32.768 kHz	X	X	X
	$I_{IDLE207}$	-	204	-	uA	1.8 V	32.768 kHz	X	X	V
	$I_{IDLE208}$	-	200	-	uA	1.8 V	32.768 kHz	X	X	X
Operating Current Idle Mode HCLK =10 kHz V_{LDO}=1.2 V	$I_{IDLE209}$	-	122	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module
						3.6 V	X	10 kHz	X	V
	$I_{IDLE210}$	-	132	-	uA	3.6 V	X	10 kHz	X	X
	$I_{IDLE211}$	-	112	-	uA	1.8 V	X	10 kHz	X	V
	$I_{IDLE212}$	-	111	-	uA	1.8 V	X	10 kHz	X	X
Standby Current Power-down Mode V_{LDO}=1.8 V	I_{PWD1}	-	1.7	-	uA	V_{DD}	HXT/HIRC/PLL	LXT(kHz)	RTC	RAM retention
						3.6 V	X	X	X	V
	I_{PWD2}	-	2.3	-	uA	3.6 V	X	32.768	V	V
	I_{PWD3}	-	1.6	-	uA	1.8 V	X	X	X	V
	I_{PWD4}	-	2.2	-	uA	1.8 V	X	32.768	V	V
Standby Current Power-down Mode V_{LDO}=1.6 V	I_{PWD5}	-	1.6	-	uA	3.6 V	X	X	X	V
	I_{PWD6}	-	2.2	-	uA	3.6 V	X	32.768	V	V
	I_{PWD7}	-	1.5	-	uA	1.8 V	X	X	X	V
	I_{PWD8}	-	2.1	-	uA	1.8 V	X	32.768	V	V
Standby Current Power-down Mode V_{LDO}=1.2 V	I_{PWD9}	-	1.6	-	uA	3.6 V	X	X	X	V
	I_{PWD10}	-	2.1	-	uA	3.6 V	X	32.768	V	V
	I_{PWD11}	-	1.4	-	uA	1.8 V	X	X	X	V
	I_{PWD12}	-	2.0	-	uA	1.8 V	X	32.768	V	V

Input Pull Up Resistor PA, PB, PC, PD, PE, PF	R_{IN}	-	42	-	KΩ	V_{DD} = 3.3V
		-	106	-	KΩ	V_{DD} = 1.8V
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-1	-	1	μA	V_{DD} = 3.3V, 0<V_{IN}<V_{DD}
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL1}	-	-	0.3*V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH1}	0.7*V_{DD}	-	-	V	ADC/ACMP/HXT/LXT shared pins and PA.8/PB.4/PB.5 pins without Input 5V tolerance.

9.4.2 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	3.6	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	40	-	μA	AV_{DD} = 3.6V
I_{LPBOD}	Quiescent Current	-	0.5	-	μA	AV_{DD} = 3.6V
V_{BOD}	Brown-out Voltage 25℃	1.75	1.8	1.79	V	BODCTL[15:12] = 0001
		1.84	1.9	1.89	V	BODCTL[15:12] = 0010
		1.94	2.0	1.99	V	BODCTL[15:12] = 0011
		2.04	2.1	2.09	V	BODCTL[15:12] = 0100
		2.14	2.2	2.19	V	BODCTL[15:12] = 0101
		2.23	2.3	2.29	V	BODCTL[15:12] = 0110
		2.33	2.4	2.39	V	BODCTL[15:12] = 0111
		2.43	2.5	2.49	V	BODCTL[15:12] = 1000
		2.53	2.6	2.59	V	BODCTL[15:12] = 1001
		2.62	2.7	2.69	V	BODCTL[15:12] = 1010
		2.72	2.8	2.79	V	BODCTL[15:12] = 1011
		2.82	2.9	2.89	V	BODCTL[15:12] = 1100
		2.92	3	2.99	V	BODCTL[15:12] = 1101
		3.02	3.1	3.09	V	BODCTL[15:12] = 1110
V_{LPBOD}	Low Power Mode Brown-out Voltage 25℃	2.01	2.0	2.07	V	BODCTL[9] = 0
		2.42	2.5	2.79	V	BODCTL[9] = 1

9.4.3 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Threshold Voltage	-	1.5	-	V	-

9.4.4 Low-Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Threshold Voltage	-	1.68	-	V	-

9.4.5 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION (supply voltage = 3V)
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40		+105	^oC	
Operating current	I_{TEMP}	-	5	-	μA	
Gain	V_{TG}	-1.64	-1.70	-1.76	mV/^oC	
Offset	V_{TO}	735	745	755	mV	Temperature at 0 ^oC

Note: Internal operation voltage comes from LDO.

11 REVISION HISTORY

Date	Revision	Description
2016.7.1	1.00	Initial version