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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	119
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	14K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12xd256cag

Chapter 3
Pierce Oscillator (S12XOSCLCPV1)

Chapter 4
Analog-to-Digital Converter (ATD10B16CV4)
Block Description

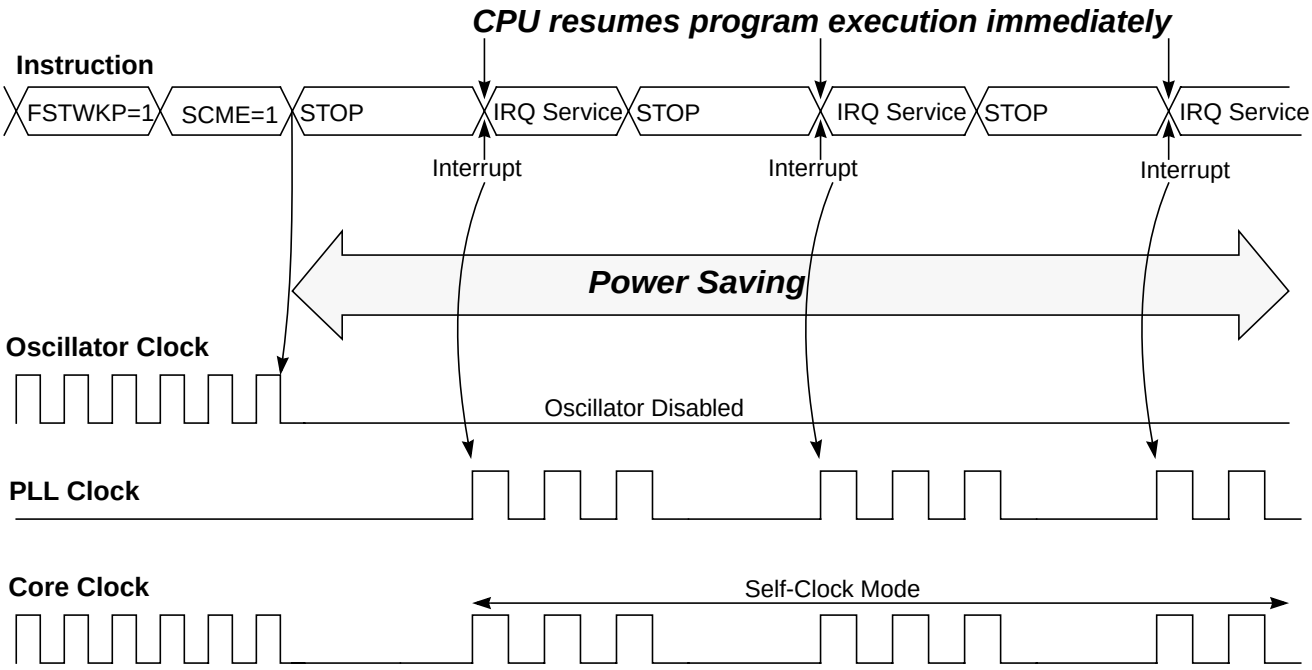

Figure 2-23. Fast Wake-up from Full Stop Mode: Example 1

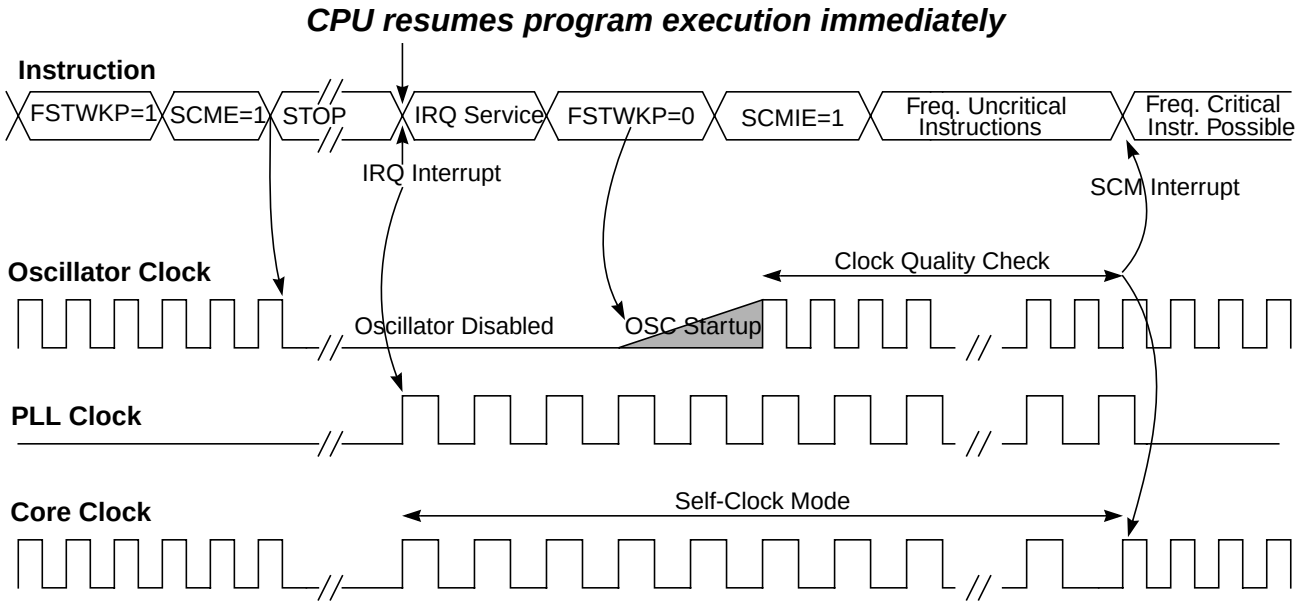

Figure 2-24. Fast Wake-up from Full Stop Mode: Example 2

ADD — Add without Carry — ADD

Operation

RS1 + RS2 ⇒ RD
RD + IMM16 ⇒ RD (translates to ADDL RD, #IMM16[7:0]; ADDH RD, #[15:8])

Performs a 16 bit addition and stores the result in the destination register RD.

CCR Effects

N	Z	V	C
Δ	Δ	Δ	Δ

N: Set if bit 15 of the result is set; cleared otherwise.

Z: Set if the result is $0000; cleared otherwise.

V: Set if a two´s complement overflow resulted from the operation; cleared otherwise.
$RS1[15] \& RS2[15] \& \overline{RD[15]}_{new} | \overline{RS1[15]} \& \overline{RS2[15]} \& RD[15]_{new}$
Refer to ADDH instruction for #IMM16 operations.

C: Set if there is a carry from bit 15 of the result; cleared otherwise.
$RS1[15] \& RS2[15] | RS1[15] \& \overline{RD[15]}_{new} | RS2[15] \& \overline{RD[15]}_{new}$
Refer to ADDH instruction for #IMM16 operations.

Code and CPU Cycles

Source Form	Address Mode	Machine Code										Cycles
ADD RD, RS1, RS2	TRI	0	0	0	1	1	RD	RS1	RS2	1	0	P
ADD RD, #IMM16	IMM8	1	1	1	0	0	RD	IMM16[7:0]				P
	IMM8	1	1	1	0	1	RD	IMM16[15:8]				P

7.3.2.12 Main Timer Interrupt Flag 1 (TFLG1)

	7	6	5	4	3	2	1	0
R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
Reset	0	0	0	0	0	0	0	0

Figure 7-17. Main Timer Interrupt Flag 1 (TFLG1)

Read: Anytime

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

NOTE

When TFFCA = 1, the flags cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference Section 7.3.2.6, “Timer System Control Register 1 (TSCR1)”.

All bits reset to zero.

TFLG1 indicates when interrupt conditions have occurred. The flags can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (reference TFFCA bit in Section 7.3.2.6, “Timer System Control Register 1 (TSCR1)”).

Use of the TFMOD bit in the ICSYS register in conjunction with the use of the ICOVW register allows a timer interrupt to be generated after capturing two values in the capture and holding registers, instead of generating an interrupt for every capture.

Table 7-16. TFLG1 Field Descriptions

Field	Description
7:0 C[7:0]F	**Input Capture/Output Compare Channel “x” Flag** — A CxF flag is set when a corresponding input capture or output compare is detected. C0F can also be set by 16-bit Pulse Accumulator B (PACB). C3F–C0F can also be set by 8-bit pulse accumulators PAC3–PAC0. If the delay counter is enabled, the CxF flag will not be set until after the delay.

In slave transmitter routine, the received acknowledge bit (RXAK) must be tested before transmitting the next byte of data. Setting RXAK means an 'end of data' signal from the master receiver, after which it must be switched from transmitter mode to receiver mode by software. A dummy read then releases the SCL line so that the master can generate a STOP signal.

9.7.1.7 Arbitration Lost

If several masters try to engage the bus simultaneously, only one master wins and the others lose arbitration. The devices which lost arbitration are immediately switched to slave receive mode by the hardware. Their data output to the SDA line is stopped, but SCL continues to be generated until the end of the byte during which arbitration was lost. An interrupt occurs at the falling edge of the ninth clock of this transfer with IBAL=1 and MS/SL=0. If one master attempts to start transmission while the bus is being engaged by another master, the hardware will inhibit the transmission; switch the MS/SL bit from 1 to 0 without generating STOP condition; generate an interrupt to CPU and set the IBAL to indicate that the attempt to engage the bus is failed. When considering these cases, the slave service routine should test the IBAL first and the software should clear the IBAL bit if it is set.

	7	6	5	4	3	2	1	0
R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-18. MSCAN Receive Error Counter (CANRXERR)

Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)

Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

10.3.2.16 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-19. MSCAN Transmit Error Counter (CANTXERR)

Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)

Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

(DBGXCTL)". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 19-24. DBGSCR3 Field Descriptions

Field	Description
3–0 SC[3:0]	**State Control Bits** — These bits select the targeted next state while in State3, based upon the match event. The trigger priorities described in Table 19-38 dictate that in the case of simultaneous matches, the match on the lower channel number (0,1,2,3) has priority. The SC[3:0] encoding ensures that a match leading to final state has priority over all other matches.

Table 19-25. State3 Sequencer Next State Selection

SC[3:0]	Description
0000	Any match triggers to state1
0001	Any match triggers to state2
0010	Any match triggers to final state
0011	Match0 triggers to State1..... Other matches have no effect
0100	Match0 triggers to State2..... Other matches have no effect
0101	Match0 triggers to final state..... Other matches have no effect
0110	Match1 triggers to State1..... Other matches have no effect
0111	Match1 triggers to State2..... Other matches have no effect
1000	Match1 triggers to final state..... Other matches have no effect
1001	Match2 triggers to State2..... Match0 triggers to final state..... Other matches have no effect
1010	Match1 triggers to State1..... Match3 triggers to State2..... Other matches have no effect
1011	Match3 triggers to State2..... Match1 triggers to final state..... Other matches have no effect
1100	Match2 triggers to final state..... Other matches have no effect
1101	Match3 triggers to final state..... Other matches have no effect
1110	Reserved
1111	Reserved

19.3.1.11 Comparator Register Descriptions

Each comparator has a bank of registers that are visible through an 8-byte window in the DBG module register address map. Comparators A and C consist of 8 register bytes (3 address bus compare registers, 2 data bus compare registers, 2 data bus mask registers and a control register).

Comparators B and D consist of 4 register bytes (3 address bus compare registers and a control register).

Each set of comparator registers is accessible in the same 8-byte window of the register address map and can be accessed using the COMRV bits in the DBGC1 register. If the Comparators B or D are accessed through the 8-byte window, then only the address and control bytes are visible, the 4 bytes associated with data bus and data bus masking read as 0 and cannot be written. Furthermore the control registers for comparators B and D differ from those of comparators A and C.

Table 19-26. Comparator Register Layout

0x0028	CONTROL	Read/Write	

Table 20-5. COMRV Encoding

COMRV	Visible Comparator	Visible Register at 0x0027
10	Comparator C	DBGSCR3
11	Comparator D	DBGMFR

21.4.2 Internal Visibility

Internal visibility allows the observation of the internal MCU address and data bus as well as the determination of the access source and the CPU pipe (queue) status through the external bus interface.

Internal visibility is always enabled in emulation single chip mode and emulation expanded mode. Internal CPU and BDM accesses are made visible on the external bus interface, except those to BDM firmware and BDM registers.

Internal reads are made visible on ADDRx/IVDx (address and read data multiplexed, see Table 21-9 to Table 21-11), internal writes on ADDRx and DATAx (see Table 21-12 to Table 21-14). R/$\overline{W}$ and $\overline{LSTRB}$ show the type of access. External read data are also visible on IVDx.

21.4.2.1 Access Source and Instruction Queue Status Signals

The access source (bus master) can be determined from the external bus control signals ACC[2:0] as shown in Table 21-8.

Table 21-8. Determining Access Source from Control Signals

ACC[2:0]	Access Description
000	Repetition of previous access cycle
001	CPU access
010	BDM access
011	XGATE PRR access[1]
100	No access[2]
101, 110, 111	Reserved

1 Invalid IVD brought out in read cycles

2 Denotes also accesses to BDM firmware and BDM registers (IQSTATx are 'XXXX' and R/$\overline{W}$ = 1 in these cases)

The CPU instruction queue status (execution-start and data-movement information) is brought out as IQSTAT[3:0] signals. For decoding of the IQSTAT values, refer to the S12X_CPU section.

21.4.2.2 Emulation Modes Timing

A bus access lasts 1 ECLK cycle. In case of a stretched external access (emulation expanded mode), up to an infinite amount of ECLK cycles may be added. ADDRx values will only be shown in ECLK high phases, while ACCx, IQSTATx, and IVDx values will only be presented in ECLK low phases.

Based on this multiplex timing, ACCx are only shown in the current (first) access cycle. IQSTATx and (for read accesses) IVDx follow in the next cycle. If the access takes more than one bus cycle, ACCx display NULL (0x000) in the second and all following cycles of the access. IQSTATx display NULL (0x0000) from the third until one cycle after the access to indicate continuation.

The resulting timing pattern of the external bus signals is outlined in the following tables for read, write and interleaved read/write accesses. Three examples represent different access lengths of 1, 2, and n–1 bus cycles. Non-shaded bold entries denote all values related to Access #0.

22.3.2.31 Port M Input Register (PTIM)

	7	6	5	4	3	2	1	0
R	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
W								
Reset[1]	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 22-33. Port M Input Register (PTIM)

1 These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Read: Anytime.

Write: Never, writes to this register have no effect.

This register always reads back the buffered state of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

Table 22-70. Expanded Bus Pin Functions versus Operating Modes (continued)

Pin	Single-Chip Modes		Expanded Modes			
	Normal Single-Chip	Special Single-Chip	Normal Expanded	Emulation Single-Chip	Emulation Expanded	Special Test
PE6	GPIO	GPIO	GPIO	TAGHI	TAGHI	GPIO
PE5	GPIO	GPIO	RE	TAGLO	TAGLO	GPIO
PE4	GPIO *or* *ECLK*	ECLK *or* *GPIO*	ECLK *or* *GPIO*	ECLK	ECLK	ECLK *or* *GPIO*
PE3	GPIO	GPIO	$\overline{\text{LDS}}$ *or* *GPIO*	$\overline{\text{LSTRB}}$	$\overline{\text{LSTRB}}$	$\overline{\text{LSTRB}}$
PE2	GPIO	GPIO	$\overline{\text{WE}}$	R/$\overline{\text{W}}$	R/$\overline{\text{W}}$	R/$\overline{\text{W}}$
PJ5	GPIO	GPIO	GPIO *or* $\overline{\text{CS2}}$	GPIO	GPIO *or* $\overline{\text{CS2}}$	GPIO *or* $\overline{\text{CS2}}$
PJ4	GPIO	GPIO	GPIO *or* $\overline{\text{CS0}}$ (1)	GPIO	GPIO *or* $\overline{\text{CS0}}$ (1)	GPIO *or* $\overline{\text{CS0}}$
PJ2	GPIO	GPIO	GPIO *or* $\overline{\text{CS1}}$	GPIO	GPIO *or* $\overline{\text{CS1}}$	GPIO *or* $\overline{\text{CS1}}$
PJ0	GPIO	GPIO	GPIO *or* $\overline{\text{CS3}}$	GPIO	GPIO *or* $\overline{\text{CS3}}$	GPIO *or* $\overline{\text{CS3}}$

1 Depending on ROMON bit. *Refer to Device Guide, S12X_EBI section and S12X_MMC section for details.*

22.4.5 Low-Power Options

22.4.5.1 Run Mode

No low-power options exist for this module in run mode.

22.4.5.2 Wait Mode

No low-power options exist for this module in wait mode.

22.4.5.3 Stop Mode

All clocks are stopped. There are asynchronous paths to generate interrupts from stop on port P, H, and J.

22.5 Initialization and Application Information

- It is not recommended to write PORTx and DDRx in a word access. When changing the register pins from inputs to outputs, the data may have extra transitions during the write access. Initialize the port data register before enabling the outputs.

Table 23-12. PORTE Field Descriptions

Field	Description
7–0 PE[7:0]	**Port E** — Port E bits 7–0 are associated with external bus control signals and interrupt inputs. These include mode select (MODB, MODA), E clock, double frequency E clock, Instruction Tagging High and Low ($\overline{\text{TAGHI}}$, $\overline{\text{TAGLO}}$), Read/Write (R/$\overline{\text{W}}$), Read Enable and Write Enable ($\overline{\text{RE}}$, $\overline{\text{WE}}$), Lower Data Select ($\overline{\text{LDS}}$), $\overline{\text{IRQ}}$, and $\overline{\text{XIRQ}}$. When not used for any of these specific functions, Port E pins 7–2 can be used as general purpose I/O and pins 1–0 can be used as general purpose inputs. If the data direction bits of the associated I/O pins are set to logic level “1”, a read returns the value of the port register, otherwise the buffered pin input state is read. Pins 6 and 5 are inputs with enabled pull-down devices while RESET pin is low. Pins 7 and 3 are inputs with enabled pull-up devices while RESET pin is low.

23.0.5.10 Port E Data Direction Register (DDRE)

	7	6	5	4	3	2	1	0
R	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 23-12. Port E Data Direction Register (DDRE)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

Table 23-13. DDRE Field Descriptions

Field	Description
7–0 DDRE[7:2]	Data Direction Port E — his register controls the data direction for port E. When Port E is operating as a general purpose I/O port, DDRE determines whether each pin is an input or output. A logic level “1” causes the associated port pin to be an output and a logic level “0” causes the associated pin to be a high-impedance input. Port E bit 1 (associated with $\overline{\text{IRQ}}$) and bit 0 (associated with $\overline{\text{XIRQ}}$) cannot be configured as outputs. Port E, bits 1 and 0, can be read regardless of whether the alternate interrupt function is enabled. 0 Associated pin is configured as input. 1 Associated pin is configured as output. **Note:** Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PORTE after changing the DDRE register.

24.0.5.36 Port P Data Direction Register (DDRP)

	7	6	5	4	3	2	1	0
R W	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
Reset	0	0	0	0	0	0	0	0

Figure 24-38. Port P Data Direction Register (DDRP)

Read: Anytime.

Write: Anytime.

This register configures each port P pin as either input or output.

If the associated PWM channel or SPI module is enabled this register has no effect on the pins.

The PWM forces the I/O state to be an output for each port line associated with an enabled PWM7–0 channel. Channel 7 can force the pin to input if the shutdown feature is enabled. *Refer to PWM section for details.*

If SPI is enabled, the SPI determines the pin direction. *Refer to SPI section for details.*

The DDRP bits revert to controlling the I/O direction of a pin when the associated peripherals are disabled.

Table 24-35. DDRP Field Descriptions

Field	Description
7–0 DDRP[7:0]	**Data Direction Port P** 0 Associated pin is configured as input. 1 Associated pin is configured as output. **Note:** Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTP or PTIP registers, when changing the DDRP register.

24.0.5.37 Port P Reduced Drive Register (RDRP)

	7	6	5	4	3	2	1	0
R W	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Reset	0	0	0	0	0	0	0	0

Figure 24-39. Port P Reduced Drive Register (RDRP)

Read: Anytime.

Write: Anytime.

This register configures the drive strength of each port P output pin as either full or reduced. If the port is used as input this bit is ignored.

Table 27-10. Flash Register Bank Selects

BKSEL[1:0]	Selected Block
10	Flash Block 2
11	Flash Block 3

27.3.2.5 Flash Protection Register (FPROT)

The FPROT register defines which Flash sectors are protected against program or erase operations.

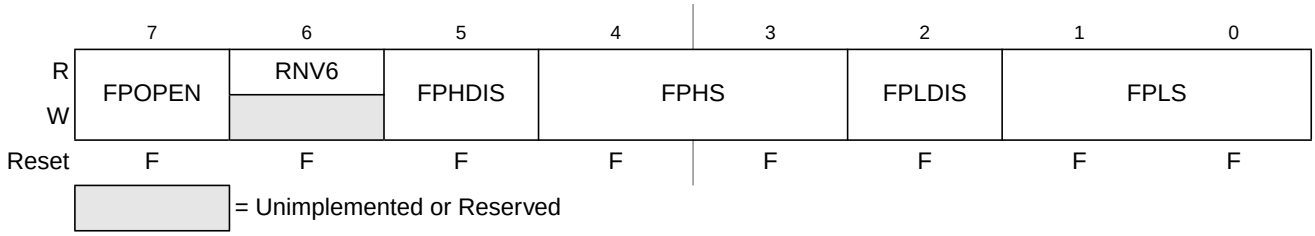

Figure 27-10. Flash Protection Register (FPROT)

All bits in the FPROT register are readable and writable with restrictions (see Section 27.3.2.5.1, “Flash Protection Restrictions”) except for RNV[6] which is only readable.

During the reset sequence, the FPROT register is loaded from the Flash Configuration Field at global address 0x7F_FF0D. To change the Flash protection that will be loaded during the reset sequence, the upper sector of the Flash memory must be unprotected, then the Flash Protect/Security byte located as described in Table 27-1 must be reprogrammed.

Trying to alter data in any protected area in the Flash memory will result in a protection violation error and the PVIOL flag will be set in the FSTAT register. The mass erase of a Flash block is not possible if any of the Flash sectors contained in the Flash block are protected.

Table 27-11. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Flash Protection Open** — The FPOPEN bit determines the protection function for program or erase as shown in Table 27-12. 0 The FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS[1:0] and FPLS[1:0] bits. For an MCU without an EEPROM module, the FPOPEN clear state allows the main part of the Flash block to be protected while a small address range can remain unprotected for EEPROM emulation. 1 The FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS[1:0] and FPLS[1:0] bits.
6 RNV6	**Reserved Nonvolatile Bit** — The RNV[6] bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the Flash memory ending with global address 0x7F_FFFF. 0 Protection/Unprotection enabled. 1 Protection/Unprotection disabled.
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS[1:0] bits determine the size of the protected/unprotected area as shown inTable 27-13. The FPHS[1:0] bits can only be written to while the FPHDIS bit is set.

CBEIF, PVIOL, and ACCERR are readable and writable, CCIF and BLANK are readable and not writable, remaining bits read 0 and are not writable in normal mode. FAIL is readable and writable in special mode. FAIL must be clear in special mode when starting a command write sequence.

Table 27-16. FSTAT Field Descriptions

Field	Description
7 CBEIF	**Command Buffer Empty Interrupt Flag** — The CBEIF flag indicates that the address, data and command buffers are empty so that a new command write sequence can be started. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the Flash address space, but before CBEIF is cleared, will abort a command write sequence and cause the ACCERR flag to be set. Writing a 0 to CBEIF outside of a command write sequence will not set the ACCERR flag. The CBEIF flag is cleared by writing a 1 to CBEIF. The CBEIF flag is used together with the CBEIE bit in the FCNFG register to generate an interrupt request (see Figure 27-32). 0 Command buffers are full. 1 Command buffers are ready to accept a new command.
6 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is cleared and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect on CCIF. The CCIF flag is used together with the CCIE bit in the FCNFG register to generate an interrupt request (see Figure 27-32). 0 Command in progress. 1 All commands are completed.
5 PVIOL	**Protection Violation Flag** —The PVIOL flag indicates an attempt was made to program or erase an address in a protected area of the Flash memory during a command write sequence. Writing a 0 to the PVIOL flag has no effect on PVIOL. The PVIOL flag is cleared by writing a 1 to PVIOL. While PVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected. 1 Protection violation has occurred.
4 ACCERR	**Access Error Flag** — The ACCERR flag indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 27.4.1.2, “Command Write Sequence”), issuing an illegal Flash command (see Table 27-18), launching the sector erase abort command terminating a sector erase operation early (see Section 27.4.2.6, “Sector Erase Abort Command”) or the execution of a CPU STOP instruction while a command is executing (CCIF = 0). Writing a 0 to the ACCERR flag has no effect on ACCERR. The ACCERR flag is cleared by writing a 1 to ACCERR.While ACCERR is set, it is not possible to launch a command or start a command write sequence. If ACCERR is set by an erase verify operation or a data compress operation, any buffered command will not launch. 0 No access error detected. 1 Access error has occurred.
2 BLANK	**Flag Indicating the Erase Verify Operation Status** — When the CCIF flag is set after completion of an erase verify command, the BLANK flag indicates the result of the erase verify operation. The BLANK flag is cleared by the Flash module when CBEIF is cleared as part of a new valid command write sequence. Writing to the BLANK flag has no effect on BLANK. 0 Flash block verified as not erased. 1 Flash block verified as erased.
1 FAIL	**Flag Indicating a Failed Flash Operation** — The FAIL flag will set if the erase verify operation fails (selected Flash block verified as not erased). Writing a 0 to the FAIL flag has no effect on FAIL. The FAIL flag is cleared by writing a 1 to FAIL. 0 Flash operation completed without error. 1 Flash operation failed.

10. If Flash block 5 is selected for compression, DATA equal to the contents of the MISR for Flash block 5 is compressed into the MISR for Flash block 0.
11. If Flash block 6 is selected for compression, DATA equal to the contents of the MISR for Flash block 6 is compressed into the MISR for Flash block 0.
12. If Flash block 7 is selected for compression, DATA equal to the contents of the MISR for Flash block 7 is compressed into the MISR for Flash block 0.
13. The contents of the MISR for Flash block 0 are written to the FDATA registers.

0x0200–0x023F Freescale Scalable CAN — MSCAN (CAN3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0200	CAN3CTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x0201	CAN3CTL1	R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		W								
0x0202	CAN3BTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x0203	CAN3BTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x0204	CAN3RFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								
0x0205	CAN3RIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		W								
0x0206	CAN3TFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
		W								
0x0207	CAN3TIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		W								
0x0208	CAN3TARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		W								
0x0209	CAN3TAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		W								
0x020A	CAN3TBSEL	R	0	0	0	0	0	TX2	TX1	TX0
		W								
0x020B	CAN3IDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		W								
0x020C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x020D	Reserved	R	0	0	0	0	0	0	0	BOHOLD
		W								
0x020E	CAN3RXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		W								
0x020F	CAN3TXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		W								
0x0210	CAN3IDAR0	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0211	CAN3IDAR1	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0212	CAN3IDAR2	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0213	CAN3IDAR3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0214	CAN3IDMR0	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0215	CAN3IDMR1	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								