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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12xdp512mal

Chapter 10
Freescale's Scalable Controller Area Network (S12MSCANV3)

Chapter 11
Serial Communication Interface (S12SCIV5)

Chapter 21
External Bus Interface (S12XEBIV2)

Chapter 22
DP512 Port Integration Module (S12XDP512PIMV2)

Table 1-7. Signal Properties Summary (Sheet 2 of 4)

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Pin Name Function 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
PE0	$\overline{\text{XIRQ}}$	—	—	—	V_{DDR}	PUCR	Up	Port E input, non-maskable interrupt
PH7	KWH7	$\overline{\text{SS2}}$	TXD5	—	V_{DDR}	PERH/PPSH	Disabled	Port H I/O, interrupt, $\overline{\text{SS}}$ of SPI2, TXD of SCI5
PH6	KWH6	SCK2	RXD5	—	V_{DDR}	PERH/ PPSH	Disabled	Port H I/O, interrupt, SCK of SPI2, RXD of SCI5
PH5	KWH5	MOSI2	TXD4	—	V_{DDR}	PERH/ PPSH	Disabled	Port H I/O, interrupt, MOSI of SPI2, TXD of SCI4
PH4	KWH4	MISO2	RXD4	—	V_{DDR}	PERH/PPSH	Disabled	Port H I/O, interrupt, MISO of SPI2, RXD of SCI4
PH3	KWH3	$\overline{\text{SS1}}$	—	—	V_{DDR}	PERH/PPSH	Disabled	Port H I/O, interrupt, $\overline{\text{SS}}$ of SPI1
PH2	KWH2	SCK1	—	—	V_{DDR}	PERH/PPSH	Disabled	Port H I/O, interrupt, SCK of SPI1
PH1	KWH1	MOSI1	—	—	V_{DDR}	PERH/PPSH	Disabled	Port H I/O, interrupt, MOSI of SPI1
PH0	KWH0	MISO1	—	—	V_{DDR}	PERH/PPSH	Disabled	Port H I/O, interrupt, MISO of SPI1
PJ7	KWJ7	TXCAN4	SCL0	TXCAN0	V_{DDX}	PERJ/ PPSJ	Up	Port J I/O, interrupt, TX of CAN4, SCL of IIC0, TX of CAN0
PJ6	KWJ6	RXCAN4	SDA0	RXCAN0	V_{DDX}	PERJ/ PPSJ	Up	Port J I/O, interrupt, RX of CAN4, SDA of IIC0, RX of CAN0
PJ5	KWJ5	SCL1	$\overline{\text{CS2}}$	—	V_{DDX}	PERJ/ PPSJ	Up	Port J I/O, interrupt, SCL of IIC1, chip select 2
PJ4	KWJ4	SDA1	$\overline{\text{CS0}}$	—	V_{DDX}	PERJ/ PPSJ	Up	Port J I/O, interrupt, SDA of IIC1, chip select 0
PJ2	KWJ2	$\overline{\text{CS1}}$	—	—	V_{DDX}	PERJ/ PPSJ	Up	Port J I/O, interrupt, chip select 1
PJ1	KWJ1	TXD2	—	—	V_{DDX}	PERJ/ PPSJ	Up	Port J I/O, interrupt, TXD of SCI2
PJ0	KWJ0	RXD2	$\overline{\text{CS3}}$	—	V_{DDX}	PERJ/ PPSJ	Up	Port J I/O, interrupt, RXD of SCI2
PK7	—	—	—	—	V_{DDX}	PUCR	Up	Port K I/O
PK[5:4]	—	—	—	—	V_{DDX}	PUCR	Up	Port K I/O
PK7	$\overline{\text{EWAIT}}$	ROMCTL	—	—	V_{DDX}	PUCR	Up	Port K I/O, EWAIT input, ROM on control
PK[6:4]	ADDR [22:20]	ACC[2:0]	—	—	V_{DDX}	PUCR	Up	Port K I/O, extended addresses, access source for external access
PK3	ADDR19	IQSTAT3	—	—	V_{DDX}	PUCR	Up	Extended address, PIPE status

Table 4-1. ATD10B16CV4 Memory Map

Address Offset	Use	Access
0x0000	ATD Control Register 0 (ATDCTL0)	R/W
0x0001	ATD Control Register 1 (ATDCTL1)	R/W
0x0002	ATD Control Register 2 (ATDCTL2)	R/W
0x0003	ATD Control Register 3 (ATDCTL3)	R/W
0x0004	ATD Control Register 4 (ATDCTL4)	R/W
0x0005	ATD Control Register 5 (ATDCTL5)	R/W
0x0006	ATD Status Register 0 (ATDSTAT0)	R/W
0x0007	Unimplemented	
0x0008	ATD Test Register 0 (ATDTEST0)[1]	R
0x0009	ATD Test Register 1 (ATDTEST1)	R/W
0x000A	ATD Status Register 2 (ATDSTAT2)	R
0x000B	ATD Status Register 1 (ATDSTAT1)	R
0x000C	ATD Input Enable Register 0 (ATDDIEN0)	R/W
0x000D	ATD Input Enable Register 1 (ATDDIEN1)	R/W
0x000E	Port Data Register 0 (PORTAD0)	R
0x000F	Port Data Register 1 (PORTAD1)	R
0x0010, 0x0011	ATD Result Register 0 (ATDDR0H, ATDDR0L)	R/W
0x0012, 0x0013	ATD Result Register 1 (ATDDR1H, ATDDR1L)	R/W
0x0014, 0x0015	ATD Result Register 2 (ATDDR2H, ATDDR2L)	R/W
0x0016, 0x0017	ATD Result Register 3 (ATDDR3H, ATDDR3L)	R/W
0x0018, 0x0019	ATD Result Register 4 (ATDDR4H, ATDDR4L)	R/W
0x001A, 0x001B	ATD Result Register 5 (ATDDR5H, ATDDR5L)	R/W
0x001C, 0x001D	ATD Result Register 6 (ATDDR6H, ATDDR6L)	R/W
0x001E, 0x001F	ATD Result Register 7 (ATDDR7H, ATDDR7L)	R/W
0x0020, 0x0021	ATD Result Register 8 (ATDDR8H, ATDDR8L)	R/W
0x0022, 0x0023	ATD Result Register 9 (ATDDR9H, ATDDR9L)	R/W
0x0024, 0x0025	ATD Result Register 10 (ATDDR10H, ATDDR10L)	R/W
0x0026, 0x0027	ATD Result Register 11 (ATDDR11H, ATDDR11L)	R/W
0x0028, 0x0029	ATD Result Register 12 (ATDDR12H, ATDDR12L)	R/W
0x002A, 0x002B	ATD Result Register 13 (ATDDR13H, ATDDR13L)	R/W
0x002C, 0x002D	ATD Result Register 14 (ATDDR14H, ATDDR14L)	R/W
0x002E, 0x002F	ATD Result Register 15 (ATDDR15H, ATDDR15L)	R/W

[1] ATDTEST0 is intended for factory test purposes only.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

6.8.1.4 Immediate 4 Bit Wide (IMM4)

The 4 bit wide immediate addressing mode is supported by all shift instructions.

RD = RD ∗ imm4

Examples:

```
LSL     R4,#1    ; R4 = R4 << 1; shift register R4 by 1 bit to the left
LSR     R4,#3    ; R4 = R4 >> 3; shift register R4 by 3 bits to the right
```

6.8.1.5 Immediate 8 Bit Wide (IMM8)

The 8 bit wide immediate addressing mode is supported by four major commands (ADD, SUB, LD, CMP).

RD = RD ∗ imm8

Examples:

```
ADDL    R1,#1    ; adds an 8 bit value to register R1
SUBL    R2,#2    ; subtracts an 8 bit value from register R2
LDH     R3,#3    ; loads an 8 bit immediate into the high byte of Register R3
CMPL    R4,#4    ; compares the low byte of register R4 with an immediate value
```

6.8.1.6 Immediate 16 Bit Wide (IMM16)

The 16 bit wide immediate addressing mode is a construct to simplify assembler code. Instructions which offer this mode are translated into two opcodes using the eight bit wide immediate addressing mode.

RD = RD ∗ imm16

Examples:

```
LDW     R4,#$1234        ; translated to LDL R4,#$34; LDH R4,#$12
ADD     R4,#$5678        ; translated to ADDL R4,#$78; ADDH R4,#$56
```

6.8.1.7 Monadic Addressing (MON)

In this addressing mode only one operand is explicitly given. This operand can either be the source (*f*(RD)), the target (RD = *f*()), or both source and target of the operation (RD = *f*(RD)).

Examples:

```
JAL     R1       ; PC = R1, R1 = PC+2
SIF     R2       ; Trigger IRQ associated with the channel number in R2.L
```

CMP — Compare — CMP

Operation

RS2 – RS1 ⇒ NONE (translates to SUB R0, RS1, RS2)
RD – IMM16 ⇒ NONE (translates to CMPL RD, #IMM16[7:0]; CPCH RD, #IMM16[15:8])

Subtracts two 16 bit values and discards the result.

CCR Effects

N	Z	V	C
Δ	Δ	Δ	Δ

N: Set if bit 15 of the result is set; cleared otherwise.

Z: Set if the result is $0000; cleared otherwise.

V: Set if a two´s complement overflow resulted from the operation; cleared otherwise.
RS1[15] & $\overline{RS2[15]}$ & $\overline{result[15]}$ | $\overline{RS1[15]}$ & RS2[15] & result[15]
RD[15] & $\overline{IMM16[15]}$ & $\overline{result[15]}$ | $\overline{RD[15]}$ & IMM16[15] & result[15]

C: Set if there is a carry from the bit 15 of the result; cleared otherwise.
$\overline{RS1[15]}$ & RS2[15] | $\overline{RS1[15]}$ & result[15] | RS2[15] & result[15]
$\overline{RD[15]}$ & IMM16[15] | $\overline{RD[15]}$ & result[15] | IMM16[15] & result[15]

Code and CPU Cycles

Source Form	Address Mode	Machine Code											Cycles
CMP RS1, RS2	TRI	0	0	0	1	1	0	0	0	RS1	RS2	0	0	P
CMP RS, #IMM16	IMM8	1	1	0	1	0	RS			IMM16[7:0]				P
	IMM8	1	1	0	1	1	RS			IMM16[15:8]				P

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
	W								
TFLG1	R	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
	W								
TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
TC0 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC0 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
TC1 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC1 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
TC2 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC2 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
TC3 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC3 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
TC4 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC4 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
TC5 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC5 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								

= Unimplemented or Reserved

Figure 7-2. ECT Register Summary (Sheet 2 of 5)

7.3.2.10 Timer Interrupt Enable Register (TIE)

	7	6	5	4	3	2	1	0
R W	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 7-15. Timer Interrupt Enable Register (TIE)

Read or write: Anytime

All bits reset to zero.

The bits C7I–C0I correspond bit-for-bit with the flags in the TFLG1 status register.

Table 7-13. TIE Field Descriptions

Field	Description
7:0 C[7:0]I	**Input Capture/Output Compare “x” Interrupt Enable** 0 The corresponding flag is disabled from causing a hardware interrupt. 1 The corresponding flag is enabled to cause an interrupt.

Table 7-34. Precision Timer Modulus Counter Prescaler Select Examples when PRNT = 1 (continued)

PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0	Prescaler Division Rate
0	0	0	0	0	1	1	1	8
0	0	0	0	1	1	1	1	16
0	0	0	1	1	1	1	1	32
0	0	1	1	1	1	1	1	64
0	1	1	1	1	1	1	1	128
1	1	1	1	1	1	1	1	256

7.3.2.27 16-Bit Pulse Accumulator B Control Register (PBCTL)

	7	6	5	4	3	2	1	0
R	0	PBEN	0	0	0	0	PBOVI	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-49. 16-Bit Pulse Accumulator B Control Register (PBCTL)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 7-35. PBCTL Field Descriptions

Field	Description
6 PBEN	**Pulse Accumulator B System Enable** — PBEN is independent from TEN. With timer disabled, the pulse accumulator can still function unless pulse accumulator is disabled. 0 16-bit pulse accumulator system disabled. 8-bit PAC1 and PAC0 can be enabled when their related enable bits in ICPAR are set. 1 Pulse accumulator B system enabled. The two 8-bit pulse accumulators PAC1 and PAC0 are cascaded to form the PACB 16-bit pulse accumulator B. When PACB is enabled, the PACN1 and PACN0 registers contents are respectively the high and low byte of the PACB. PA1EN and PA0EN control bits in ICPAR have no effect. The PACB shares the input pin with IC0.
1 PBOVI	**Pulse Accumulator B Overflow Interrupt Enable** 0 Interrupt inhibited 1 Interrupt requested if PBOVF is set

1 Not applicable for receive buffers
2 Read-only for CPU
3 Read-only for CPU

Figure 10-24 shows the common 13-byte data structure of receive and transmit buffers for extended identifiers. The mapping of standard identifiers into the IDR registers is shown in Figure 10-25.

All bits of the receive and transmit buffers are 'x' out of reset because of RAM-based implementation[1]. All reserved or unused bits of the receive and transmit buffers always read 'x'.

1. Exception: The transmit priority registers are 0 out of reset.

SPI operation in wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPICR2 register. In wait mode, if the SPISWAI bit is clear, the SPI operates like in run mode. If the SPISWAI bit is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.

- Stop mode

  The SPI is inactive in stop mode for reduced power consumption. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.

This is a high level description only, detailed descriptions of operating modes are contained in Section 12.4.7, “Low Power Mode Options”.

12.1.4 Block Diagram

Figure 12-1 gives an overview on the SPI architecture. The main parts of the SPI are status, control and data registers, shifter logic, baud rate generator, master/slave control logic, and port control logic.

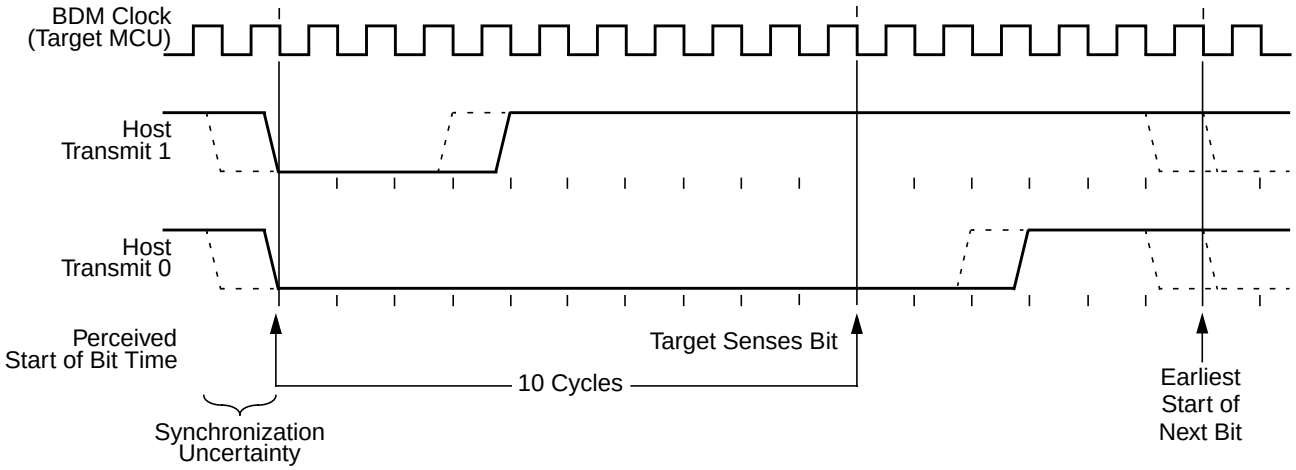

Figure 15-8. BDM Host-to-Target Serial Bit Timing

The receive cases are more complicated. Figure 15-9 shows the host receiving a logic 1 from the target system. Since the host is asynchronous to the target, there is up to one clock-cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

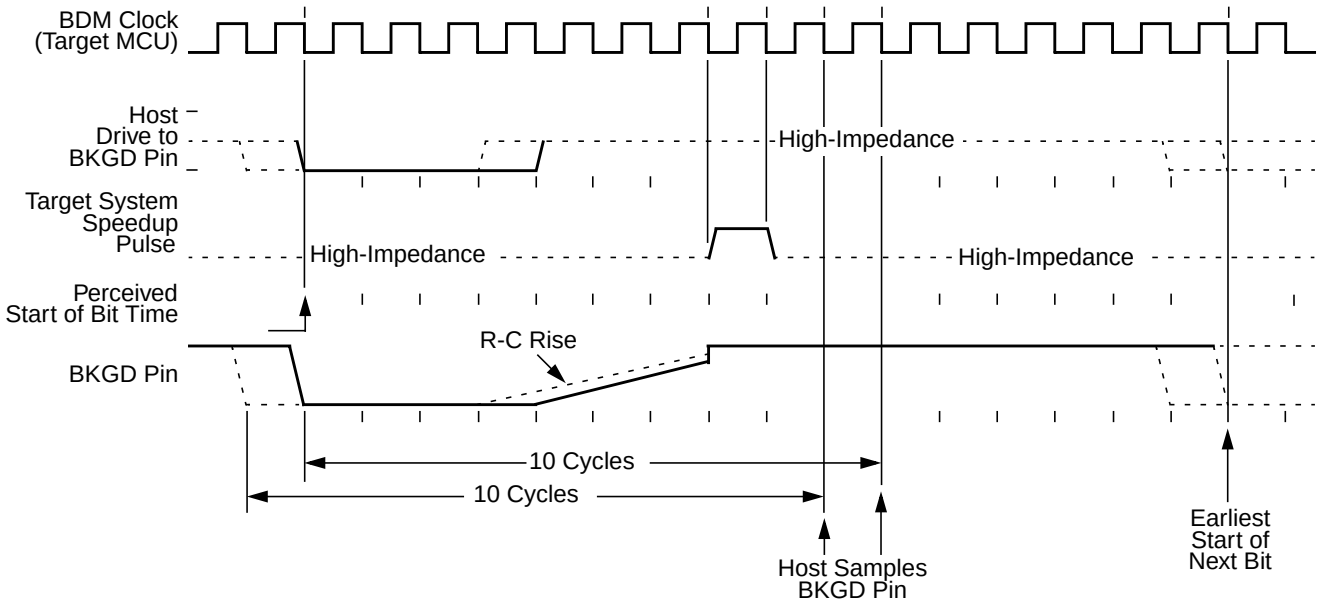

Figure 15-9. BDM Target-to-Host Serial Bit Timing (Logic 1)

Table 18-21 shows the address boundaries of each chip select and the relationship with the implemented resources (internal) parameters.

Table 18-21. Global Chip Selects Memory Space

Chip Selects	Bottom Address	Top Address
$\overline{CS3}$	0x00_0800	0x0F_FFFF minus RAMSIZE[1]
$\overline{CS2}$	0x10_0000	0x13_FFFF minus EEPROMSIZE[2]
$\overline{CS2}$[3]	0x14_0000	0x1F_FFFF
$\overline{CS1}$	0x20_0000	0x3F_FFFF
$\overline{CS0}$[4]	0x40_0000	0x7F_FFFF minus FLASHSIZE[5]

1 External RPAGE accesses in (NX, EX and ST)

2 External EPAGE accesses in (NX, EX and ST)

3 When ROMHM is set (see ROMHM in Table 18-19) the $\overline{CS2}$ is asserted in the space occupied by this on-chip memory block.

4 When the internal NVM is enabled (see ROMON in Section 18.3.2.5, “MMC Control Register (MMCCTL1)) the $\overline{CS0}$ is not asserted in the space occupied by this on-chip memory block.

5 External PPAGE accesses in (NX, EX and ST)

Figure 18-23. Local to Implemented Global Address Mapping (Without GPAGE)

18.4.2.4 XGATE Memory Map Scheme

18.4.2.4.1 Expansion of the XGATE Local Address Map

The XGATE 64 Kbyte memory space allows access to internal resources only (Registers, RAM, and FLASH). The 2 Kilobyte register address range is the same register address range as for the CPU and the BDM module . XGATE can access the FLASH in single chip modes, even when the MCU is secured. In expanded modes, XGATE can not access the FLASH when MCU is secured.

The local address of the XGATE RAM access is translated to the global RAM address range. The XGATE shares the RAM resource with the CPU and the BDM module . The local address of the XGATE FLASH access is translated to the global address as shown in Figure 18-24. For the implemented memory spaces and addresses please refer to Table 1-4 and Table 1-5.

When program control returns from a tagged breakpoint using an RTI or BDM GO command without program counter modification it will return to the instruction whose tag generated the breakpoint. Thus care must be taken to avoid re triggering a breakpoint at the same location. This can be done by reconfiguring the DBG module in the SWI routine, (SWI configuration), or by executing a TRACE command before the GO (BDM configuration) to increment the program flow past the tagged instruction.

Comparators should not be configured for the vector address range while tagging, since these addresses are not opcode addresses

20.3.2.7.1 Debug State Control Register 1 (DBGSCR1)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-9. Debug State Control Register 1 (DBGSCR1)

Read: Anytime

Write: Anytime when S12XDBG not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 00. The state control register 1 selects the targeted next state whilst in State1. The matches refer to the match channels of the comparator match control logic as depicted in Figure 20-1 and described in Section 20.3.2.8.1". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 20-20. DBGSCR1 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State1, based upon the match event.

Table 20-21. State1 Sequencer Next State Selection

SC[3:0]	Description
0000	Any match triggers to state2
0001	Any match triggers to state3
0010	Any match triggers to Final State
0011	Match2 triggers to State2..... Other matches have no effect
0100	Match2 triggers to State3..... Other matches have no effect
0101	Match2 triggers to Final State..... Other matches have no effect
0110	Match0 triggers to State2..... Match1 triggers to State3..... Other matches have no effect
0111	Match1 triggers to State3..... Match0 triggers Final State..... Other matches have no effect
1000	Match0 triggers to State2..... Match2 triggers to State3..... Other matches have no effect
1001	Match2 triggers to State3..... Match0 triggers Final State..... Other matches have no effect
1010	Match1 triggers to State2..... Match3 triggers to State3..... Other matches have no effect
1011	Match3 triggers to State3..... Match1 triggers to Final State..... Other matches have no effect
1100	Match3 has no effect..... All other matches (M0,M1,M2) trigger to State2
1101	Reserved
1110	Reserved
1111	Reserved

The trigger priorities described in Table 20-38 dictate that in the case of simultaneous matches, the match on the lower channel number (0,1,2,3) has priority. The SC[3:0] encoding ensures that a match leading to final state has priority over all other matches.

22.3.2.45 Port P Interrupt Flag Register (PIFP)

	7	6	5	4	3	2	1	0
R W	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
Reset	0	0	0	0	0	0	0	0

Figure 22-47. Port P Interrupt Flag Register (PIFP)

Read: Anytime.

Write: Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSP register. To clear this flag, write logic level “1” to the corresponding bit in the PIFP register. Writing a “0” has no effect.

Table 22-44. PIFP Field Descriptions

Field	Description
7–0 PIFP[7:0]	**Interrupt Flags Port P** 0 No active edge pending. Writing a “0” has no effect. 1 Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set). Writing a logic level “1” clears the associated flag.

External Signal Description

This section lists and describes the signals that do connect off-chip.

23.0.3 Signal Properties

Table 23-1 shows all the pins and their functions that are controlled by the PIM. *Refer to Section , "Functional Description" for the availability of the individual pins in the different package options.*

NOTE

If there is more than one function associated with a pin, the priority is indicated by the position in the table from top (highest priority) to bottom (lowest priority).

Table 23-1. Pin Functions and Priorities (Sheet 1 of 7)

Port	Pin Name	Pin Function and Priority	I/O	Description	Pin Function after Reset
—	BKGD	MODC[1]	I	MODC input during $\overline{\text{RESET}}$	BKGD
		BKGD	I/O	S12X_BDM communication pin	
A	PA[7:0]	ADDR[15:8] mux IVD[15:8][2]	O	High-order external bus address output (multiplexed with IVIS data)	Mode dependent[3]
		GPIO	I/O	General-purpose I/O	
B	PB[7:1]	ADDR[7:1] mux IVD[7:1][2]	O	Low-order external bus address output (multiplexed with IVIS data)	Mode dependent[3]
		GPIO	I/O	General-purpose I/O	
	PB[0]	ADDR[0] mux IVD0[2]	O	Low-order external bus address output (multiplexed with IVIS data)	
		$\overline{\text{UDS}}$	O	Upper data strobe	
		GPIO	I/O	General-purpose I/O	
C	PC[7:0]	DATA[15:8]	I/O	High-order bidirectional data input/output Configurable for reduced input threshold	Mode dependent[3]
		GPIO	I/O	General-purpose I/O	
D	PD[7:0]	DATA[7:0]	I/O	Low-order bidirectional data input/output Configurable for reduced input threshold	Mode dependent[3]
		GPIO	I/O	General-purpose I/O	

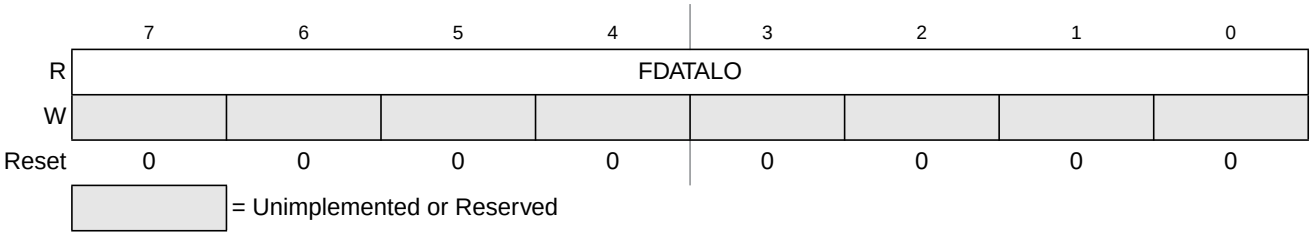

Figure 29-17. Flash Data Low Register (FDATALO)

All FDATAHI and FDATALO bits are readable but are not writable. At the completion of a data compress operation, the resulting 16-bit signature is stored in the FDATA registers. The data compression signature is readable in the FDATA registers until a new command write sequence is started.

29.3.2.11 RESERVED1

This register is reserved for factory testing and is not accessible.

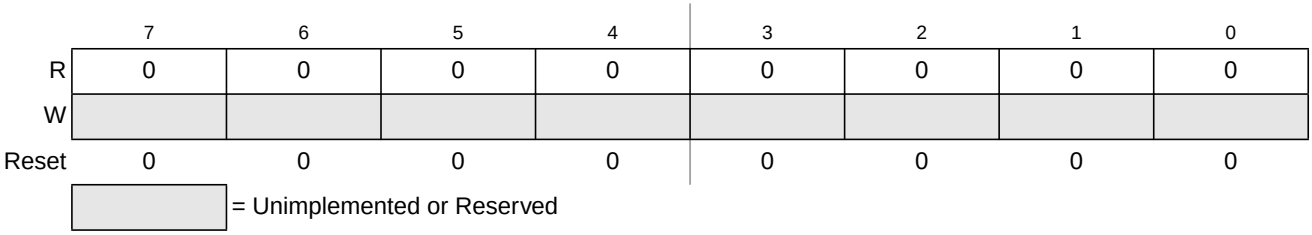

Figure 29-18. RESERVED1

All bits read 0 and are not writable.

29.3.2.12 RESERVED2

This register is reserved for factory testing and is not accessible.

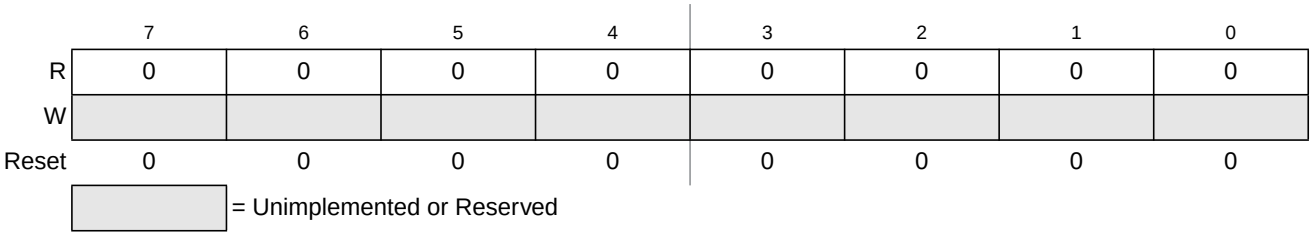

Figure 29-19. RESERVED2

All bits read 0 and are not writable.

29.3.2.13 RESERVED3

This register is reserved for factory testing and is not accessible.

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
LQFP144							
1	T	Thermal resistance LQFP144, single sided PCB[2]	θ_{JA}	—	—	41	°C/W
2	T	Thermal resistance LQFP144, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	32	°C/W
3		Junction to Board LQFP 144	θ_{JB}	—	—	22	°C/W
4		Junction to Case LQFP 144[4]	θ_{JC}	—	—	7/4	°C/W
5		Junction to Package Top LQFP144[5]	Ψ_{JT}	—	—	3	°C/W
LQFP112							
6	T	Thermal resistance LQFP112, single sided PCB[2]	θ_{JA}	—	—	43[3]/49[4]	°C/W
7	T	Thermal resistance LQFP112, double sided PCB with 2 internal planes[5]	θ_{JA}	—	—	32[3]/39[4]	°C/W
8		Junction to Board LQFP112	θ_{JB}	—	—	22[3]/27[4]	°C/W
9		Junction to Case LQFP112[4]	θ_{JC}	—	—	7[3]/11[4]	°C/W
10		Junction to Package Top LQFP112[5]	Ψ_{JT}	—	—	3/2	°C/W
QFP80							
11	T	Thermal resistance QFP 80, single sided PCB[2]	θ_{JA}	—	—	45[3]/49[4]	°C/W
12	T	Thermal resistance QFP 80, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	33[3]/36[4]	°C/W
13	T	Junction to Board QFP 80	θ_{JB}	—	—	19[3]/20[4]	°C/W
14	T	Junction to Case QFP 80[6]	θ_{JC}	—	—	11[3]/14[4]	°C/W
15	T	Junction to Package Top QFP 80[7]	Ψ_{JT}	—	—	3	°C/W

1 The values for thermal resistance are achieved by package simulations

2 Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection.

3 Maskset L15Y / M84E in LQFP112 or QFP80

4 Maskset M42E in LQFP112 or QFP80

5 Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to the JEDEC specification JESD51-7 in a horizontal configuration in natural convection.

6 Junction to case thermal resistance was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. This basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.

7 Thermal characterization parameter Ψ_{JT} is the “resistance” from junction to reference point thermocouple on top center of the case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in a steady state customer enviroment.

Table A-23. PLL Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self clock mode frequency	f_{SCM}	1	—	5.5	MHz
2	D	VCO locking range	f_{VCO}	8	—	80	MHz
3	D	Lock detector transition from acquisition to tracking mode	$\|\Delta_{trk}\|$	3	—	4	%[1]
4	D	Lock detection	$\|\Delta_{Lock}\|$	0	—	1.5	%[1]
5	D	Unlock detection	$\|\Delta_{unl}\|$	0.5	—	2.5	%[1]
6	D	Lock detector transition from tracking to acquisition mode	$\|\Delta_{unt}\|$	6	—	8	%[1]
7	C	PLLON total stabilization delay (auto mode)[2]	t_{stab}	—	0.24	—	ms
8	D	PLLON acquisition mode stabilization delay[2]	t_{acq}	—	0.09	—	ms
9	D	PLLON tracking mode stabilization delay[2]	t_{al}	—	0.16	—	ms
10	D	Fitting parameter VCO loop gain	K_1	—	–195	—	MHz/V
11	D	Fitting parameter VCO loop frequency	f_1	—	126	—	MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$	—	38.5	—	µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$	—	3.5	—	µA
14	C	Jitter fit parameter 1[2]	j_1	—	0.9	1.3	%
15	C	Jitter fit parameter 2[2]	j_2	—	0.02	0.12	%

1 % deviation from target frequency

2 f_{osc} = 4 MHz, f_{BUS} = 40 MHz equivalent f_{VCO} = 80 MHz: REFDV = #$00, SYNR = #$09, C_S = 4.7 nF, C_P = 470 pF, R_S = 4.7 kΩ

A.6 MSCAN

Table A-24. MSCAN Wake-up Pulse Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN wakeup dominant pulse filtered	t_{WUP}	—	—	2	µs
2	P	MSCAN wakeup dominant pulse pass	t_{WUP}	5	—	—	µs