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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	119
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12xdp512vag

1.2.3.3 TEST — Test Pin

This input only pin is reserved for test. This pin has a pulldown device.

NOTE

The TEST pin must be tied to V_{SS} in all applications.

1.2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator. The input has a pullup device.

1.2.3.5 XFC — PLL Loop Filter Pin

Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

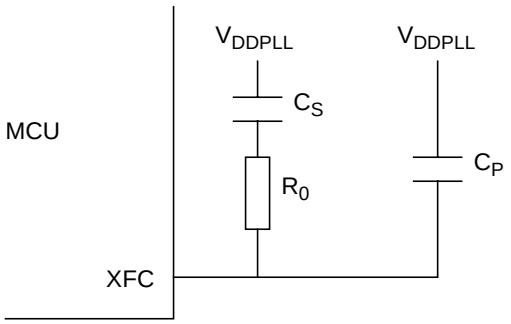

Figure 1-10. PLL Loop Filter Connections

1.2.3.6 BKGD / MODC — Background Debug and Mode Pin

The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pullup device.

1.2.3.7 PAD[23:8] / AN[23:8] — Port AD Input Pins of ATD1

PAD[23:8] are general-purpose input or output pins and analog inputs AN[23:8] of the analog-to-digital converter ATD1.

1.2.3.8 PAD[7:0] / AN[7:0] — Port AD Input Pins of ATD0

PAD[7:0] are general-purpose input or output pins and analog inputs AN[7:0] of the analog-to-digital converter ATD0.

1.2.3.9 PAD[15:0] / AN[15:0] — Port AD Input Pins of ATD1

PAD[15:0] are general-purpose input or output pins and analog inputs AN[15:0] of the analog-to-digital converter ATD1.

5.3.2.8 Reserved Register (ATDTEST0)

	7	6	5	4	3	2	1	0
R	U	U	U	U	U	U	U	U
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-10. Reserved Register (ATDTEST0)

Read: Anytime, returns unpredictable values

Write: Anytime in special modes, unimplemented in normal modes

NOTE

Writing to this register when in special modes can alter functionality.

5.3.2.9 ATD Test Register 1 (ATDTEST1)

This register contains the SC bit used to enable special channel conversions.

	7	6	5	4	3	2	1	0
R	U	U	0	0	0	0	0	SC
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-11. ATD Test Register 1 (ATDTEST1)

Read: Anytime, returns unpredictable values for Bit7 and Bit6

Write: Anytime

Table 5-18. ATDTEST1 Field Descriptions

Field	Description
0 SC	**Special Channel Conversion Bit** — If this bit is set, then special channel conversion can be selected using CC, CB and CA of ATDCTL5. Table 5-19 lists the coding. 0 Special channel conversions disabled 1 Special channel conversions enabled **Note:** Always write remaining bits of ATDTEST1 (Bit7 to Bit1) zero when writing SC bit. Not doing so might result in unpredictable ATD behavior.

Table 5-19. Special Channel Select Coding

SC	CC	CB	CA	Analog Input Channel
1	0	X	X	Reserved
1	1	0	0	V_{RH}
1	1	0	1	V_{RL}
1	1	1	0	$(V_{RH}+V_{RL}) / 2$
1	1	1	1	Reserved

BITL — Bit Test Immediate 8 bit Constant (Low Byte) — BITL

Operation

RD.L & IMM8 ⇒ NONE

Performs a bit wise logical AND between the low byte of register RD and an immediate 8 bit constant. Only the condition code flags get updated, but no result is written back.

CCR Effects

N	Z	V	C
Δ	Δ	0	—

N: Set if bit 7 of the result is set; cleared otherwise.
Z: Set if the 8 bit result is $00; cleared otherwise.
V: 0; cleared.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code							Cycles
BITL RD, #IMM8	IMM8	1	0	0	1	0	RD	IMM8	P

BLS Branch if Lower or Same BLS

Operation

If C | Z = 1, then PC + $0002 + (REL9 << 1) ⇒ PC

Branch instruction to compare unsigned numbers.

Branch if RS1 ≤ RS2:

```
SUB     R0,RS1,RS2
BLS     REL9
```

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code								Cycles
BLS REL9	REL9	0	0	1	1	0	0	1	REL9	PP/P

SSEM Set Semaphore SSEM

Operation

Attempts to set a semaphore. The state of the semaphore will be stored in the Carry-Flag:

1 = Semaphore is locked by the RISC core

0 = Semaphore is locked by the S12X_CPU

In monadic address mode, bits RS[2:0] select the semaphore to be set.

CCR Effects

N	Z	V	C
—	—	—	Δ

N: Not affected.

Z: Not affected.

V: Not affected.

C: Set if semaphore is locked by the RISC core; cleared otherwise.

Code and CPU Cycles

Source Form	Address Mode	Machine Code														Cycles
SSEM #IMM3	IMM3	0	0	0	0	0	IMM3	1	1	1	1	0	0	1	0	PA
SSEM RS	MON	0	0	0	0	0	RS	1	1	1	1	0	0	1	1	PA

- Internal timer for time-stamping of received and transmitted messages
- Three low-power modes: sleep, power down, and MSCAN enable
- Global initialization of configuration registers

10.1.4 Modes of Operation

The following modes of operation are specific to the MSCAN. See Section 10.4, "Functional Description," for details.

- Listen-Only Mode
- MSCAN Sleep Mode
- MSCAN Initialization Mode
- MSCAN Power Down Mode

10.2 External Signal Description

The MSCAN uses two external pins:

10.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

10.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

0 = Dominant state
1 = Recessive state

10.2.3 CAN System

A typical CAN system with MSCAN is shown in Figure 10-2. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations.

PIT operation in wait mode is controlled by the PITSWAI bit located in the PITCFLMT register. In wait mode, if the bus clock is globally enabled and if the PITSWAI bit is clear, the PIT operates like in run mode. In wait mode, if the PITSWAI bit is set, the PIT module is stalled.

- Stop mode

  In full stop mode or pseudo stop mode, the PIT module is stalled.

- Freeze mode

  PIT operation in freeze mode is controlled by the PITFRZ bit located in the PITCFLMT register. In freeze mode, if the PITFRZ bit is clear, the PIT operates like in run mode. In freeze mode, if the PITFRZ bit is set, the PIT module is stalled.

13.1.4 Block Diagram

Figure 13-1 shows a block diagram of the PIT.

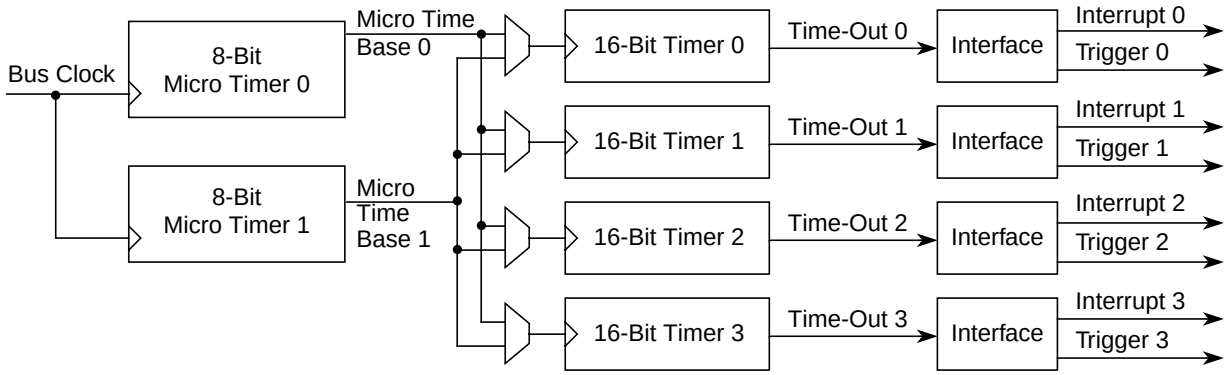

Figure 13-1. PIT Block Diagram

13.2 External Signal Description

The PIT module has no external pins.

14.2 External Signal Description

Due to the nature of VREG_3V3 being a voltage regulator providing the chip internal power supply voltages, most signals are power supply signals connected to pads.

Table 14-1 shows all signals of VREG_3V3 associated with pins.

Table 14-1. Signal Properties

Name	Function	Reset State	Pull Up
V_{DDR}	Power input (positive supply)	—	—
V_{DDA}	Quiet input (positive supply)	—	—
V_{SSA}	Quiet input (ground)	—	—
V_{DD}	Primary output (positive supply)	—	—
V_{SS}	Primary output (ground)	—	—
V_{DDPLL}	Secondary output (positive supply)	—	—
V_{SSPLL}	Secondary output (ground)	—	—
V_{REGEN} (optional)	Optional Regulator Enable	—	—

NOTE

Check device level specification for connectivity of the signals.

14.2.1 VDDR — Regulator Power Input Pins

Signal V_{DDR} is the power input of VREG_3V3. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (>=100 nF, X7R ceramic) between V_{DDR} and V_{SSR} (if V_{SSR} is not available V_{SS}) can smooth ripple on V_{DDR}.

For entering Shutdown Mode, pin V_{DDR} should also be tied to ground on devices without VREGEN pin.

14.2.2 VDDA, VSSA — Regulator Reference Supply Pins

Signals $V_{DDA}/V_{SSA,}$ which are supposed to be relatively quiet, are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (>=100 nF, X7R ceramic) between V_{DDA} and V_{SSA} can further improve the quality of this supply.

14.2.3 VDD, VSS — Regulator Output1 (Core Logic) Pins

Signals V_{DD}/V_{SS} are the primary outputs of VREG_3V3 that provide the power supply for the core logic. These signals are connected to device pins to allow external decoupling capacitors (220 nF, X7R ceramic).

In Shutdown Mode an external supply driving V_{DD}/V_{SS} can replace the voltage regulator.

17.4.3 Chip Access Restrictions

17.4.3.1 Illegal XGATE Accesses

A possible access error is flagged by the MMC and signalled to XGATE under the following conditions:

- XGATE performs misaligned word (in case of load-store or opcode or vector fetch accesses).
- XGATE accesses the register space (in case of opcode or vector fetch).
- XGATE performs a write to Flash in any modes (in case of load-store access).
- XGATE performs an access to a secured Flash in expanded modes (in case of load-store or opcode or vector fetch accesses).
- XGATE performs a write to non-XGATE region in RAM (RAM protection mechanism) (in case of load-store access).

For further details refer to the XGATE Block Guide.

17.4.3.2 Illegal CPU Accesses

After programming the protection mechanism registers (see Figure 1-17, Figure 1-18, Figure 1-19, and Figure 1-20) and setting the RWPE bit (see Figure 1-17) there are 3 regions recognized by the MMC module:

1. XGATE RAM region
2. CPU RAM region
3. Shared Region (XGATE AND CPU)

If the RWPE bit is set the CPU write accesses into the XGATE RAM region are blocked. If the CPU tries to write the XGATE RAM region the AVIF bit is set and an interrupt is generated if enabled. Furthermore if the XGATE tries to write to outside of the XGATE RAM or shared regions and the RWPE bit is set, the write access is suppressed and the access error will be flagged to the XGATE module (see Section 1.4.3.1, “Illegal XGATE Accesses” and the XGATE Block Guide).

The bottom address of the XGATE RAM region always starts at the lowest implemented RAM address.

The values stored in the boundary registers define the boundary addresses in 256 byte steps. The 256 byte block selected by any of the registers is always included in the respective region. For example setting the shared region lower boundary register (RAMSHL) to $C1 and the shared region upper boundary register (RAMSHU) to $E0 defines the shared region from address $0F_C100 to address $0F_E0FF in the global memory space (see Figure 1-25).

The interrupt requests generated by the MMC are listed in Table 1-23. Refer to the Device User Guide for the related interrupt vector address and interrupt priority.

19.3.1.3 Debug Trace Control Register (DBGTCR)

0x0022

	7	6	5	4	3	2	1	0
R W	TSOURCE		TRANGE		TRCMOD		TALIGN	
Reset	0	0	0	0	0	0	0	0

Figure 19-5. Debug Trace Control Register (DBGTCR)

Read: Anytime

Write: Bits 7:6 only when DBG is neither secure nor armed.
Bits 5:0 anytime the module is disarmed.

Table 19-8. DBGTCR Field Descriptions

Field	Description
7–6 TSOURCE	**Trace Source Control Bits** — The TSOURCE bits select the data source for the tracing session. If the MCU system is secured, these bits cannot be set and tracing is inhibited. See Table 19-9.
5–4 TRANGE[5:4]	**Trace Range Bits** —The TRANGE bits allow filtering of trace information from a selected address range when tracing from the CPU in detail mode. The XGATE tracing range cannot be narrowed using these bits. To use a comparator for range filtering, the corresponding COMPE and SRC bits must remain cleared. If the COMPE bit is not clear then the comparator will also be used to generate state sequence triggers or tags. If the SRC bit is set the comparator is mapped to the XGATE busses, corrupting the trace. See Table 19-10.
3–2 TRCMOD[3:2]	**Trace Mode Bits** — See Section 19.4.5.2, “Trace Modes“ for detailed trace mode descriptions. In normal mode, change of flow information is stored. In loop1 mode, change of flow information is stored but redundant entries into trace memory are inhibited. In detail mode, address and data for all memory and register accesses is stored. See Table 19-11
1–0 TALIGN[1:0]	**Trigger Align Bits** — These bits control whether the trigger is aligned to the beginning, end or the middle of a tracing session. See Table 19-12.

Table 19-9. TSOURCE Trace Source Bit Encoding

TSOURCE	Tracing Source
00	No tracing requested
01	CPU
10[1]	XGATE
11[1, 2]	Both CPU and XGATE

1 No range limitations are allowed. Thus tracing operates as if TRANGE = 00.

2 No detail mode tracing supported. If TRCMOD =10, no information is stored.

Table 19-10. TRANGE Trace Range Encoding

TRANGE	Tracing Source
00	Trace from all addresses (No filter)
01	Trace only in address range from 0x0000 to comparator D
10	Trace only in address range from comparator C to 0x7FFFFF

Table 19-10. TRANGE Trace Range Encoding

TRANGE	Tracing Source
11	Trace only in range from comparator C to comparator D

Table 19-11. TRCMOD Trace Mode Bit Encoding

TRCMOD	Description
00	NORMAL
01	LOOP1
10	DETAIL
11	Reserved

Table 19-12. TALIGN Trace Alignment Encoding

TALIGN	Description
00	Trigger at end of stored data
01	Trigger before storing data
10	Trace buffer entries before and after trigger
11	Reserved

19.3.1.4 Debug Control Register2 (DBGC2)

0x0023

	7	6	5	4	3	2	1	0
R	0	0	0	0	CDCM		ABCM	
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 19-6. Debug Control Register2 (DBGC2)

Read: Anytime

Write: Anytime the module is disarmed.

This register configures the comparators for range matching.

Table 19-13. DBGC2 Field Descriptions

Field	Description
3–2 CDCM[3:2]	**C and D Comparator Match Control** — These bits determine the C and D comparator match mapping as described in Table 19-14.
1–0 ABCM[1:0]	**A and B Comparator Match Control** — These bits determine the A and B comparator match mapping as described in Table 19-15.

19.4.6.1 External Tagging using $\overline{\text{TAGHI}}$ and $\overline{\text{TAGLO}}$

External tagging using the external $\overline{\text{TAGHI}}$ and $\overline{\text{TAGLO}}$ pins can only be used to tag CPU opcodes; tagging of XGATE code using these pins is not possible. An external tag triggers the state sequencer into State0 when the tagged opcode reaches the execution stage of the instruction queue.

The pins operate independently, thus the state of one pin does not affect the function of the other. External tagging is possible in emulation modes only. The presence of logic level 0 on either pin at the rising edge of the external clock (ECLK) performs the function indicated in the Table 19-43. It is possible to tag both bytes of an instruction word. If a taghit comes from the low or high byte, a breakpoint generated according to the DBGBRK and BDM bits in DBGC1. Each time $\overline{\text{TAGHI}}$ or $\overline{\text{TAGLO}}$ are low on the rising edge of ECLK, the old tag is replaced by a new one

Table 19-43. Tag Pin Function

$\overline{\text{TAGHI}}$	$\overline{\text{TAGLO}}$	Tag
1	1	No tag
1	0	Low byte
0	1	High byte
0	0	Both bytes

19.4.7 Breakpoints

It is possible to select breakpoints to the XGATE and let the CPU continue operation, setting DBGBRK[0], or breakpoints to the CPU and let the XGATE continue operation setting, DBGBRK[1], or a breakpoint to both CPU and XGATE, setting both bits DBGBRK[1:0].

There are several ways to generate breakpoints to the XGATE and CPU modules.

- Through XGATE software breakpoint requests.
- From comparator channel triggers to final state.
- Using software to write to the TRIG bit in the DBGC1 register.
- From taghits generated using the external TAGHI and TAGLO pins.

19.4.7.1 XGATE Software Breakpoints

The XGATE software breakpoint instruction BRK can request an CPU breakpoint, via the DBG module. In this case, if the XGSBPE bit is set, the DBG module immediately generates a forced breakpoint request to the CPU, the state sequencer is returned to state0 and tracing, if active, is terminated. If configured for begin-trigger and tracing has not yet been triggered from another source, the trace buffer contains no new information. Breakpoint requests from the XGATE module do not depend upon the state of the DBGBRK or ARM bits in DBGC1. They depend solely on the state of the XGSBPE and BDM bits. Thus it is not necessary to ARM the DBG module to use XGATE software breakpoints to generate breakpoints in the CPU program flow, but it is necessary to set XGSBPE. Furthermore if a breakpoint to BDM is required, the BDM bit must also be set. When the XGATE requests an CPU breakpoint, the XGATE program flow stops by default, independent of the DBG module. The user can thus determine if an XGATE breakpoint has occurred by reading out the XGATE program counter over the BDM interface.

21.1.3 Block Diagram

Figure 21-1 is a block diagram of the XEBI with all related I/O signals.

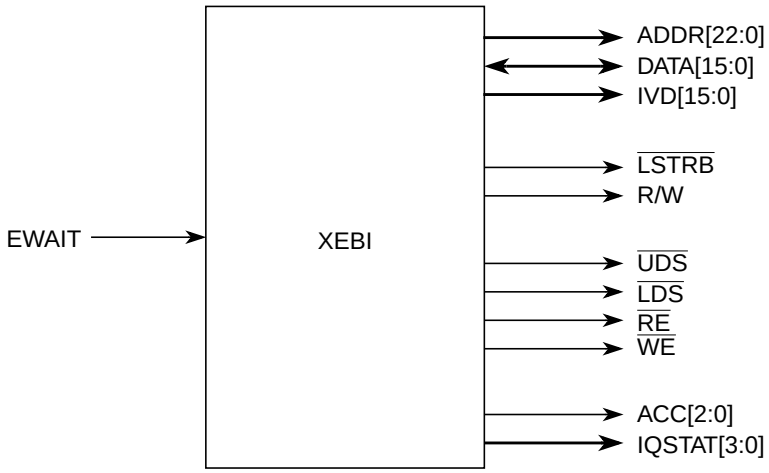

Figure 21-1. XEBI Block Diagram

21.2 External Signal Description

The user is advised to refer to the SoC section for port configuration and location of external bus signals.

NOTE

The following external bus related signals are described in other sections:
$\overline{CS2}$, $\overline{CS1}$, $\overline{CS0}$ (chip selects) — S12X_MMC section
ECLK, ECLKX2 (free-running clocks) — PIM section
$\overline{TAGHI}$, $\overline{TAGLO}$ (tag inputs) — PIM section, S12X_DBG section

Table 21-1 outlines the pin names and gives a brief description of their function. Refer to the SoC section and PIM section for reset states of these pins and associated pull-ups or pull-downs.

22.3.2.30 Port M Data Register (PTM)

	7	6	5	4	3	2	1	0
R W	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
CAN	TXCAN3	RXCAN3	TXCAN2	RXCAN2	TXCAN1	RXCAN1	TXCAN0	RXCAN0
Routed CAN0			TXCAN0	RXCAN0	TXCAN0	RXCAN0		
Routed CAN4	TXCAN4	RXCAN4	TXCAN4	RXCAN4				
Routed SPIO			SCK0	MOSI0	$\overline{SS0}$	MISO0		
Reset	0	0	0	0	0	0	0	0

Figure 22-32. Port M Data Register (PTM)

Read: Anytime.

Write: Anytime.

Port M pins 75–0 are associated with the CAN0, CAN1, CAN2, CAN3, SCI3, as well as the routed CAN0, CAN4, and SPI0 modules. When not used with any of the peripherals, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level “1”, a read returns the value of the port register, otherwise the buffered pin input state is read.

Table 22-32. PTM Field Descriptions

Field	Description
7–6 PTM[7:6]	The CAN3 function (TXCAN3 and RXCAN3) takes precedence over the CAN4, SCI3 and the general purpose I/O function if the CAN3 module is enabled. *Refer to MSCAN section for details.* The CAN4 function (TXCAN4 and RXCAN4) takes precedence over the SCI3 and the general purpose I/O function if the CAN4 module is enabled. *Refer to MSCAN section for details.* The SCI3 function (TXD3 and RXD3) takes precedence over the general purpose I/O function if the SCI3 module is enabled. *Refer to SCI section for details.*
5–4 PTM[5:4]	The CAN2 function (TXCAN2 and RXCAN2) takes precedence over the routed CAN0, routed CAN4, the routed SPI0 and the general purpose I/O function if the CAN2 module is enabled{pim_9xd_prio.m}. The routed CAN0 function (TXCAN0 and RXCAN0) takes precedence over the routed CAN4, the routed SPI0 and the general purpose I/O function if the routed CAN0 module is enabled. The routed CAN4 function (TXCAN4 and RXCAN4) takes precedence over the routed SPI0 and general purpose I/O function if the routed CAN4 module is enabled. *Refer to MSCAN section for details.* The routed SPI0 function (SCK0 and MOSI0) takes precedence of the general purpose I/O function if the routed SPI0 is enabled. *Refer to SPI section for details.*

22.3.2.41 Port P Reduced Drive Register (RDRP)

	7	6	5	4	3	2	1	0
R W	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Reset	0	0	0	0	0	0	0	0

Figure 22-43. Port P Reduced Drive Register (RDRP)

Read: Anytime.

Write: Anytime.

This register configures the drive strength of each port P output pin as either full or reduced. If the port is used as input this bit is ignored.

Table 22-40. RDRP Field Descriptions

Field	Description
7–0 RDRP[7:0]	**Reduced Drive Port P** 0 Full drive strength at output. 1 Associated pin drives at about 1/6 of the full drive strength.

22.3.2.42 Port P Pull Device Enable Register (PERP)

	7	6	5	4	3	2	1	0
R W	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
Reset	0	0	0	0	0	0	0	0

Figure 22-44. Port P Pull Device Enable Register (PERP)

Read: Anytime.

Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

Table 22-41. PERP Field Descriptions

Field	Description
7–0 PERP[7:0]	**Pull Device Enable Port P** 0 Pull-up or pull-down device is disabled. 1 Either a pull-up or pull-down device is enabled.

22.3.2.64 Port AD0 Reduced Drive Register 1 (RDR1AD0)

	7	6	5	4	3	2	1	0
R W	RDR1AD07	RDR1AD06	RDR1AD05	RDR1AD04	RDR1AD03	RDR1AD02	RDR1AD01	RDR1AD00
Reset	0	0	0	0	0	0	0	0

Figure 22-66. Port AD0 Reduced Drive Register 1 (RDR1AD0)

Read: Anytime.

Write: Anytime.

This register configures the drive strength of each output pin PAD[07:00] as either full or reduced. If the port is used as input this bit is ignored.

Table 22-59. RDR1AD0 Field Descriptions

Field	Description
7–0 RDR1AD0[7:0]	**Reduced Drive Port AD0 Register 1** 0 Full drive strength at output. 1 Associated pin drives at about 1/6 of the full drive strength.

22.3.2.65 Port AD0 Pull Up Enable Register 1 (PER1AD0)

	7	6	5	4	3	2	1	0
R W	PER1AD07	PER1AD06	PER1AD05	PER1AD04	PER1AD03	PER1AD02	PER1AD01	PER1AD00
Reset	0	0	0	0	0	0	0	0

Figure 22-67. Port AD0 Pull Up Enable Register 1 (PER1AD0)

Read: Anytime.

Write: Anytime.

This register activates a pull-up device on the respective pin PAD[07:00] if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

Table 22-60. PER1AD0 Field Descriptions

Field	Description
7–0 PER1AD0[7:0]	**Pull Device Enable Port AD0 Register 1** 0 Pull-up device is disabled. 1 Pull-up device is enabled.

Table 23-1. Pin Functions and Priorities (Sheet 5 of 7)

Port	Pin Name	Pin Function and Priority	I/O	Description	Pin Function after Reset
P	PP7	PWM7	I/O	Pulse Width Modulator input/output channel 7	GPIO
		SCK2	I/O	Serial Peripheral Interface 2 serial clock pin	
		GPIO/KWP7	I/O	General-purpose I/O with interrupt	
	PP6	PWM6	O	Pulse Width Modulator output channel 6	
		$\overline{SS2}$	I/O	Serial Peripheral Interface 2 slave select output in master mode, input for slave mode or master mode.	
		GPIO/KWP6	I/O	General-purpose I/O with interrupt	
	PP5	PWM5	O	Pulse Width Modulator output channel 5	
		MOSI2	I/O	Serial Peripheral Interface 2 master out/slave in pin	
		GPIO/KWP5	I/O	General-purpose I/O with interrupt	
	PP4	PWM4	O	Pulse Width Modulator output channel 4	
		MISO2	I/O	Serial Peripheral Interface 2 master in/slave out pin	
		GPIO/KWP4	I/O	General-purpose I/O with interrupt	
	PP3	PWM3	O	Pulse Width Modulator output channel 3	
		$\overline{SS1}$	I/O	Serial Peripheral Interface 1 slave select output in master mode, input for slave mode or master mode.	
		GPIO/KWP3	I/O	General-purpose I/O with interrupt	
	PP2	PWM2	O	Pulse Width Modulator output channel 2	
		SCK1	I/O	Serial Peripheral Interface 1 serial clock pin	
		GPIO/KWP2	I/O	General-purpose I/O with interrupt	
	PP1	PWM1	O	Pulse Width Modulator output channel 1	
		MOSI1	I/O	Serial Peripheral Interface 1 master out/slave in pin	
		GPIO/KWP1	I/O	General-purpose I/O with interrupt	
	PP0	PWM0	O	Pulse Width Modulator output channel 0	
		MISO1	I/O	Serial Peripheral Interface 1 master in/slave out pin	
		GPIO/KWP0	I/O	General-purpose I/O with interrupt	

Table 24-40. PIFP Field Descriptions

Field	Description
7–0 PIFP[7:0]	**Interrupt Flags Port P** 0 No active edge pending. Writing a “0” has no effect. 1 Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set). Writing a logic level “1” clears the associated flag.

24.0.5.42 Port H Data Register (PTH)

	7	6	5	4	3	2	1	0
R W	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
Routed SPI					$\overline{SS1}$	SCK1	MOSI1	MISO1
Reset	0	0	0	0	0	0	0	0

Figure 24-44. Port H Data Register (PTH)

Read: Anytime.

Write: Anytime.

Port H pins 7–0 are associated with the routed SPI1.

These pins can be used as general purpose I/O when not used with any of the peripherals.

If the data direction bits of the associated I/O pins are set to logic level “1”, a read returns the value of the port register, otherwise the buffered pin input state is read.

The routed SPI1 function takes precedence over the general purpose I/O function if the routed SPI1 is enabled. *Refer to SPI section for details.*

24.0.5.43 Port H Input Register (PTIH)

	7	6	5	4	3	2	1	0
R	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
W								
Reset[1]	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 24-45. Port H Input Register (PTIH)

1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Read: Anytime.

Write: Never, writes to this register have no effect.

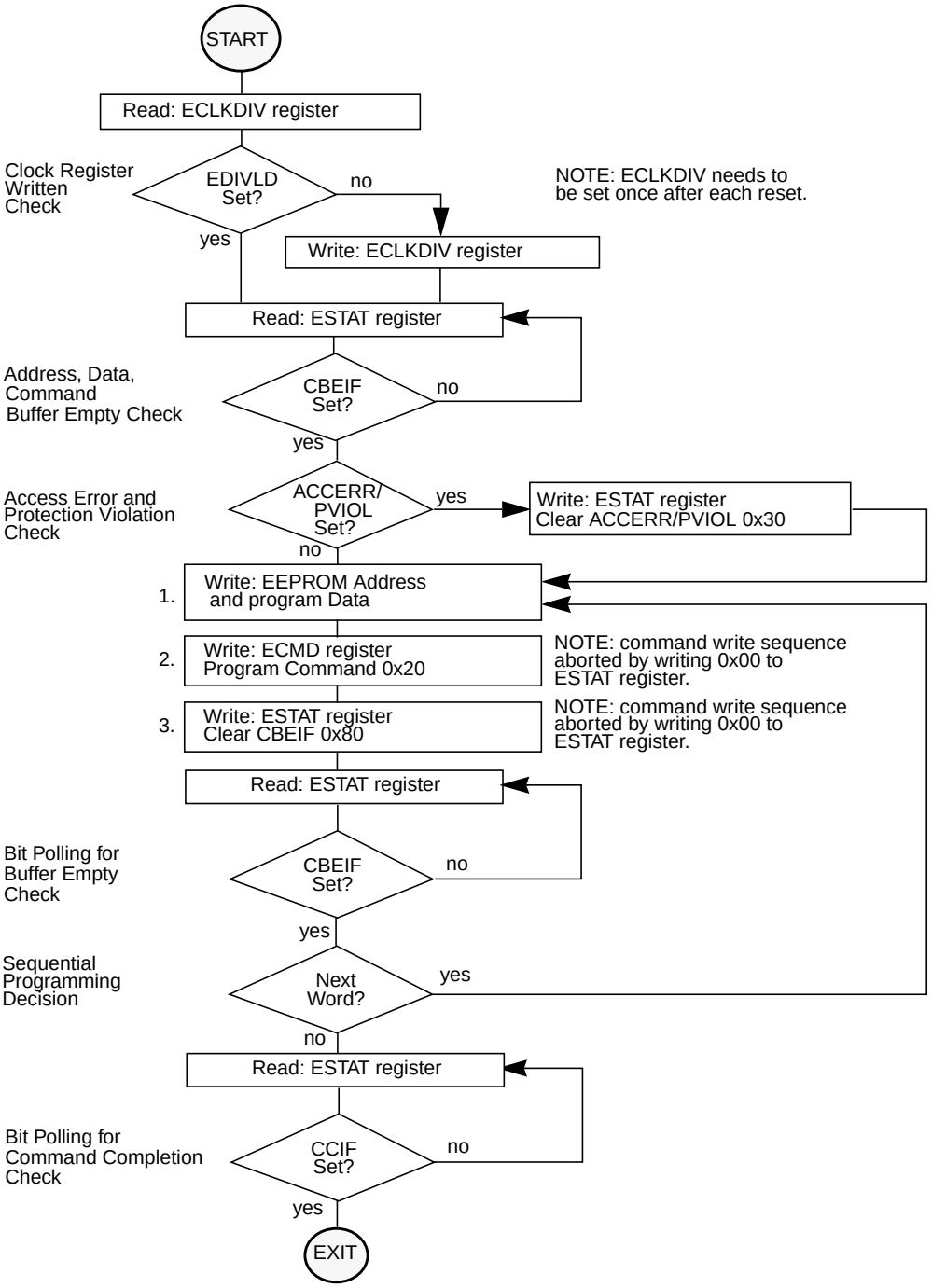

Figure 25-19. Example Program Command Flow

0x02C0–0x02DF Analog-to-Digital Converter 10-Bit 8-Channel (ATD0) Map (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02D6	ATD0DR3H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x02D7	ATD0DR3L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x02D8	ATD0DR4H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x02D9	ATD0DR4L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x02DA	ATD0DR5H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x02DB	ATD0DR5L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x02DC	ATD0DR6H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x02DD	ATD0DR6L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x02DE	ATD0DR7H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x02DF	ATD0DR7L	R	Bit7	Bit6	0	0	0	0	0	0
		W								

0x02E0–0x02EF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02E0–0x02EF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x02F0–0x02F7 Voltage Regulator (VREG_3V3) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F0	VREGHTCL	R	Reserved for Factory Test							
		W								
0x02F1	VREGCTRL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x02F2	VREGAPICL	R	APICLK	0	0	0	0	APIFE	APIE	APIF
		W								
0x02F3	VREGAPITR	R	APITR5	APITR4	APITR3	APITR2	APITR1	APITR0	0	0
		W								
0x02F4	VREGAPIRH	R	0	0	0	0	APIR11	APIR10	APIR9	APIR8
		W								
0x02F5	VREGAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x02F6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02F7	Reserved	R	0	0	0	0	0	0	0	0
		W								