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Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
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Chapter 5Analog-to-Digital Converter (S12ATD10B8CV3)

Chapter 6
XGATE (S12XGATEV2)

1.2.2 Signal Properties Summary

Table 1-7 summarizes the pin functionality of the MC9S12XDP512. For available modules on other parts of the S12XD, S12XB and S12XA family please refer to Appendix E Derivative Differences.

Table 1-7. Signal Properties Summary (Sheet 1 of 4)

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Pin Name Function 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
EXTAL	—	—	—	—	V_{DDPLL}	NA	NA	Oscillator pins
XTAL	—	—	—	—	V_{DDPLL}	NA	NA	
$\overline{\text{RESET}}$	—	—	—	—	V_{DDR}	PULLUP		External reset
TEST	—	—	—	—	N.A.	$\overline{\text{RESET}}$ pin	DOWN	Test input
VREGEN	—	—	—	—	V_{DDX}	PUCR	Up	Voltage regulator enable Input
XFC	—	—	—	—	V_{DDPLL}	NA	NA	PLL loop filter
BKGD	MODC	—	—	—	V_{DDX}	Always on	Up	Background debug
PAD[23:08]	AN[23:8]	—	—	—	V_{DDA}	PER0/ PER1	Disabled	Port AD I/O, Port AD inputs of ATD1 and analog inputs of ATD1
PAD[07:00]	AN[7:0]	—	—	—	V_{DDA}	PER1	Disabled	Port AD I/O, Port AD inputs of ATD0 and analog inputs of ATD0
PA[7:0]	—	—	—	—	V_{DDR}	PUCR	Disabled	Port A I/O
PB[7:0]	—	—	—	—	V_{DDR}	PUCR	Disabled	Port BI/O
PA[7:0]	ADDR[15:8]	IVD[15:8]	—	—	V_{DDR}	PUCR	Disabled	Port A I/O, address bus, internal visibility data
PB[7:1]	ADDR[7:1]	IVD[7:0]	—	—	V_{DDR}	PUCR	Disabled	Port B I/O, address bus, internal visibility data
PB0	ADDR0	$\overline{\text{UDS}}$			V_{DDR}	PUCR	Disabled	Port B I/O, address bus, upper data strobe
PC[7:0]	DATA[15:8]	—	—	—	V_{DDR}	PUCR	Disabled	Port C I/O, data bus
PD[7:0]	DATA[7:0]	—	—	—	V_{DDR}	PUCR	Disabled	Port D I/O, data bus
PE7	ECLKX2	$\overline{\text{XCLKS}}$	—	—	V_{DDR}	PUCR	Up	Port E I/O, system clock output, clock select
PE6	$\overline{\text{TAGHI}}$	MODB	—	—	V_{DDR}	While $\overline{\text{RESET}}$ pin is low: down		Port E I/O, tag high, mode input
PE5	$\overline{\text{RE}}$	MODA	$\overline{\text{TAGLO}}$	—	V_{DDR}	While $\overline{\text{RESET}}$ pin is low: down		Port E I/O, read enable, mode input, tag low input
PE4	ECLK	—	—	—	V_{DDR}	PUCR	Up	Port E I/O, bus clock output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{LDS}}$	EROMCTL	—	V_{DDR}	PUCR	Up	Port E I/O, low byte data strobe, EROMON control
PE2	R/$\overline{\text{W}}$	$\overline{\text{WE}}$	—	—	V_{DDR}	PUCR	Up	Port E I/O, read/write
PE1	$\overline{\text{IRQ}}$	—	—	—	V_{DDR}	PUCR	Up	Port E Input, maskable interrupt

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
ATDD47H	10-BIT	0	0	0	0	0	0	BIT 9 MSB	BIT 8
	8-BIT	0	0	0	0	0	0	0	0
	W								
ATDD47L	10-BIT	BIT 7 BIT 7 MSB	BIT 6 BIT 6	BIT 5 BIT 5	BIT 4 BIT 4	BIT 3 BIT 3	BIT 2 BIT 2	BIT 1 BIT 1	BIT 0 BIT 0
	8-BIT								

= Unimplemented or Reserved

Figure 5-2. ATD Register Summary (Sheet 5 of 5)

5.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence but will not start a new sequence.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	0	1	1	1

= Unimplemented or Reserved

Figure 5-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime

Table 5-1. ATDCTL0 Field Descriptions

Field	Description
2–0 WRAP[2:0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 5-2.

Table 5-2. Multi-Channel Wrap Around Coding

WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wrap Around to AN0 after Converting
0	0	0	Reserved
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

8.4.2.2 PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

8.4.2.3 PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect “immediately” by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, since the counter is readable, it is possible to know where the count is with respect to the duty value and software can be used to make adjustments

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

8.4.2.4 PWM Timer Counters

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source (see Section 8.4.1, “PWM Clock Select” for the available clock sources and rates). The counter compares to two registers, a duty register and a period register as shown in Figure 8-19. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register behaves differently depending on what output mode is selected as shown in Figure 8-19 and described in Section 8.4.2.5, “Left Aligned Outputs” and Section 8.4.2.6, “Center Aligned Outputs”.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0002 CANBTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
	W								
0x0003 CANBTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
	W								
0x0004 CANRFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
	W								
0x0005 CANRIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
	W								
0x0006 CANTFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
	W								
0x0007 CANTIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
	W								
0x0008 CANTARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
	W								
0x0009 CANTAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
	W								
0x000A CANTBSEL	R	0	0	0	0	0	TX2	TX1	TX0
	W								
0x000B CANIDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
	W								
0x000C Reserved	R	0	0	0	0	0	0	0	0
	W								
0x000D CANMISC	R	0	0	0	0	0	0	0	BOHOLD
	W								
0x000E CANRXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
	W								
0x000F CANTXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
	W								
0x0010–0x0013 CANIDAR0–3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	W								

= Unimplemented or Reserved u = Unaffected

Figure 10-3. MSCAN Register Summary (continued)

Table 10-2. CANCTL1 Register Field Descriptions (continued)

Field	Description
1 SLPAK	**Sleep Mode Acknowledge** — This flag indicates whether the MSCAN module has entered sleep mode (see Section 10.4.5.4, "MSCAN Sleep Mode"). It is used as a handshake flag for the SLPRQ sleep mode request. Sleep mode is active when SLPRQ = 1 and SLPAK = 1. Depending on the setting of WUPE, the MSCAN will clear the flag if it detects activity on the CAN bus while in sleep mode. 0 Running — The MSCAN operates normally 1 Sleep mode active — The MSCAN has entered sleep mode
0 INITAK	**Initialization Mode Acknowledge** — This flag indicates whether the MSCAN module is in initialization mode (see Section 10.4.5.5, "MSCAN Initialization Mode"). It is used as a handshake flag for the INITRQ initialization mode request. Initialization mode is active when INITRQ = 1 and INITAK = 1. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0–CANIDAR7, and CANIDMR0–CANIDMR7 can be written only by the CPU when the MSCAN is in initialization mode. 0 Running — The MSCAN operates normally 1 Initialization mode active — The MSCAN has entered initialization mode

10.3.2.3 MSCAN Bus Timing Register 0 (CANBTR0)

The CANBTR0 register configures various CAN bus timing parameters of the MSCAN module.

	7	6	5	4	3	2	1	0
R W	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
Reset:	0	0	0	0	0	0	0	0

Figure 10-6. MSCAN Bus Timing Register 0 (CANBTR0)

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 10-3. CANBTR0 Register Field Descriptions

Field	Description
7:6 SJW[1:0]	**Synchronization Jump Width** — The synchronization jump width defines the maximum number of time quanta (Tq) clock cycles a bit can be shortened or lengthened to achieve resynchronization to data transitions on the CAN bus (see Table 10-4).
5:0 BRP[5:0]	**Baud Rate Prescaler** — These bits determine the time quanta (Tq) clock which is used to build up the bit timing (see Table 10-5).

Table 10-4. Synchronization Jump Width

SJW1	SJW0	Synchronization Jump Width
0	0	1 Tq clock cycle
0	1	2 Tq clock cycles
1	0	3 Tq clock cycles
1	1	4 Tq clock cycles

field of the CAN frame, is received into the next available RxBG. If the MSCAN receives an invalid message in its RxBG (wrong identifier, transmission errors, etc.) the actual contents of the buffer will be over-written by the next message. The buffer will then not be shifted into the FIFO.

When the MSCAN module is transmitting, the MSCAN receives its own transmitted messages into the background receive buffer, RxBG, but does not shift it into the receiver FIFO, generate a receive interrupt, or acknowledge its own messages on the CAN bus. The exception to this rule is in loopback mode (see Section 10.3.2.2, "MSCAN Control Register 1 (CANCTL1)") where the MSCAN treats its own messages exactly like all other incoming messages. The MSCAN receives its own transmitted messages in the event that it loses arbitration. If arbitration is lost, the MSCAN must be prepared to become a receiver.

An overrun condition occurs when all receive message buffers in the FIFO are filled with correctly received messages with accepted identifiers and another message is correctly received from the CAN bus with an accepted identifier. The latter message is discarded and an error interrupt with overrun indication is generated if enabled (see Section 10.4.7.5, "Error Interrupt"). The MSCAN remains able to transmit messages while the receiver FIFO being filled, but all incoming messages are discarded. As soon as a receive buffer in the FIFO is available again, new valid messages will be accepted.

10.4.3 Identifier Acceptance Filter

The MSCAN identifier acceptance registers (see Section 10.3.2.12, "MSCAN Identifier Acceptance Control Register (CANIDAC)") define the acceptable patterns of the standard or extended identifier (ID[10:0] or ID[28:0]). Any of these bits can be marked 'don't care' in the MSCAN identifier mask registers (see Section 10.3.2.18, "MSCAN Identifier Mask Registers (CANIDMR0–CANIDMR7)").

A filter hit is indicated to the application software by a set receive buffer full flag (RXF = 1) and three bits in the CANIDAC register (see Section 10.3.2.12, "MSCAN Identifier Acceptance Control Register (CANIDAC)"). These identifier hit flags (IDHIT[2:0]) clearly identify the filter section that caused the acceptance. They simplify the application software's task to identify the cause of the receiver interrupt. If more than one hit occurs (two or more filters match), the lower hit has priority.

A very flexible programmable generic identifier acceptance filter has been introduced to reduce the CPU interrupt loading. The filter is programmable to operate in four different modes (see Bosch CAN 2.0A/B protocol specification):

- Two identifier acceptance filters, each to be applied to:
  - The full 29 bits of the extended identifier and to the following bits of the CAN 2.0B frame:
    - Remote transmission request (RTR)
    - Identifier extension (IDE)
    - Substitute remote request (SRR)
  - The 11 bits of the standard identifier plus the RTR and IDE bits of the CAN 2.0A/B messages[1]. This mode implements two filters for a full length CAN 2.0B compliant extended identifier. Figure 10-40 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces a filter 0 hit. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces a filter 1 hit.

1.Although this mode can be used for standard identifiers, it is recommended to use the four or eight identifier acceptance filters for standard identifiers

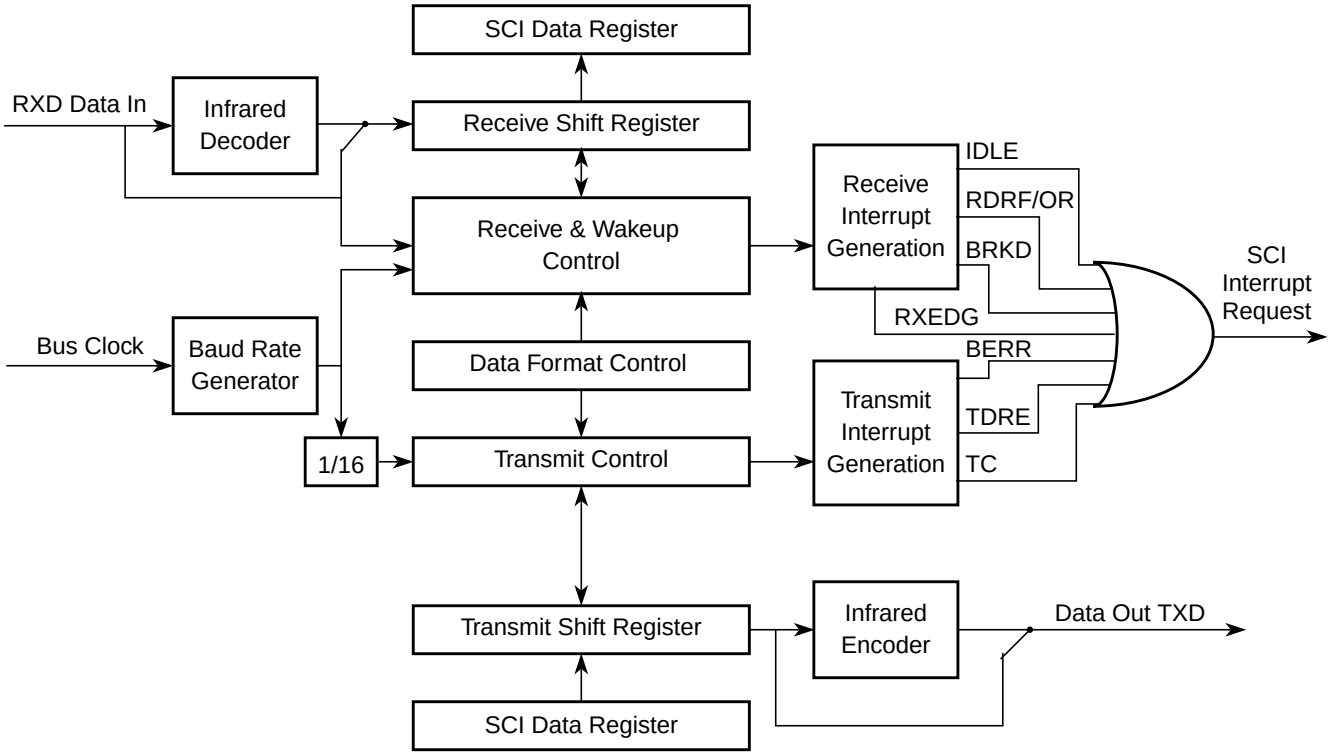

Figure 11-1. SCI Block Diagram

PIT operation in wait mode is controlled by the PITSWAI bit located in the PITCFLMT register. In wait mode, if the bus clock is globally enabled and if the PITSWAI bit is clear, the PIT operates like in run mode. In wait mode, if the PITSWAI bit is set, the PIT module is stalled.

- Stop mode

  In full stop mode or pseudo stop mode, the PIT module is stalled.

- Freeze mode

  PIT operation in freeze mode is controlled by the PITFRZ bit located in the PITCFLMT register. In freeze mode, if the PITFRZ bit is clear, the PIT operates like in run mode. In freeze mode, if the PITFRZ bit is set, the PIT module is stalled.

13.1.4 Block Diagram

Figure 13-1 shows a block diagram of the PIT.

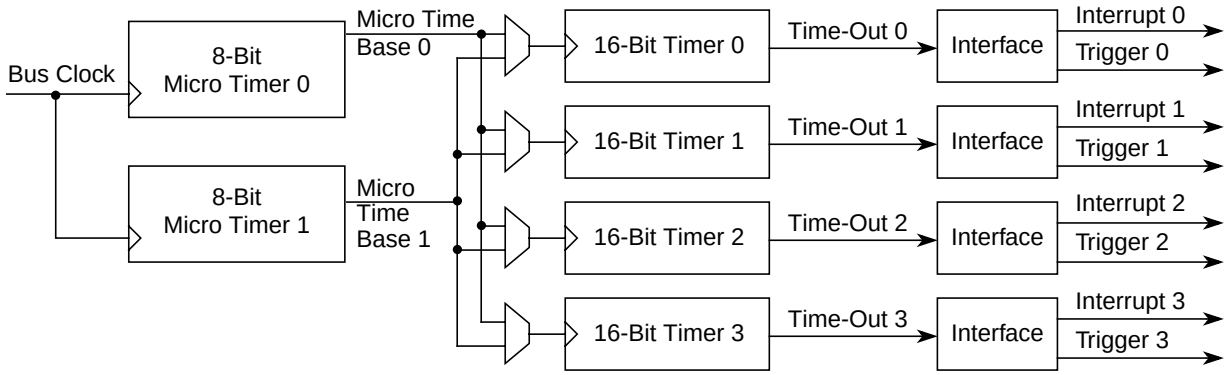

Figure 13-1. PIT Block Diagram

13.2 External Signal Description

The PIT module has no external pins.

19.3.1.11.4 Debug Comparator Address Low Register (DBGXAL)

0x002B

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 19-17. Debug Comparator Address Low Register (DBGXAL)

Read: Anytime

Write: Anytime when DBG not armed.

Table 19-31. DBGXAL Field Descriptions

Field	Description
7–0 Bits [7:0]	**Comparator Address Low Compare Bits** — The comparator address low compare bits control whether the selected comparator will compare the address bus bits [7:0] to a logic 1 or logic 0. 0 Compare corresponding address bit to a logic 0 1 Compare corresponding address bit to a logic 1

19.3.1.11.5 Debug Comparator Data High Register (DBGXDH)

0x002C

	7	6	5	4	3	2	1	0
R W	Bit 15	14	13	12	11	10	9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 19-18. Debug Comparator Data High Register (DBGXDH)

Read: Anytime

Write: Anytime when DBG not armed.

Table 19-32. DBGXDH Field Descriptions

Field	Description
7–0 Bits [15:8]	**Comparator Data High Compare Bits** — The comparator data high compare bits control whether the selected comparator compares the data bus bits [15:8] to a logic 1 or logic 0. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparators A and C. 0 Compare corresponding data bit to a logic 0 1 Compare corresponding data bit to a logic 1

Table 20-5. COMRV Encoding

COMRV	Visible Comparator	Visible Register at 0x0027
10	Comparator C	DBGSCR3
11	Comparator D	DBGMFR

20.3.2.5 Debug Trace Buffer Register (DBGTBH:DBGTBL)

Address: 0x0024, 0x0025

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 20-7. Debug Trace Buffer Register (DBGTB)

Read: Anytime when unlocked and not secured and not armed.

Write: Aligned word writes when disarmed unlock the trace buffer for reading but do not affect trace buffer contents.

Table 20-16. DBGTB Field Descriptions

Field	Description
15–0 Bit[15:0]	**Trace Buffer Data Bits** — The Trace Buffer Register is a window through which the 64-bit wide data lines of the Trace Buffer may be read 16 bits at a time. Each valid read of DBGTB increments an internal trace buffer pointer which points to the next address to be read. When the ARM bit is written to 1 the trace buffer is locked to prevent reading. The trace buffer can only be unlocked for reading by writing to DBGTB with an aligned word write when the module is disarmed. The DBGTB register can be read only as an aligned word, any byte reads or misaligned access of these registers will return 0 and will not cause the trace buffer pointer to increment to the next trace buffer address. The same is true for word reads while the debugger is armed. System resets do not affect the trace buffer contents. The POR state is undefined.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSP register. To clear this flag, write logic level “1” to the corresponding bit in the PIFP register. Writing a “0” has no effect.

Table 23-44. PIFP Field Descriptions

Field	Description
7–0 PIFP[7:0]	**Interrupt Flags Port P** 0 No active edge pending. Writing a “0” has no effect. 1 Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set). Writing a logic level “1” clears the associated flag.

23.0.5.46 Port H Data Register (PTH)

	7	6	5	4	3	2	1	0
R W	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
SCI			TXD4	RXD4				
Routed SPI	$\overline{SS2}$	SCK2	MOSI2	MISO2	$\overline{SS1}$	SCK1	MOSI1	MISO1
Reset	0	0	0	0	0	0	0	0

Figure 23-48. Port H Data Register (PTH)

Read: Anytime.

Write: Anytime.

Port H pins 7–0 are associated with the SCI4 as well as the routed SPI1 and SPI2.

These pins can be used as general purpose I/O when not used with any of the peripherals.

If the data direction bits of the associated I/O pins are set to logic level “1”, a read returns the value of the port register, otherwise the buffered pin input state is read.

The routed SPI2 function takes precedence over the SCI4 and the general purpose I/O function if the routed SPI2 module is enabled. *Refer to SPI section for details.*The routed SPI1 function takes precedence over the general purpose I/O function if the routed SPI1 is enabled. *Refer to SPI section for details.*

The SCI4 function takes precedence over the general purpose I/O function if the SCI4 is enabled

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

Table 24-21. PERT Field Descriptions

Field	Description
7–0 PERT[7:0]	**Pull Device Enable Port T** 0 Pull-up or pull-down device is disabled. 1 Either a pull-up or pull-down device is enabled.

24.0.5.18 Port T Polarity Select Register (PPST)

	7	6	5	4	3	2	1	0
R W	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset	0	0	0	0	0	0	0	0

Figure 24-20. Port T Polarity Select Register (PPST)

Read: Anytime.

Write: Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

Table 24-22. PPST Field Descriptions

Field	Description
7–0 PPST[7:0]	**Pull Select Port T** 0 A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input. 1 A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

24.0.5.19 Port S Data Register (PTS)

	7	6	5	4	3	2	1	0
R W	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
SCI/SPI	$\overline{SS0}$	SCK0	MOSI0	MISO0	TXD1	RXD1	TXD0	RXD0
Reset	0	0	0	0	0	0	0	0

Figure 24-21. Port S Data Register (PTS)

Read: Anytime.

Write: Anytime.

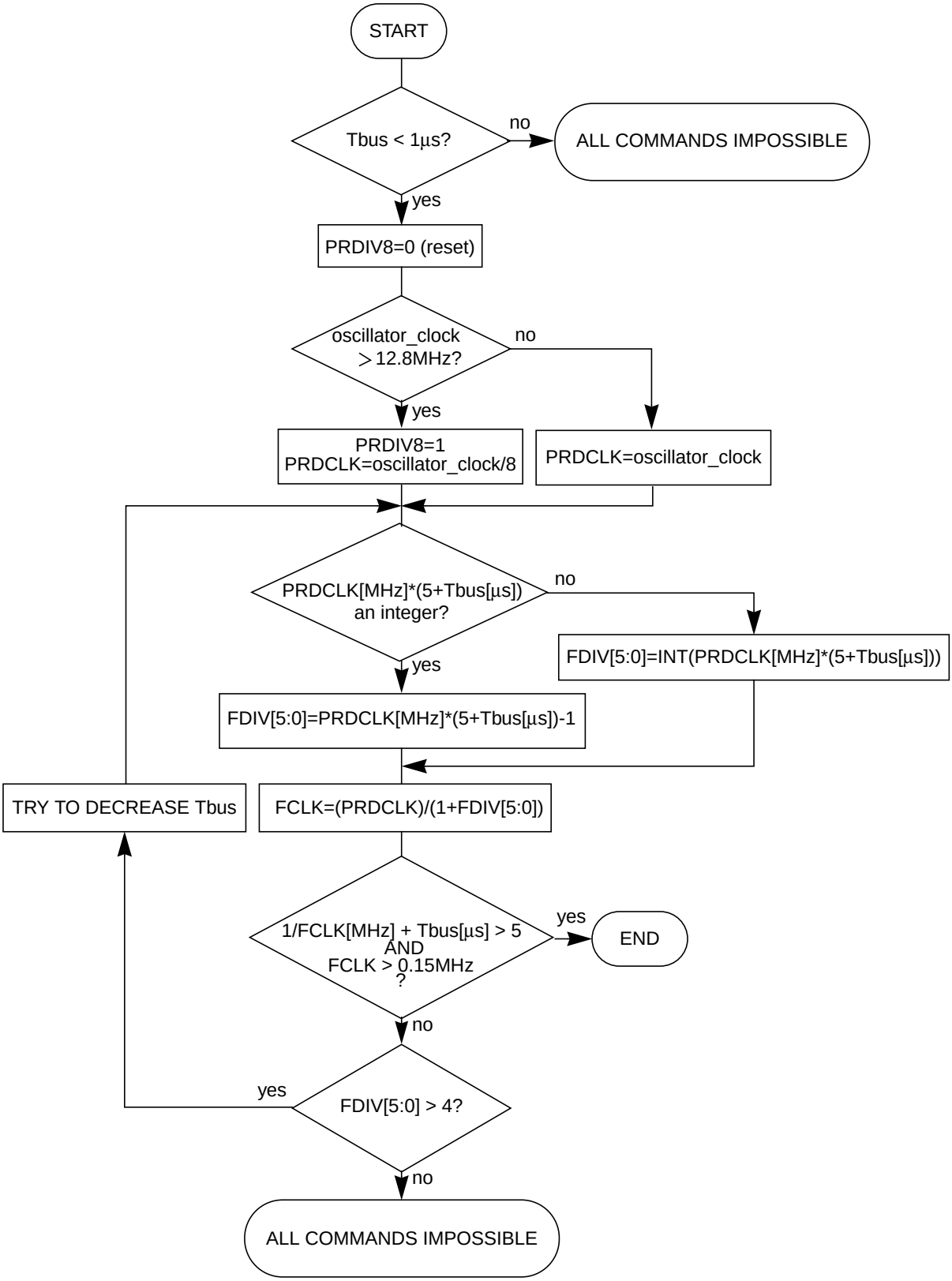

Figure 27-24. Determination Procedure for PRDIV8 and FDIV Bits

Table 29-9. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Flash Protection Open** — The FPOPEN bit determines the protection function for program or erase as shown in Table 29-10. 0 The FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS[1:0] and FPLS[1:0] bits. For an MCU without an EEPROM module, the FPOPEN clear state allows the main part of the Flash block to be protected while a small address range can remain unprotected for EEPROM emulation. 1 The FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS[1:0] and FPLS[1:0] bits.
6 RNV6	**Reserved Nonvolatile Bit** — The RNV[6] bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the Flash memory ending with global address 0x7F_FFFF. 0 Protection/Unprotection enabled. 1 Protection/Unprotection disabled.
4:3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS[1:0] bits determine the size of the protected/unprotected area as shown inTable 29-11. The FPHS[1:0] bits can only be written to while the FPHDIS bit is set.
2 FPLDIS	**Flash Protection Lower Address Range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the Flash memory beginning with global address 0x7F_8000. 0 Protection/Unprotection enabled. 1 Protection/Unprotection disabled.
1:0 FPLS[1:0]	**Flash Protection Lower Address Size** — The FPLS[1:0] bits determine the size of the protected/unprotected area as shown in Table 29-12. The FPLS[1:0] bits can only be written to while the FPLDIS bit is set.

Table 29-10. Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function[1]
1	1	1	No Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full Flash memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

1 For range sizes, refer to Table 29-11 and Table 29-12.

Table 29-11. Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x7F_F800–0x7F_FFFF	2 Kbytes
01	0x7F_F000–0x7F_FFFF	4 Kbytes
10	0x7F_E000–0x7F_FFFF	8 Kbytes
11	0x7F_C000–0x7F_FFFF	16 Kbytes

0x01C0–0x01FF Freescale Scalable CAN — MSCAN (CAN2) Map (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01D1	CAN2IDAR1	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x01D2	CAN2IDAR2	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x01D3	CAN2IDAR3	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x01D4	CAN2IDMR0	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01D5	CAN2IDMR1	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01D6	CAN2IDMR2	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01D7	CAN2IDMR3	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01D8	CAN2IDAR4	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x01D9	CAN2IDAR5	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x01DA	CAN2IDAR6	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x01DB	CAN2IDAR7	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x01DC	CAN2IDMR4	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01DD	CAN2IDMR5	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01DE	CAN2IDMR6	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01DF	CAN2IDMR7	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x01E0– 0x01EF	CAN2RXFG	R	FOREGROUND RECEIVE BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								
0x01F0– 0x01FF	CAN2TXFG	R W	FOREGROUND TRANSMIT BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							

0x0280–0x02BF Freescale Scalable CAN — MSCAN (CAN4) Map (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x028D	CAN4MISC	R	0	0	0	0	0	0	0	BOHOLD
		W								
0x028E	CAN4RXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		W								
0x028F	CAN4TXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		W								
0x0290	CAN4IDAR0	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0291	CAN4IDAR1	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0292	CAN4IDAR2	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0293	CAN4IDAR3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0294	CAN4IDMR0	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0295	CAN4IDMR1	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0296	CAN4IDMR2	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0297	CAN4IDMR3	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0298	CAN4IDAR4	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0299	CAN4IDAR5	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x029A	CAN4IDAR6	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x029B	CAN4IDAR7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x029C	CAN4IDMR4	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x029D	CAN4IDMR5	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x029E	CAN4IDMR6	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x029F	CAN4IDMR7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x02A0–0x02AF	CAN4RXFG	R	FOREGROUND RECEIVE BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								
0x02B0–0x02BF	CAN4TXFG	R	FOREGROUND TRANSMIT BUFFER (See Detailed MSCAN Foreground Receive and Transmit Buffer Layout)							
		W								