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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | HCS12X |
| Core Size | 16-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 119 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12xdt512vag |

The following conditions apply when the PLL is in automatic bandwidth control mode (AUTO = 1):

- The TRACK bit is a read-only indicator of the mode of the filter.
- The TRACK bit is set when the VCO frequency is within a certain tolerance, $\Delta_{trk}$, and is clear when the VCO frequency is out of a certain tolerance, $\Delta_{unt}$.
- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within a certain tolerance, $\Delta_{Lock}$, and is cleared when the VCO frequency is out of a certain tolerance, $\Delta_{unl}$.
- Interrupt requests can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.

The PLL can also operate in manual mode (AUTO = 0). Manual mode is used by systems that do not require an indicator of the lock condition for proper operation. Such systems typically operate well below the maximum system frequency ($f_{sys}$) and require fast start-up. The following conditions apply when in manual mode:

- ACQ is a writable control bit that controls the mode of the filter. Before turning on the PLL in manual mode, the ACQ bit should be asserted to configure the filter in acquisition mode.
- After turning on the PLL by setting the PLLON bit software must wait a given time ($t_{acq}$) before entering tracking mode (ACQ = 0).
- After entering tracking mode software must wait a given time ($t_{al}$) before selecting the PLLCLK as the source for system and core clocks (PLLSEL = 1).

### 2.4.1.2 System Clocks Generator

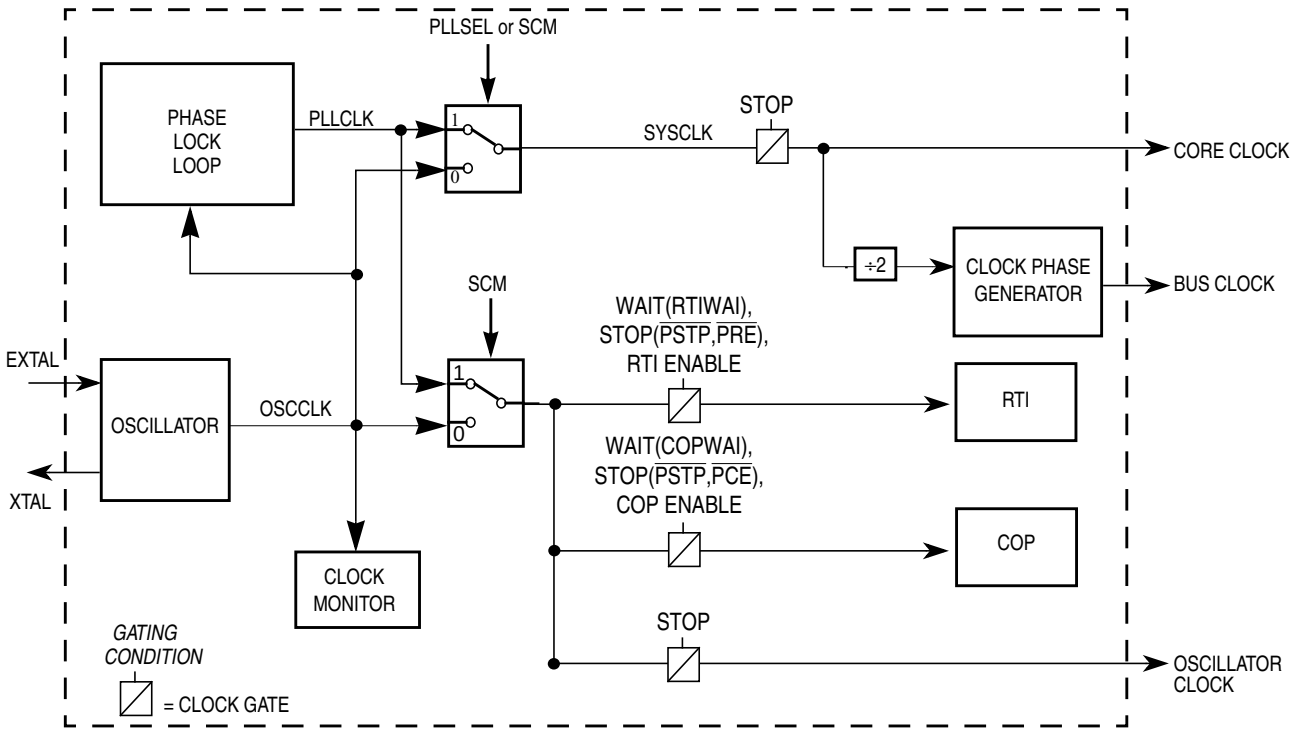



**Figure 2-17. System Clocks Generator**

### 6.8.2.2 Logic and Arithmetic Instructions

All logic and arithmetic instructions support the 8 bit immediate addressing mode (IMM8: RD = RD ∗ #IMM8) and the triadic addressing mode (TRI: RD = RS1 ∗ RS2).

All arithmetic is considered as signed, sign, overflow, zero and carry flag will be updated. The carry will not be affected for logical operations.

```
ADDL    R2,#1           ; increment R2
ANDH    R4,#$FE         ; R4.H = R4.H & $FE, clear lower bit of higher byte

ADD     R3,R4,R5        ; R3 = R4 + R5
SUB     R3,R4,R5        ; R3 = R4 - R5

AND     R3,R4,R5        ; R3 = R4 & R5 logical AND on the whole word
OR      R3,R4,R5        ; R3 = R4 | R5
```

### 6.8.2.3 Register – Register Transfers

This group comprises transfers from and to some special registers

```
        TFR     R3,CCR          ; transfers the condition code register to the low byte of
                                ; register R3
Branch Instructions
```

The branch offset is +255 words or -256 words counted from the beginning of the next instruction. Since instructions have a fixed 16 bit width, the branch offsets are word aligned by shifting the offset value by 2.

```
        BEQ     label           ; if Z flag = 1 branch to label
```

An unconditional branch allows a +511 words or -512 words branch distance.

```
        BRA     label
```

### 6.8.2.4 Shift Instructions

Shift operations allow the use of a 4 bit wide immediate value to identify a shift width within a 16 bit word. For shift operations a value of 0 does not shift at all, while a value of 15 shifts the register RD by 15 bits. In a second form the shift value is contained in the bits 3:0 of the register RS.

Examples:

```
        LSL     R4,#1   ; R4 = R4 << 1; shift register R4 by 1 bit to the left
        LSR     R4,#3   ; R4 = R4 >> 3; shift register R4 by 3 bits to the right
        ASR     R4,R2   ; R4 = R4 >> R2;arithmetic shift register R4 right by the amount
                        ;             of bits contained in R2[3:0].
```

# BLE Branch if Less or Equal to Zero BLE

## Operation

If Z | (N ^ V) = 1, then PC + $0002 + (REL9 << 1) ⇒ PC

Branch instruction to compare signed numbers.

Branch if RS1 ≤ RS2:

```
SUB     R0,RS1,RS2
BLE     REL9
```

## CCR Effects

| N | Z | V | C |
|---|---|---|---|
| — | — | — | — |

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

## Code and CPU Cycles

| Source Form | Address Mode | Machine Code | | | | | | | | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|
| BLE REL9 | REL9 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | REL9 | PP/P |

# COM One's Complement COM

## Operation

~RS ⇒ RD (translates to XNOR RD, R0, RS)
~RD ⇒ RD (translates to XNOR RD, R0, RD)

Performs a one's complement on a general purpose register.

## CCR Effects

| N | Z | V | C |
|---|---|---|---|
| Δ | Δ | 0 | — |

N: Set if bit 15 of the result is set; cleared otherwise.
Z: Set if the result is $0000; cleared otherwise.
V: 0; cleared.
C: Not affected.

## Code and CPU Cycles

| Source Form | Address Mode | Machine Code | | | | | | | | | | | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COM RD, RS | TRI | 0 | 0 | 0 | 1 | 0 | RD | 0 | 0 | 0 | RS | 1 | 1 | P |
| COM RD | TRI | 0 | 0 | 0 | 1 | 0 | RD | 0 | 0 | 0 | RD | 1 | 1 | P |

When PACN1 overflows from 0x00FF to 0x0000, the interrupt flag PBOVF in PBFLG is set.

Full count register access will take place in one clock cycle.

**NOTE**

A separate read/write for high byte and low byte will give a different result than accessing them as a word.

When clocking pulse and write to the registers occurs simultaneously, write takes priority and the register is not incremented.

- Four identifier acceptance filters, each to be applied to
  - a) the 14 most significant bits of the extended identifier plus the SRR and IDE bits of CAN 2.0B messages or
  - b) the 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B messages. Figure 10-41 shows how the first 32-bit filter bank (CANIDAR0–CANIDA3, CANIDMR0–3CANIDMR) produces filter 0 and 1 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 2 and 3 hits.
- Eight identifier acceptance filters, each to be applied to the first 8 bits of the identifier. This mode implements eight independent filters for the first 8 bits of a CAN 2.0A/B compliant standard identifier or a CAN 2.0B compliant extended identifier. Figure 10-42 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 to 3 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 4 to 7 hits.
- Closed filter. No CAN message is copied into the foreground buffer RxFG, and the RXF flag is never set.

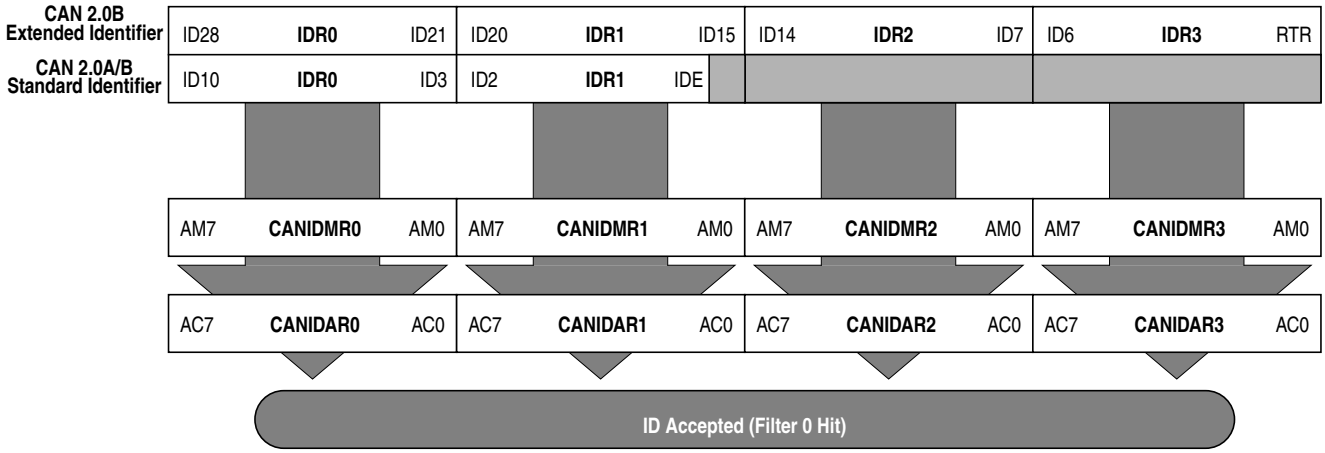



**Figure 10-40. 32-bit Maskable Identifier Acceptance Filter**

Address: 0x012C

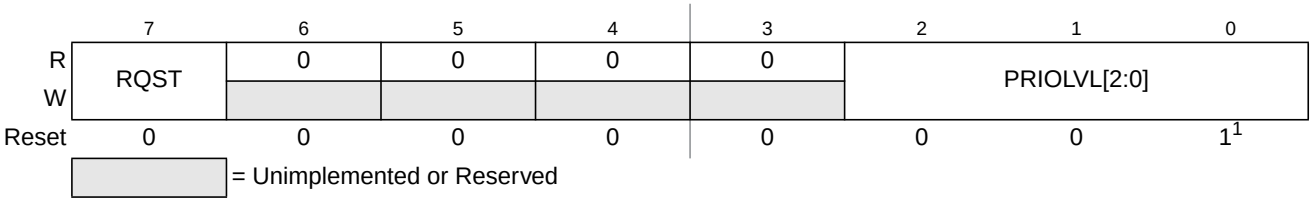



**Figure 16-10. Interrupt Request Configuration Data Register 4 (INT_CFDATA4)**

[1] Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x012D

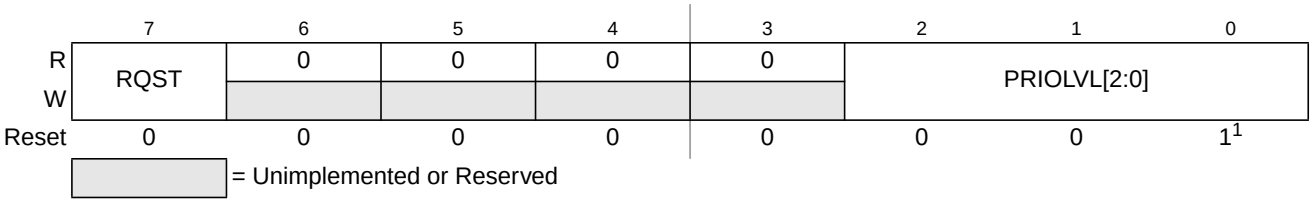



**Figure 16-11. Interrupt Request Configuration Data Register 5 (INT_CFDATA5)**

[1] Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x012E

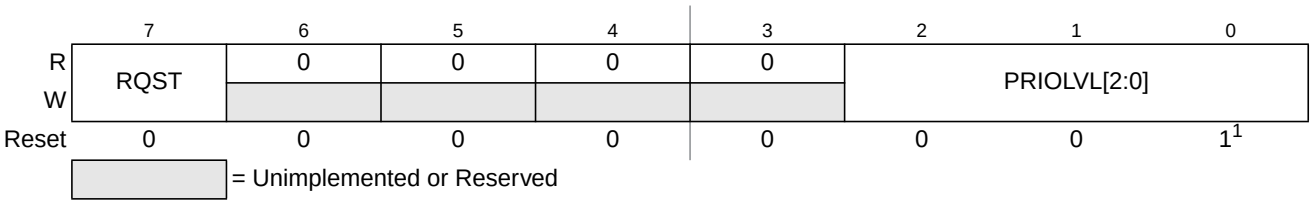



**Figure 16-12. Interrupt Request Configuration Data Register 6 (INT_CFDATA6)**

[1] Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x012F

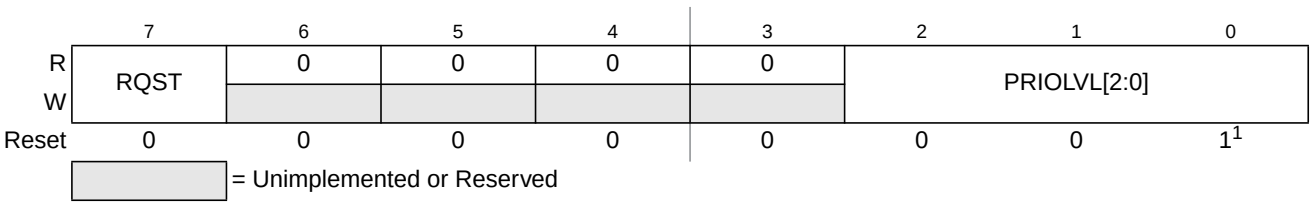



**Figure 16-13. Interrupt Request Configuration Data Register 7 (INT_CFDATA7)**

[1] Please refer to the notes following the PRIOLVL[2:0] description below.

Read: Anytime

Write: Anytime

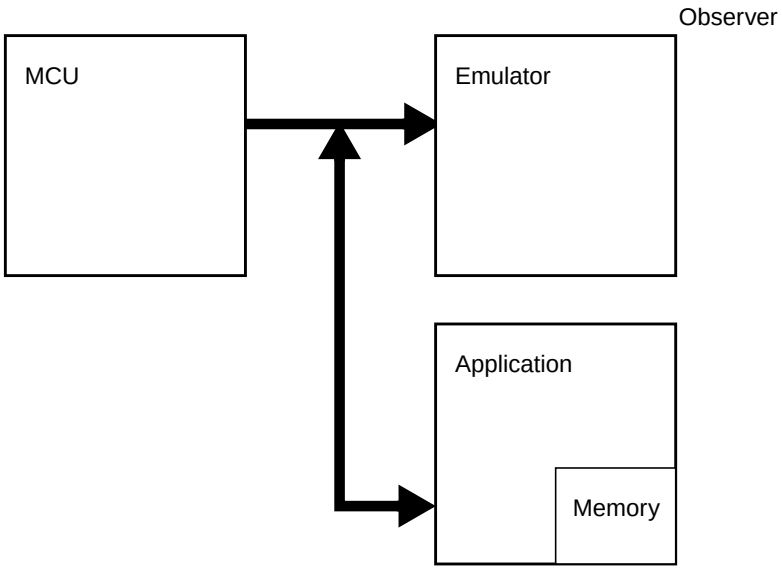



**Figure 17-31. ROMON = 0 in Emulation Expanded Mode**

### 17.5.3.5 ROM Control in Special Test Mode

In special test mode the external bus is connected to the application. If the ROMON bit is set, the internal FLASH provides the data, otherwise the application memory provides the data (see Figure 1-32).

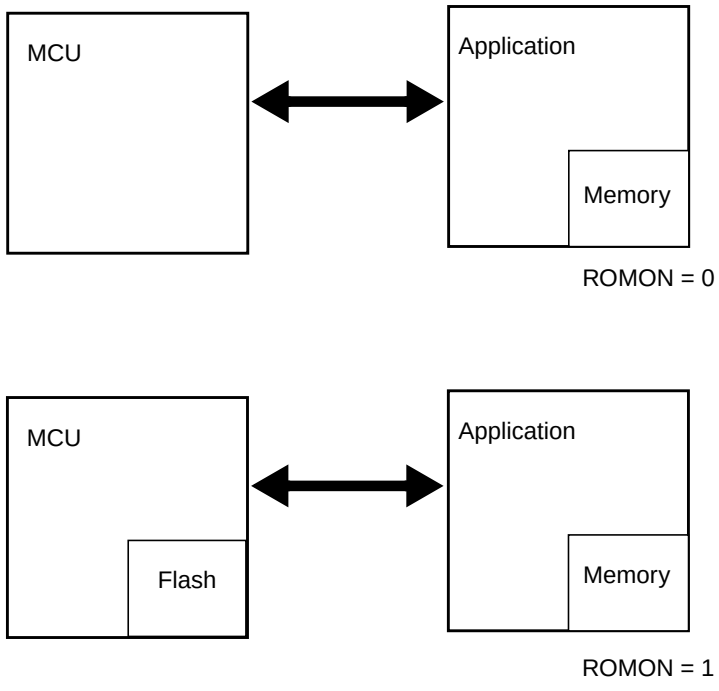



**Figure 17-32. ROM in Special Test Mode**

Table 18-21 shows the address boundaries of each chip select and the relationship with the implemented resources (internal) parameters.

**Table 18-21. Global Chip Selects Memory Space**

| Chip Selects | Bottom Address | Top Address |
|---|---|---|
| $\overline{CS3}$ | 0x00_0800 | 0x0F_FFFF minus RAMSIZE[1] |
| $\overline{CS2}$ | 0x10_0000 | 0x13_FFFF minus EEPROMSIZE[2] |
| $\overline{CS2}$[3] | 0x14_0000 | 0x1F_FFFF |
| $\overline{CS1}$ | 0x20_0000 | 0x3F_FFFF |
| $\overline{CS0}$[4] | 0x40_0000 | 0x7F_FFFF minus FLASHSIZE[5] |

1 External RPAGE accesses in (NX, EX and ST)

2 External EPAGE accesses in (NX, EX and ST)

3 When ROMHM is set (see ROMHM in Table 18-19) the $\overline{CS2}$ is asserted in the space occupied by this on-chip memory block.

4 When the internal NVM is enabled (see ROMON in Section 18.3.2.5, “MMC Control Register (MMCCTL1)) the $\overline{CS0}$ is not asserted in the space occupied by this on-chip memory block.

5 External PPAGE accesses in (NX, EX and ST)

**Figure 18-23. Local to Implemented Global Address Mapping (Without GPAGE)**

## 18.4.2.4 XGATE Memory Map Scheme

### 18.4.2.4.1 Expansion of the XGATE Local Address Map

The XGATE 64 Kbyte memory space allows access to internal resources only (Registers, RAM, and FLASH). The 2 Kilobyte register address range is the same register address range as for the CPU and the BDM module . XGATE can access the FLASH in single chip modes, even when the MCU is secured. In expanded modes, XGATE can not access the FLASH when MCU is secured.

The local address of the XGATE RAM access is translated to the global RAM address range. The XGATE shares the RAM resource with the CPU and the BDM module . The local address of the XGATE FLASH access is translated to the global address as shown in Figure 18-24. For the implemented memory spaces and addresses please refer to Table 1-4 and Table 1-5.

### 21.5.2 Emulation Modes

In emulation mode applications, the development systems use a custom PRU device to rebuild the single-chip or expanded bus functions which are lost due to the use of the external bus with an emulator.

Accesses to a set of registers controlling the related ports in normal modes (refer to SoC section) are directed to the external bus in emulation modes which are substituted by PRR as part of the PRU. Accesses to these registers take a constant time of 2 cycles.

Depending on the setting of ROMON and EROMON (refer to S12X_MMC section), the program code can be executed from internal memory or an optional external emulation memory (EMULMEM). No wait state operation (stretching) of the external bus access is done in emulation modes when accessing internal memory or emulation memory addresses.

In both modes observation of the internal operation is supported through the external bus (internal visibility).

### 22.3.2.26 Port S Reduced Drive Register (RDRS)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | RDRS7 | RDRS6 | RDRS5 | RDRS4 | RDRS3 | RDRS2 | RDRS1 | RDRS0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 22-28. Port S Reduced Drive Register (RDRS)**

Read: Anytime.

Write: Anytime.

This register configures the drive strength of each port S output pin as either full or reduced. If the port is used as input this bit is ignored.

**Table 22-28. RDRS Field Descriptions**

| Field | Description |
|---|---|
| 7–0<br>RDRS[7:0] | **Reduced Drive Port S**<br>0 Full drive strength at output.<br>1 Associated pin drives at about 1/6 of the full drive strength. |

### 22.3.2.27 Port S Pull Device Enable Register (PERS)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PERS7 | PERS6 | PERS5 | PERS4 | PERS3 | PERS2 | PERS1 | PERS0 |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Figure 22-29. Port S Pull Device Enable Register (PERS)**

Read: Anytime.

Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-OR (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

**Table 22-29. PERS Field Descriptions**

| Field | Description |
|---|---|
| 7–0<br>PERS[7:0] | **Pull Device Enable Port S**<br>0 Pull-up or pull-down device is disabled.<br>1 Either a pull-up or pull-down device is enabled. |

### 22.3.2.61 Port J Interrupt Flag Register (PIFJ)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | PIFJ7 | PIFJ6 | PIFJ5 | PIFJ4 | 0 | PIFJ2 | PIFJ1 | PIFJ0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 22-63. Port J Interrupt Flag Register (PIFJ)**

Read: Anytime.

Write: Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSJ register. To clear this flag, write logic level “1” to the corresponding bit in the PIFJ register. Writing a “0” has no effect.

**Table 22-57. PIEJ Field Descriptions**

| Field | Description |
|---|---|
| 7–0<br>PIFJ[7:4]<br>PIFJ[2:0] | **Interrupt Flags Port J**<br>0 No active edge pending. Writing a “0” has no effect.<br>1 Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set). Writing a logic level “1” clears the associated flag. |

### 22.3.2.62 Port AD0 Data Register 1 (PT1AD0)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | PT1AD07 | PT1AD06 | PT1AD05 | PT1AD04 | PT1AD03 | PT1AD02 | PT1AD01 | PT1AD00 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 22-64. Port AD0 Data Register 1 (PT1AD0)**

Read: Anytime.

Write: Anytime.

This register is associated with AD0 pins PAD[7:0]. These pins can also be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

# Chapter 23
# DQ256 Port Integration Module (S12XDQ256PIMV2)

**Introduction**

The S12XD family port integration module (below referred to as PIM) establishes the interface between the peripheral modules including the non-multiplexed external bus interface module (S12X_EBI) and the I/O pins for all ports. It controls the electrical pin properties as well as the signal prioritization and multiplexing on shared pins.

This document covers the description of:

- Port A, B used as address output of the S12X_EBI and Port C, D used as data I/O of the S12X_EBI
- Port E associated with the S12X_EBI control signals and the IRQ, XIRQ interrupt inputs
- Port K associated with address output and control signals of the S12X_EBI
- Port T connected to the Enhanced Capture Timer (ECT) module
- Port S associated with 2 SCI and 1 SPI modules
- Port M associated with 3 MSCAN modules
- Port P connected to the PWM and 2 SPI modules — inputs can be used as an external interrupt source
- Port H associated with 1 SCI module — inputs can be used as an external interrupt source
- Port J associated with 1 MSCAN, 1 SCI, and 1 IIC module — inputs can be used as an external interrupt source
- Port AD0 and AD1 associated with one 8-channel andone 16-channel ATD module

Most I/O pins can be configured by register bits to select data direction and drive strength, to enable and select pull-up or pull-down devices. Interrupts can be enabled on specific pins resulting in status flags.

The I/O’s of 2 MSCAN and 3 SPI modules can be routed from their default location to alternative port pins.

**NOTE**

The implementation of the PIM is device dependent. Therefore some functions are not available on certain derivatives or 112-pin and 80-pin package options.

## 23.0.1 Features

A full-featured PIM module includes these distinctive registers:

- Data and data direction registers for Ports A, B, C, D, E, K, T, S, M, P, H, J, AD0, and AD1 when used as general-purpose I/O

**Table 23-59. RDR1AD0 Field Descriptions**

| Field | Description |
|---|---|
| 7–0<br>RDR1AD0[7:0] | **Reduced Drive Port AD0 Register 1**<br>0 Full drive strength at output.<br>1 Associated pin drives at about 1/6 of the full drive strength. |

## 23.0.5.65 Port AD0 Pull Up Enable Register 1 (PER1AD0)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PER1AD07 | PER1AD06 | PER1AD05 | PER1AD04 | PER1AD03 | PER1AD02 | PER1AD01 | PER1AD00 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 23-67. Port AD0 Pull Up Enable Register 1 (PER1AD0)**

Read: Anytime.

Write: Anytime.

This register activates a pull-up device on the respective pin PAD[07:00] if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

**Table 23-60. PER1AD0 Field Descriptions**

| Field | Description |
|---|---|
| 7–0<br>PER1AD0[7:0] | **Pull Device Enable Port AD0 Register 1**<br>0 Pull-up device is disabled.<br>1 Pull-up device is enabled. |

## 23.0.5.66 Port AD1 Data Register 0 (PT0AD1)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PT0AD123 | PT0AD122 | PT0AD121 | PT0AD120 | PT0AD119 | PT0AD118 | PT0AD117 | PT0AD116 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 23-68. Port AD1 Data Register 0 (PT0AD1)**

Read: Anytime.

Write: Anytime.

This register is associated with AD1 pins PAD[23:16]. These pins can also be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

#### 26.4.2.1 Erase Verify Command

The erase verify operation will verify that the EEPROM memory is erased.

An example flow to execute the erase verify operation is shown in Figure 26-18. The erase verify command write sequence is as follows:

1. Write to an EEPROM address to start the command write sequence for the erase verify command. The address and data written will be ignored.
2. Write the erase verify command, 0x05, to the ECMD register.
3. Clear the CBEIF flag in the ESTAT register by writing a 1 to CBEIF to launch the erase verify command.

After launching the erase verify command, the CCIF flag in the ESTAT register will set after the operation has completed unless a new command write sequence has been buffered. The number of bus cycles required to execute the erase verify operation is equal to the number of words in the EEPROM memory plus 14 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. Upon completion of the erase verify operation, the BLANK flag in the ESTAT register will be set if all addresses in the EEPROM memory are verified to be erased. If any address in the EEPROM memory is not erased, the erase verify operation will terminate and the BLANK flag in the ESTAT register will remain clear.

### 29.4.2.2 Data Compress Command

The data compress operation will check Flash code integrity by compressing data from a selected portion of the Flash memory into a signature analyzer.

An example flow to execute the data compress operation is shown in Figure 29-24. The data compress command write sequence is as follows:

1. Write to a Flash block address to start the command write sequence for the data compress command. The address written determines the starting address for the data compress operation and the data written determines the number of consecutive words to compress. If the data value written is 0x0000, 64K addresses or 128 Kbytes will be compressed.
2. Write the data compress command, 0x06, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the data compress command.

After launching the data compress command, the CCIF flag in the FSTAT register will set after the data compress operation has completed. The number of bus cycles required to execute the data compress operation is equal to two times the number of consecutive words to compress plus 18 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. Once the CCIF flag is set, the signature generated by the data compress operation is available in the FDATA registers. The signature in the FDATA registers can be compared to the expected signature to determine the integrity of the selected data stored in the selected Flash memory. If the last address of a Flash block is reached during the data compress operation, data compression will continue with the starting address of the Flash block. The MRDS bits in the FTSTMOD register will determine the sense-amp margin setting during the data compress operation.

**NOTE**

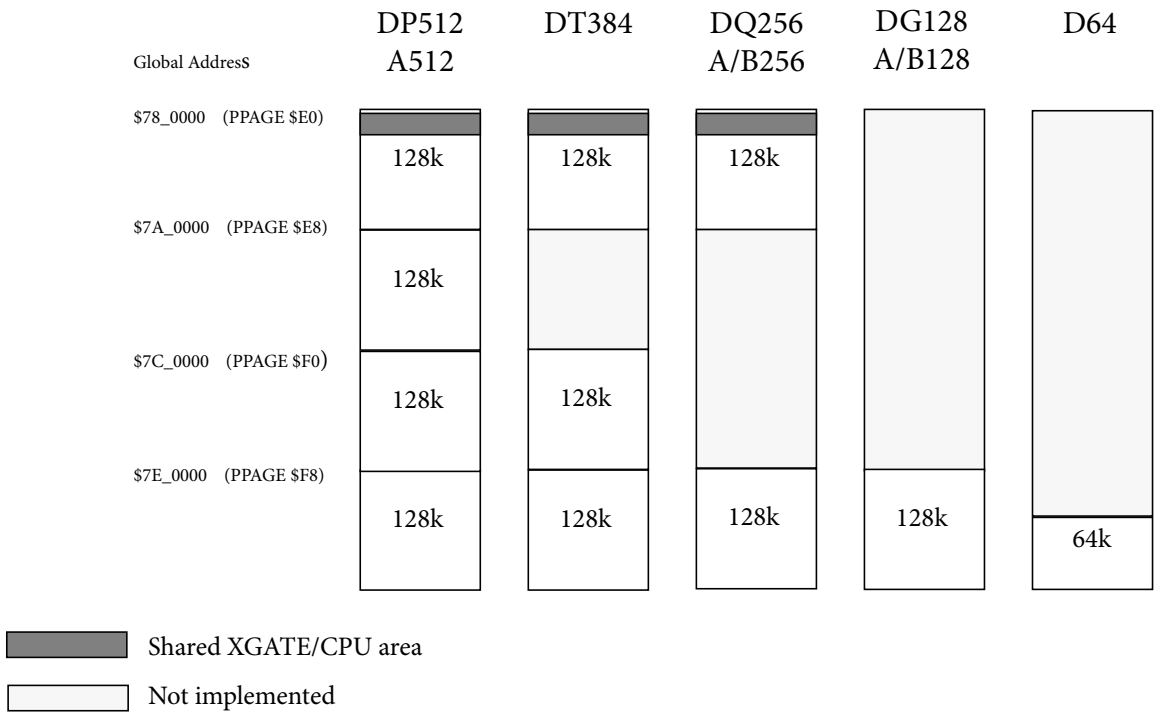
Since the FDATA registers (or data buffer) are written to as part of the data compress operation, a command write sequence is not allowed to be buffered behind a data compress command write sequence. The CBEIF flag will not set after launching the data compress command to indicate that a command should not be buffered behind it. If an attempt is made to start a new command write sequence with a data compress operation active, the ACCERR flag in the FSTAT register will be set. A new command write sequence should only be started after reading the signature stored in the FDATA registers.

In order to take corrective action, it is recommended that the data compress command be executed on a Flash sector or subset of a Flash sector. If the data compress operation on a Flash sector returns an invalid signature, the Flash sector should be erased using the sector erase command and then reprogrammed using the program command.

The data compress command can be used to verify that a sector or sequential set of sectors are erased.

## E.3 MC9S12XD-Family Flash Configuration[1 2 3 4 5]

**Figure E-1. MC9S12XD Family Flash Configuration**




1. XGATE read access to Flash not possible on DG128/D128/A128/B128 and D64
2. Program Pages available on DT384 are $E0 - $E7 and $F0 - $FF
3. Program Pages available on B256/A256/DQ256/DT256/D256 are $E0 - $E7 and $F8 - $FF
4. Shared XGATE/CPU area on A512/DP512/DT512/DT384 at global address $78_0800 to $78_7FFF (30Kbyte)
5. Shared XGATE/CPU area on A256/B256/DT256/DQ256/D256 at global address $78_0800 to $78_7FFF (30Kbyte)