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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912xdt256f1mal

Revision History

Date	Revision Level	Description
April, 2005	02.07	New Book
May, 2005	02.08	Minor corrections
May, 2005	02.09	removed ESD Machine Model from electrical characteristics added thermal characteristics added more details to run current measurement configurations VDDA supply voltage range 3.15V - 3.6V fot ATD Operating Characteristics I/O Chararcteristics for alll pins except EXTAL, XTAL .... corrected VREG electrical spec IDD wait max 95mA
May 2005	02.10	Improvements to NVM reliabity spec, added part numbers
July 2005	02.11	Added ROM parts to App.
October 2005	02.12	Single Souce S12XD Fam. Document, New Memory Map Figures,
May 2006	2.13	SPI electricals updated Voltage Regulator electricals updated Added Partnumbers and 1L15Y maskset Updated App. E 6SCI's on 112 pin DT/P512 and 3 SPI's on all D256 parts
June 2006	2.14	Data Sheet covers S12XD/B & A Family Included differnt pull device specification for differnt masksets
July 2006	2.15	Minor Corrections and Improvments
June 2007	2.16	Added 2M42E and 1M84E masksets
July 2007	2.17	Modified Appendix
April 2008	2.18	Better explanation of ATD0/1 for S12XD-Family see page 1305 S12XB256 ATD specification changed see Appendix E.6 added M23S maskset
August 2008	2.19	Corrected XGRAMSIZE of S12XD256 on page 44 Corrected 17.4.2.4 XGATE Memory Map Scheme Corrected 18.4.2.4 XGATE Memory Map Scheme
September 2009	2.20	Corrected Table E-6 , 30K flash memory available for XGATE on B256
October 2009	2.21	Corrected Footnote in Appendix E3 regarding Shared XGATE/CPU area

Chapter 28
256 Kbyte Flash Module (S12XFTX256K2V1)

Chapter 29
128 Kbyte Flash Module (S12XFTX128K1V1)

Table 5-12. Clock Prescaler Values

Prescale Value	Total Divisor Value	Max. Bus Clock[1]	Min. Bus Clock[2]
00000	Divide by 2	4 MHz	1 MHz
00001	Divide by 4	8 MHz	2 MHz
00010	Divide by 6	12 MHz	3 MHz
00011	Divide by 8	16 MHz	4 MHz
00100	Divide by 10	20 MHz	5 MHz
00101	Divide by 12	24 MHz	6 MHz
00110	Divide by 14	28 MHz	7 MHz
00111	Divide by 16	32 MHz	8 MHz
01000	Divide by 18	36 MHz	9 MHz
01001	Divide by 20	40 MHz	10 MHz
01010	Divide by 22	44 MHz	11 MHz
01011	Divide by 24	48 MHz	12 MHz
01100	Divide by 26	52 MHz	13 MHz
01101	Divide by 28	56 MHz	14 MHz
01110	Divide by 30	60 MHz	15 MHz
01111	Divide by 32	64 MHz	16 MHz
10000	Divide by 34	68 MHz	17 MHz
10001	Divide by 36	72 MHz	18 MHz
10010	Divide by 38	76 MHz	19 MHz
10011	Divide by 40	80 MHz	20 MHz
10100	Divide by 42	84 MHz	21 MHz
10101	Divide by 44	88 MHz	22 MHz
10110	Divide by 46	92 MHz	23 MHz
10111	Divide by 48	96 MHz	24 MHz
11000	Divide by 50	100 MHz	25 MHz
11001	Divide by 52	104 MHz	26 MHz
11010	Divide by 54	108 MHz	27 MHz
11011	Divide by 56	112 MHz	28 MHz
11100	Divide by 58	116 MHz	29 MHz
11101	Divide by 60	120 MHz	30 MHz
11110	Divide by 62	124 MHz	31 MHz
11111	Divide by 64	128 MHz	32 MHz

1 Maximum ATD conversion clock frequency is 2 MHz. The maximum allowed bus clock frequency is shown in this column.

2 Minimum ATD conversion clock frequency is 500 kHz. The minimum allowed bus clock frequency is shown in this column.

LDW — Load Word from Memory — LDW

Operation

M[RB, #OFFS5] ⇒ RD
M[RB, RI] ⇒ RD
M[RB, RI] ⇒ RD; RI+2 ⇒ RI[1]
RI-2 ⇒ RI; M[RS, RI] ⇒ RD
IMM16 ⇒ RD (translates to LDL RD, #IMM16[7:0]; LDH RD, #IMM16[15:8])

Loads a 16 bit value into the register RD.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code										Cycles
LDW RD, (RB, #OFFS5)	IDO5	0	1	0	0	1	RD	RB	OFFS5			PR
LDW RD, (RB, RI)	IDR	0	1	1	0	1	RD	RB	RI	0	0	PR
LDW RD, (RB, RI+)	IDR+	0	1	1	0	1	RD	RB	RI	0	1	PR
LDW RD, (RB, -RI)	-IDR	0	1	1	0	1	RD	RB	RI	1	0	PR
LDW RD, #IMM16	IMM8	1	1	1	1	0	RD	IMM16[7:0]				P
	IMM8	1	1	1	1	1	RD	IMM16[15:8]				P

1. If the same general purpose register is used as index (RI) and destination register (RD), the content of the register will not be incremented after the data move: M[RB, RI] ⇒ RD

STB

Store Byte to Memory (Low Byte)

STB

Operation

RS.L ⇒ M[RB, #OFFS5]
RS.L ⇒ M[RB, RI]
RS.L ⇒ M[RB, RI]; RI+1 ⇒ RI;
RI–1 ⇒ RI; RS.L ⇒ M[RB, RI][1]

Stores the low byte of register RD to memory.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code										Cycles
STB RS, (RB, #OFFS5),	IDO5	0	1	0	1	0	RS	RB	OFFS5			Pw
STB RS, (RB, RI)	IDR	0	1	1	1	0	RS	RB	RI	0	0	Pw
STB RS, (RB, RI+)	IDR+	0	1	1	1	0	RS	RB	RI	0	1	Pw
STB RS, (RB, -RI)	-IDR	0	1	1	1	0	RS	RB	RI	1	0	Pw

1. If the same general purpose register is used as index (RI) and source register (RS), the unmodified content of the source register is written to the memory: RS.L ⇒ M[RB, RS-1]; RS-1 ⇒ RS

7.3.2.23 Input Control Overwrite Register (ICOVW)

	7	6	5	4	3	2	1	0
R W	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
Reset	0	0	0	0	0	0	0	0

Figure 7-45. Input Control Overwrite Register (ICOVW)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 7-29. ICOVW Field Descriptions

Field	Description
7:0 NOVW[7:0]	**No Input Capture Overwrite** 0 The contents of the related capture register or holding register can be overwritten when a new input capture or latch occurs. 1 The related capture register or holding register cannot be written by an event unless they are empty (see Section 7.4.1.1, “IC Channels”). This will prevent the captured value being overwritten until it is read or latched in the holding register.

Table 7-32. Precision Timer Prescaler Selection Examples when PRNT = 1

PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0	Prescale Factor
0	0	0	0	0	1	1	1	8
0	0	0	0	1	1	1	1	16
0	0	0	1	1	1	1	1	32
0	0	1	1	1	1	1	1	64
0	1	1	1	1	1	1	1	128
1	1	1	1	1	1	1	1	256

7.3.2.26 Precision Timer Modulus Counter Prescaler Select Register (PTMCPSR)

	7	6	5	4	3	2	1	0
R W	PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0
Reset	0	0	0	0	0	0	0	0

Figure 7-48. Precision Timer Modulus Counter Prescaler Select Register (PTMCPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 7-33. PTMCPSR Field Descriptions

Field	Description
7:0 PTMPS[7:0]	**Precision Timer Modulus Counter Prescaler Select Bits** — These eight bits specify the division rate of the modulus counter prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. Table 7-34 shows some possible division rates. The newly selected prescaler division rate will not be effective until a load of the load register into the modulus counter count register occurs.

Table 7-34. Precision Timer Modulus Counter Prescaler Select Examples when PRNT = 1

PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0	Prescaler Division Rate
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	0	0	5
0	0	0	0	0	1	0	1	6
0	0	0	0	0	1	1	0	7

Read: Anytime

Write: Anytime

NOTE

Write these bits only when the corresponding channel is disabled.

Table 8-7. PWMCAE Field Descriptions

Field	Description
7–0 CAE[7:0]	**Center Aligned Output Modes on Channels 7–0** 0 Channels 7–0 operate in left aligned output mode. 1 Channels 7–0 operate in center aligned output mode.

8.3.2.6 PWM Control Register (PWMCTL)

The PWMCTL register provides for various control of the PWM module.

	7	6	5	4	3	2	1	0
R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-8. PWM Control Register (PWMCTL)

Read: Anytime

Write: Anytime

There are three control bits for concatenation, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. When channels 6 and 7are concatenated, channel 6 registers become the high order bytes of the double byte channel. When channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high order bytes of the double byte channel.

See Section 8.4.2.7, “PWM 16-Bit Functions” for a more detailed description of the concatenation PWM Function.

NOTE

Change these bits only when both corresponding channels are disabled.

Table 9-7. IBSR Field Descriptions (continued)

Field	Description
2 SRW	**Slave Read/Write** — When IAAS is set this bit indicates the value of the R/W command bit of the calling address sent from the master This bit is only valid when the I-bus is in slave mode, a complete address transfer has occurred with an address match and no other transfers have been initiated. Checking this bit, the CPU can select slave transmit/receive mode according to the command of the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IBIF	**I-Bus Interrupt** — The IBIF bit is set when one of the following conditions occurs: — Arbitration lost (IBAL bit set) — Byte transfer complete (TCF bit set) — Addressed as slave (IAAS bit set) It will cause a processor interrupt request if the IBIE bit is set. This bit must be cleared by software, writing a one to it. A write of 0 has no effect on this bit.
0 RXAK	**Received Acknowledge** — The value of SDA during the acknowledge bit of a bus cycle. If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 bits data transmission on the bus. If RXAK is high, it means no acknowledge signal is detected at the 9th clock. 0 Acknowledge received 1 No acknowledge received

9.3.2.5 IIC Data I/O Register (IBDR)

	7	6	5	4	3	2	1	0
R W	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	0	0	0	0	0	0

Figure 9-8. IIC Bus Data I/O Register (IBDR)

In master transmit mode, when data is written to the IBDR a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates next byte data receiving. In slave mode, the same functions are available after an address match has occurred.Note that the Tx/Rx bit in the IBCR must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For instance, if the IIC is configured for master transmit but a master receive is desired, then reading the IBDR will not initiate the receive.

Reading the IBDR will return the last byte received while the IIC is configured in either master receive or slave receive modes. The IBDR does not reflect every byte that is transmitted on the IIC bus, nor can software verify that a byte has been written to the IBDR correctly by reading it back.

In master transmit mode, the first byte of data written to IBDR following assertion of MS/$\overline{SL}$ is used for the address transfer and should com.prise of the calling address (in position D7:D1) concatenated with the required R/$\overline{W}$ bit (in position D0).

Table 10-5. Baud Rate Prescaler

BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	Prescaler value (P)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

10.3.2.4 MSCAN Bus Timing Register 1 (CANBTR1)

The CANBTR1 register configures various CAN bus timing parameters of the MSCAN module.

	7	6	5	4	3	2	1	0
R W	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
Reset:	0	0	0	0	0	0	0	0

Figure 10-7. MSCAN Bus Timing Register 1 (CANBTR1)

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 10-6. CANBTR1 Register Field Descriptions

Field	Description
7 SAMP	**Sampling** — This bit determines the number of CAN bus samples taken per bit time. 0 One sample per bit. 1 Three samples per bit[1]. If SAMP = 0, the resulting bit value is equal to the value of the single bit positioned at the sample point. If SAMP = 1, the resulting bit value is determined by using majority rule on the three total samples. For higher bit rates, it is recommended that only one sample is taken per bit time (SAMP = 0).
6:4 TSEG2[2:0]	**Time Segment 2** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 10-44). Time segment 2 (TSEG2) values are programmable as shown in Table 10-7.
3:0 TSEG1[3:0]	**Time Segment 1** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 10-44). Time segment 1 (TSEG1) values are programmable as shown in Table 10-8.

[1] In this case, PHASE_SEG1 must be at least 2 time quanta (Tq).

15.1.2.3 Low-Power Modes

The BDM can be used until all bus masters (e.g., CPU or XGATE) are in stop mode. When CPU is in a low power mode (wait or stop mode) all BDM firmware commands as well as the hardware BACKGROUND command can not be used respectively are ignored. In this case the CPU can not enter BDM active mode, and only hardware read and write commands are available. Also the CPU can not enter a low power mode during BDM active mode.

If all bus masters are in stop mode, the BDM clocks are stopped as well. When BDM clocks are disabled and one of the bus masters exits from stop mode the BDM clocks will restart and BDM will have a soft reset (clearing the instruction register, any command in progress and disable the ACK function). The BDM is now ready to receive a new command.

15.1.3 Block Diagram

A block diagram of the BDM is shown in Figure 15-1.

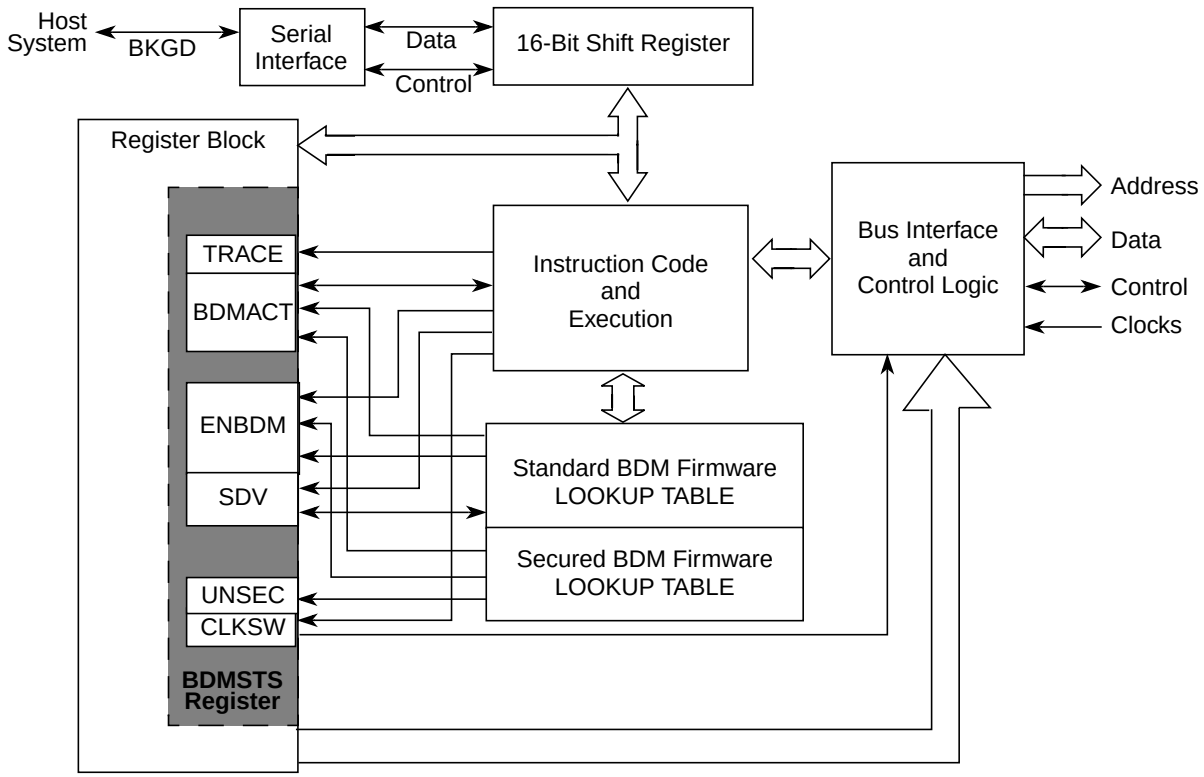


Figure 15-1. BDM Block Diagram

22.3.2.63 Port AD0 Data Direction Register 1 (DDR1AD0)

	7	6	5	4	3	2	1	0
R W	DDR1AD07	DDR1AD06	DDR1AD05	DDR1AD04	DDR1AD03	DDR1AD02	DDR1AD01	DDR1AD00
Reset	0	0	0	0	0	0	0	0

Figure 22-65. Port AD0 Data Direction Register 1 (DDR1AD0)

Read: Anytime.

Write: Anytime.

This register configures pins PAD[07:00] as either input or output.

Table 22-58. DDR1AD0 Field Descriptions

Field	Description
7–0 DDR1AD0[7:0]	**Data Direction Port AD0 Register 1** 0 Associated pin is configured as input. 1 Associated pin is configured as output. **Note:** Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTAD01 register, when changing the DDR1AD0 register. **Note:** To use the digital input function on port AD0 the ATD0 digital input enable register (ATD0DIEN) has to be set to logic level “1”.

22.3.2.70 Port AD1 Reduced Drive Register 0 (RDR0AD1)

	7	6	5	4	3	2	1	0
R W	RDR0AD123	RDR0AD122	RDR0AD121	RDR0AD120	RDR0AD119	RDR0AD118	RDR0AD117	RDR0AD116
Reset	0	0	0	0	0	0	0	0

Figure 22-72. Port AD1 Reduced Drive Register 0 (RDR0AD1)

Read: Anytime.

Write: Anytime.

This register configures the drive strength of each PAD[23:16] output pin as either full or reduced. If the port is used as input this bit is ignored.

Table 22-63. RDR0AD1 Field Descriptions

Field	Description
7–0 RDR0AD1[23:16]	**Reduced Drive Port AD1 Register 0** 0 Full drive strength at output. 1 Associated pin drives at about 1/6 of the full drive strength.

22.3.2.71 Port AD1 Reduced Drive Register 1 (RDR1AD1)

	7	6	5	4	3	2	1	0
R W	RDR1AD115	RDR1AD114	RDR1AD113	RDR1AD112	RDR1AD111	RDR1AD110	RDR1AD19	RDR1AD18
Reset	0	0	0	0	0	0	0	0

Figure 22-73. Port AD1 Reduced Drive Register 1 (RDR1AD1)

Read: Anytime.

Write: Anytime.

This register configures the drive strength of each PAD[15:08] output pin as either full or reduced. If the port is used as input this bit is ignored.

Table 22-64. RDR1AD1 Field Descriptions

Field	Description
7–0 RDR1AD1[15:8]	**Reduced Drive Port AD1 Register 1** 0 Full drive strength at output. 1 Associated pin drives at about 1/6 of the full drive strength.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 26-6. RESERVED2

All bits read 0 and are not writable.

26.3.2.4 EEPROM Configuration Register (ECNFG)

The ECNFG register enables the EEPROM interrupts.

	7	6	5	4	3	2	1	0
R	CBEIE	CCIE	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 26-7. EEPROM Configuration Register (ECNFG)

CBEIE and CCIE bits are readable and writable while all remaining bits read 0 and are not writable.

Table 26-4. ECNFG Field Descriptions

Field	Description
7 CBEIE	**Command Buffer Empty Interrupt Enable** — The CBEIE bit enables an interrupt in case of an empty command buffer in the EEPROM module. 0 Command Buffer Empty interrupt disabled. 1 An interrupt will be requested whenever the CBEIF flag (see Section 26.3.2.6, “EEPROM Status Register (ESTAT)”) is set.
6 CCIE	**Command Complete Interrupt Enable** — The CCIE bit enables an interrupt in case all commands have been completed in the EEPROM module. 0 Command Complete interrupt disabled. 1 An interrupt will be requested whenever the CCIF flag (see Section 26.3.2.6, “EEPROM Status Register (ESTAT)”) is set.

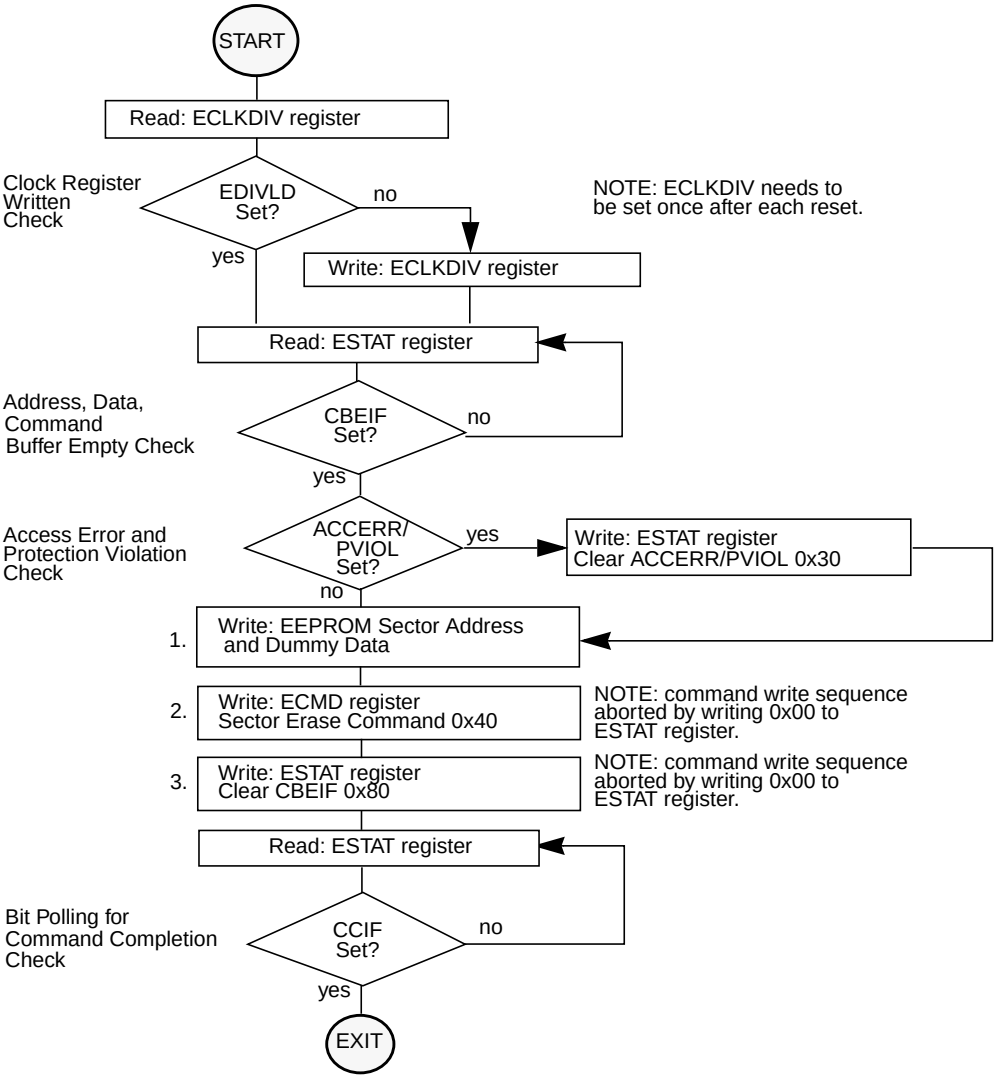


Figure 26-20. Example Sector Erase Command Flow

26.4.2.6 Sector Modify Command

The sector modify operation will erase both words in a sector of EEPROM memory followed by a reprogram of the addressed word using an embedded algorithm.

An example flow to execute the sector modify operation is shown in Figure 26-23. The sector modify command write sequence is as follows:

1. Write to an EEPROM memory address to start the command write sequence for the sector modify command. The EEPROM address written determines the sector to be erased and word to be reprogrammed while byte address bit 0 is ignored.
2. Write the sector modify command, 0x60, to the ECMD register.
3. Clear the CBEIF flag in the ESTAT register by writing a 1 to CBEIF to launch the sector erase command.

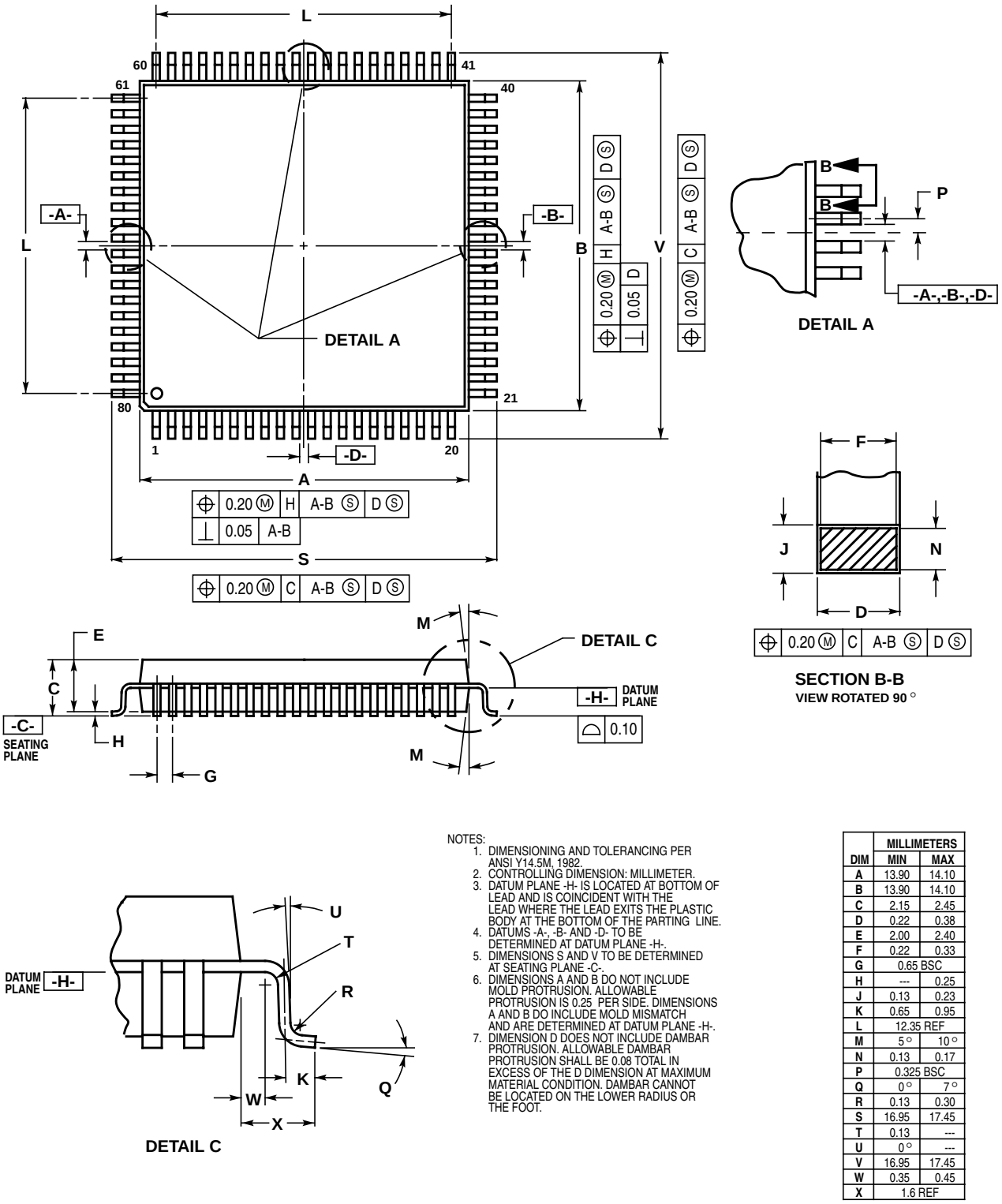
If an EEPROM sector to be modified is in a protected area of the EEPROM memory, the PVIOL flag in the ESTAT register will set and the sector modify command will not launch. Once the sector modify command has successfully launched, the CCIF flag in the ESTAT register will set after the sector modify operation has completed unless a new command write sequence has been buffered.

CBEIF, PVIOL, and ACCERR are readable and writable, CCIF and BLANK are readable and not writable, remaining bits read 0 and are not writable in normal mode. FAIL is readable and writable in special mode. FAIL must be clear in special mode when starting a command write sequence.

Table 29-14. FSTAT Field Descriptions

Field	Description
7 CBEIF	**Command Buffer Empty Interrupt Flag** — The CBEIF flag indicates that the address, data and command buffers are empty so that a new command write sequence can be started. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the Flash address space, but before CBEIF is cleared, will abort a command write sequence and cause the ACCERR flag to be set. Writing a 0 to CBEIF outside of a command write sequence will not set the ACCERR flag. The CBEIF flag is cleared by writing a 1 to CBEIF. The CBEIF flag is used together with the CBEIE bit in the FCNFG register to generate an interrupt request (see Figure 29-30). 0 Command buffers are full. 1 Command buffers are ready to accept a new command.
6 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is cleared and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect on CCIF. The CCIF flag is used together with the CCIE bit in the FCNFG register to generate an interrupt request (see Figure 29-30). 0 Command in progress. 1 All commands are completed.
5 PVIOL	**Protection Violation Flag** —The PVIOL flag indicates an attempt was made to program or erase an address in a protected area of the Flash memory during a command write sequence. Writing a 0 to the PVIOL flag has no effect on PVIOL. The PVIOL flag is cleared by writing a 1 to PVIOL. While PVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No protection violation detected. 1 Protection violation has occurred.
4 ACCERR	**Access Error Flag** — The ACCERR flag indicates an illegal access has occurred to the Flash memory caused by either a violation of the command write sequence (see Section 29.4.1.2, “Command Write Sequence”), issuing an illegal Flash command (see Table 29-16), launching the sector erase abort command terminating a sector erase operation early (see Section 29.4.2.6, “Sector Erase Abort Command”) or the execution of a CPU STOP instruction while a command is executing (CCIF = 0). Writing a 0 to the ACCERR flag has no effect on ACCERR. The ACCERR flag is cleared by writing a 1 to ACCERR.While ACCERR is set, it is not possible to launch a command or start a command write sequence. If ACCERR is set by an erase verify operation or a data compress operation, any buffered command will not launch. 0 No access error detected. 1 Access error has occurred.
2 BLANK	**Flag Indicating the Erase Verify Operation Status** — When the CCIF flag is set after completion of an erase verify command, the BLANK flag indicates the result of the erase verify operation. The BLANK flag is cleared by the Flash module when CBEIF is cleared as part of a new valid command write sequence. Writing to the BLANK flag has no effect on BLANK. 0 Flash block verified as not erased. 1 Flash block verified as erased.
1 FAIL	**Flag Indicating a Failed Flash Operation** — The FAIL flag will set if the erase verify operation fails (Flash block verified as not erased). Writing a 0 to the FAIL flag has no effect on FAIL. The FAIL flag is cleared by writing a 1 to FAIL. 0 Flash operation completed without error. 1 Flash operation failed.

B.3 80-Pin QFP Package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure B-3. 80-Pin QFP Mechanical Dimensions (Case No. 841B)

Figure C-2. 112-Pin LQFP Recommended PCB Layout