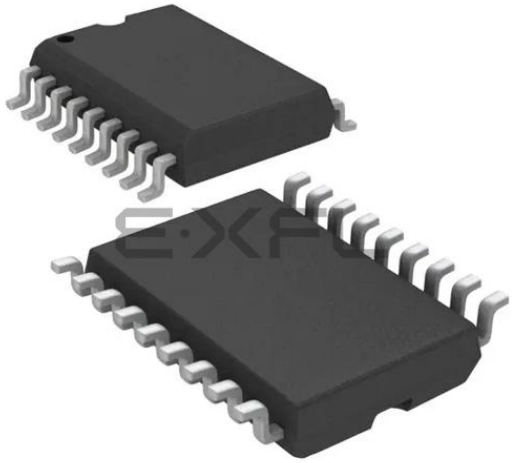

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f54-e-so

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PIC16F5X

Flash-Based, 8-Bit CMOS Microcontroller Series

High-Performance RISC CPU:

- Only 33 single-word instructions to learn
- All instructions are single cycle except for program branches which are two-cycle
- Two-level deep hardware stack
- Direct, Indirect and Relative Addressing modes for data and instructions
- Operating speed:
  - DC – 20 MHz clock speed
  - DC – 200 ns instruction cycle time
- On-chip Flash program memory:
  - 512 x 12 on PIC16F54
  - 2048 x 12 on PIC16F57
  - 2048 x 12 on PIC16F59
- General Purpose Registers (SRAM):
  - 25 x 8 on PIC16F54
  - 72 x 8 on PIC16F57
  - 134 x 8 on PIC16F59

Special Microcontroller Features:

- Power-on Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable Code Protection
- Power-Saving Sleep mode
- In-Circuit Serial Programming™ (ICSP™)
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power-saving, low-frequency crystal
- Packages:
  - 18-pin PDIP and SOIC for PIC16F54
  - 20-pin SSOP for PIC16F54
  - 28-pin PDIP, SOIC and SSOP for PIC16F57
  - 40-pin PDIP for PIC16F59
  - 44-pin TQFP for PIC16F59

Low-Power Features:

- Operating Current:
  - 170 μA @ 2V, 4 MHz, typical
  - 15 μA @ 2V, 32 kHz, typical
- Standby Current:
  - 500 nA @ 2V, typical

Peripheral Features:

- 12/20/32 I/O pins:
  - Individual direction control
  - High current source/sink
- 8-bit real-time clock/counter (TMR0) with 8-bit programmable prescaler

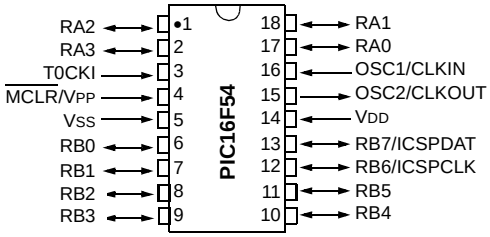
CMOS Technology:

- Wide operating voltage range:
  - Industrial: 2.0V to 5.5V
  - Extended: 2.0V to 5.5V
- Wide temperature range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C
- High-endurance Flash:
  - 100K write/erase cycles
  - > 40-year retention

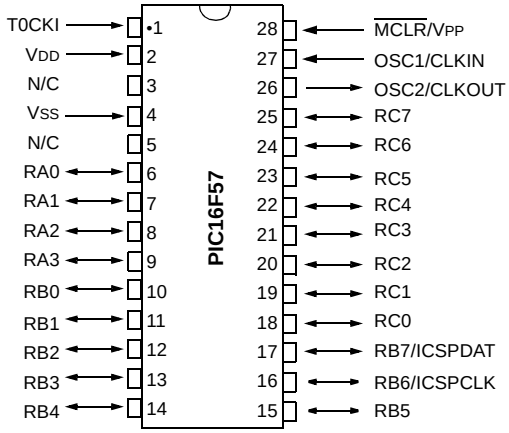
Device	Program Memory	Data Memory	I/O	Timers 8-bit
	Flash (words)	SRAM (bytes)		
PIC16F54	512	25	12	1
PIC16F57	2048	72	20	1
PIC16F59	2048	134	32	1

Pin Diagrams

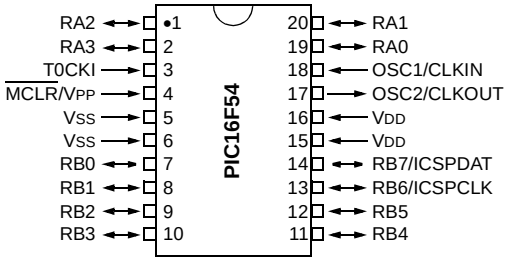
PDIP, SOIC



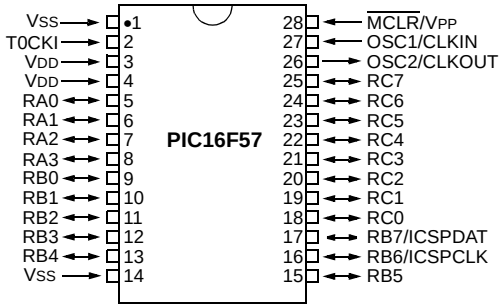
PDIP, SOIC



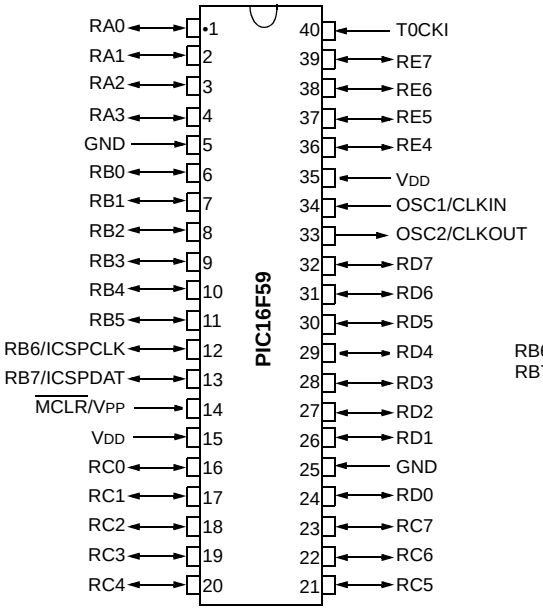
SSOP



SSOP



PDIP, 0.600"



TQFP

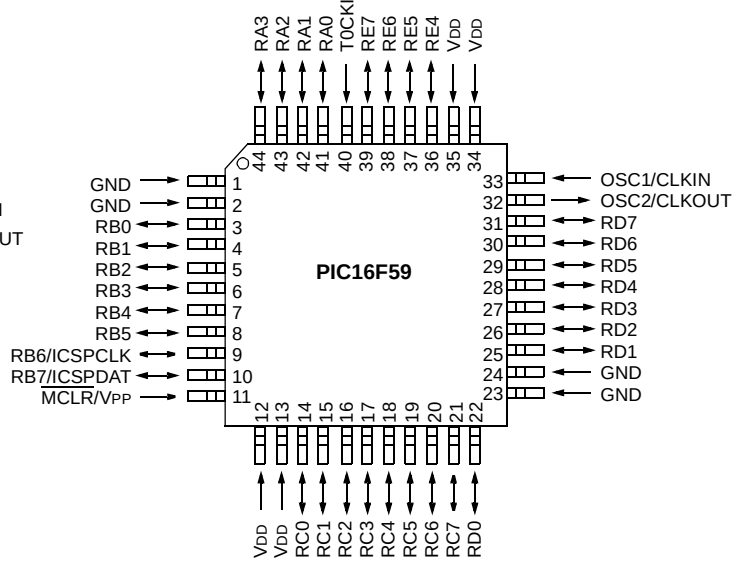


FIGURE 2-1: PIC16F5X SERIES BLOCK DIAGRAM

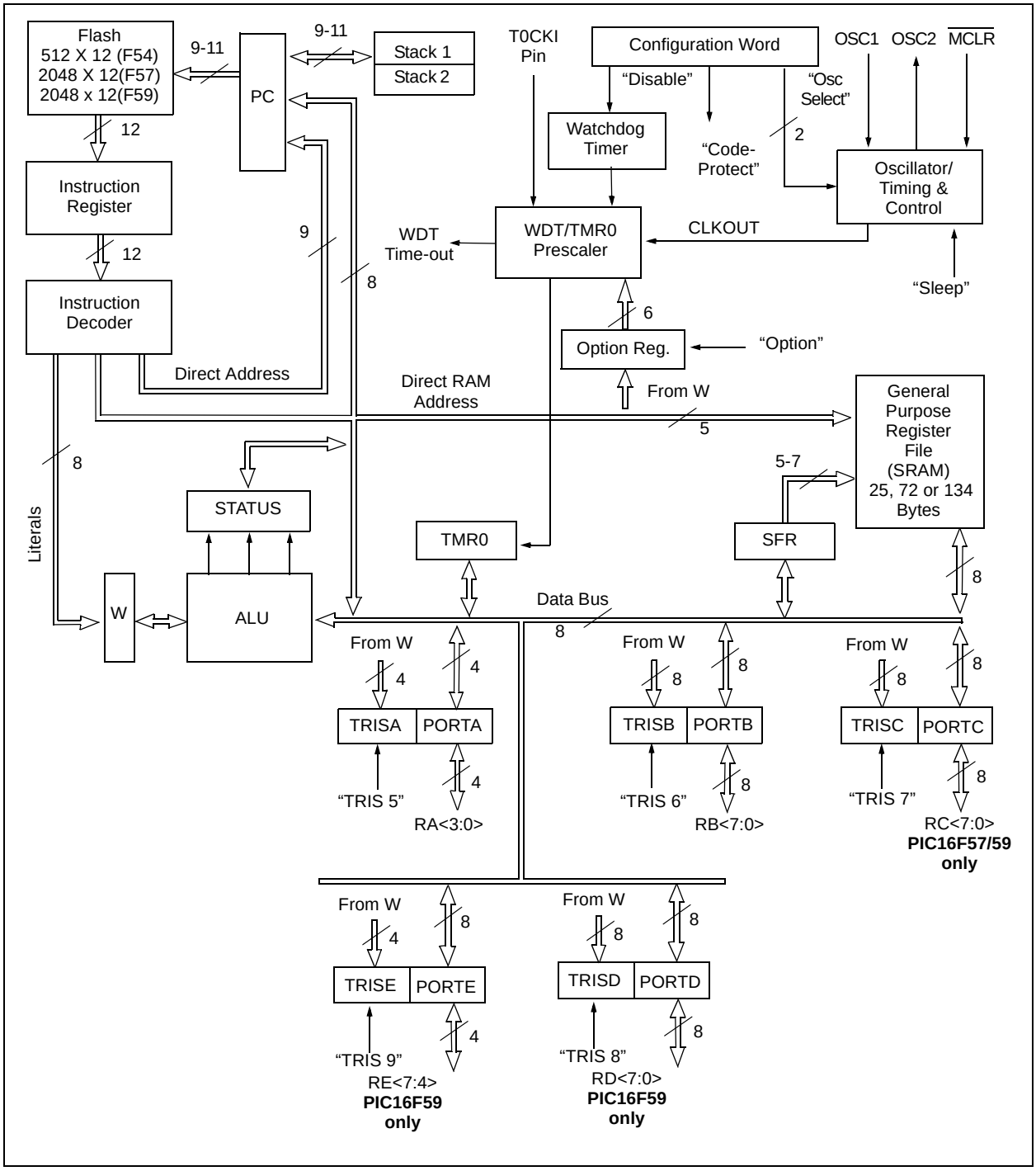


TABLE 2-2: PIC16F57 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0	RA0	TTL	CMOS	Bidirectional I/O pin
RA1	RA1	TTL	CMOS	Bidirectional I/O pin
RA2	RA2	TTL	CMOS	Bidirectional I/O pin
RA3	RA3	TTL	CMOS	Bidirectional I/O pin
RB0	RB0	TTL	CMOS	Bidirectional I/O pin
RB1	RB1	TTL	CMOS	Bidirectional I/O pin
RB2	RB2	TTL	CMOS	Bidirectional I/O pin
RB3	RB3	TTL	CMOS	Bidirectional I/O pin
RB4	RB4	TTL	CMOS	Bidirectional I/O pin
RB5	RB5	TTL	CMOS	Bidirectional I/O pin
RB6/ICSPCLK	RB6	TTL	CMOS	Bidirectional I/O pin
	ICSPCLK	ST	—	Serial programming clock
RB7/ICSPDAT	RB7	TTL	CMOS	Bidirectional I/O pin
	ICSPDAT	ST	CMOS	Serial programming I/O
RC0	RC0	TTL	CMOS	Bidirectional I/O pin
RC1	RC1	TTL	CMOS	Bidirectional I/O pin
RC2	RC2	TTL	CMOS	Bidirectional I/O pin
RC3	RC3	TTL	CMOS	Bidirectional I/O pin
RC4	RC4	TTL	CMOS	Bidirectional I/O pin
RC5	RC5	TTL	CMOS	Bidirectional I/O pin
RC6	RC6	TTL	CMOS	Bidirectional I/O pin
RC7	RC7	TTL	CMOS	Bidirectional I/O pin
T0CKI	T0CKI	ST	—	Clock input to Timer0. Must be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.
$\overline{MCLR}/V_{PP}$	$\overline{MCLR}$	ST	—	Active-low Reset to device. Voltage on the $\overline{MCLR}/V_{PP}$ pin must not exceed V_{DD} to avoid unintended entering of Programming mode.
	V_{PP}	HV	—	Programming voltage input
OSC1/CLKIN	OSC1	XTAL	—	Oscillator crystal input
	CLKIN	ST	—	External clock source input
OSC2/CLKOUT	OSC2	—	XTAL	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
	CLKOUT	—	CMOS	In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1.
V_{DD}	V_{DD}	Power	—	Positive supply for logic and I/O pins
V_{SS}	V_{SS}	Power	—	Ground reference for logic and I/O pins
N/C	N/C	—	—	Unused, do not connect

Legend: I = input, O = output, ST = Schmitt Trigger input, I/O = input/output, — = Not Used, TTL = TTL input, CMOS = CMOS output, XTAL = Crystal input/output, HV = High Voltage

3.6 Stack

The PIC16F54 device has a 9-bit wide, two-level hardware PUSH/POP stack. The PIC16F57 and PIC16F59 devices have an 11-bit wide, two-level hardware PUSH/POP stack.

A CALL instruction will PUSH the current value of stack 1 into stack 2 and then PUSH the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will POP the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2.

Note:	The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top-of-Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

3.7 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 3-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 09h)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although Status bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 3-2.

EXAMPLE 3-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
          MOVLW  H'10'  ;initialize pointer
          MOVWF  FSR    ;to RAM
NEXT      CLRF   INDF   ;clear INDF Register
          INCF   FSR,F  ;inc pointer
          BTFSC  FSR,4  ;all done?
          GOTO   NEXT   ;NO, clear next
CONTINUE
          :             ;YES, continue
```

The FSR is either a 5-bit (PIC16F54), 7-bit (PIC16F57) or 8-bit (PIC16F59) wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16F54: This does not use banking. FSR<7:5> bits are unimplemented and read as '1's.

PIC16F57: FSR<7> bit is unimplemented and read as '1'. FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = Bank 0, 01 = Bank 1, 10 = Bank 2, 11 = Bank 3).

PIC16F59: FSR<7:5> are the bank select bits and are used to select the bank to be addressed (000 = Bank 0, 001 = Bank 1, 010 = Bank 2, 011 = Bank 3, 100 = Bank 4, 101 = Bank 5, 110 = Bank 6, 111 = Bank 7).

Note:	A CLRF FSR instruction may not result in an FSR value of 00h if there are unimplemented bits present in the FSR.

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

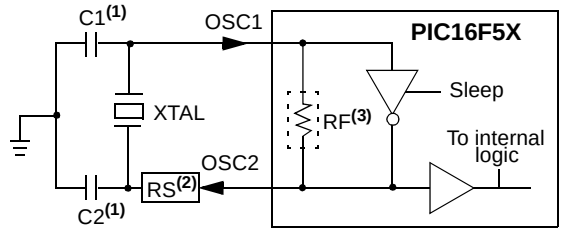
The PIC16F5X devices can be operated in four different oscillator modes. The user can program two Configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low-power Crystal
- XT: Crystal/Resonator
- HS: High-speed Crystal/Resonator
- RC: Resistor/Capacitor

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16F5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency outside of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required.
3: RF varies with the Oscillator mode chosen (approx. value = 10 MΩ).

FIGURE 4-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

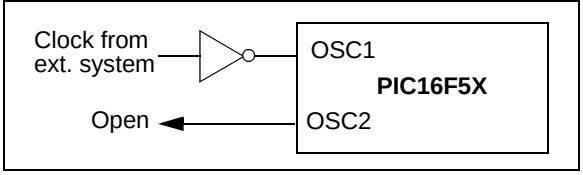


TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Osc Type	Resonator Freq.	Cap. Range C1	Cap. Range C2
XT	455 kHz 2.0 MHz 4.0 MHz	68-100 pF 15-33 pF 10-22 pF	68-100 pF 15-33 pF 10-22 pF
HS	8.0 MHz 16.0 MHz	10-22 pF 10 pF	10-22 pF 10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq.	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	100 kHz 200 kHz 455 kHz 1 MHz 2 MHz 4 MHz	15-30 pF 15-30 pF 15-30 pF 15-30 pF 15 pF 15 pF	200-300 pF 100-200 pF 15-100 pF 15-30 pF 15 pF 15 pF
HS	4 MHz 8 MHz 20 MHz	15 pF 15 pF 15 pF	15 pF 15 pF 15 pF

Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specifications. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Note 1: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

2: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD})

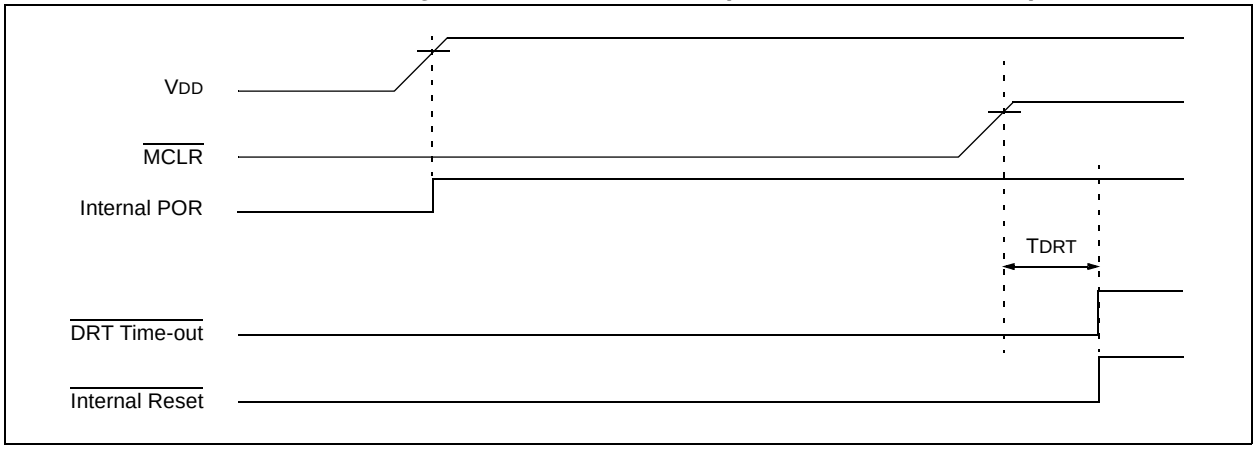


FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME

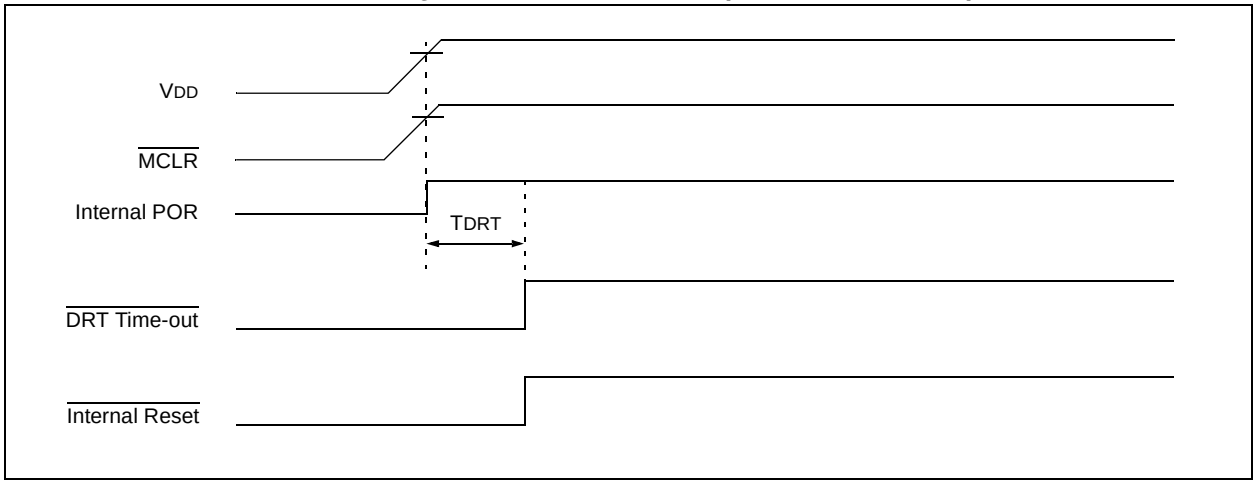
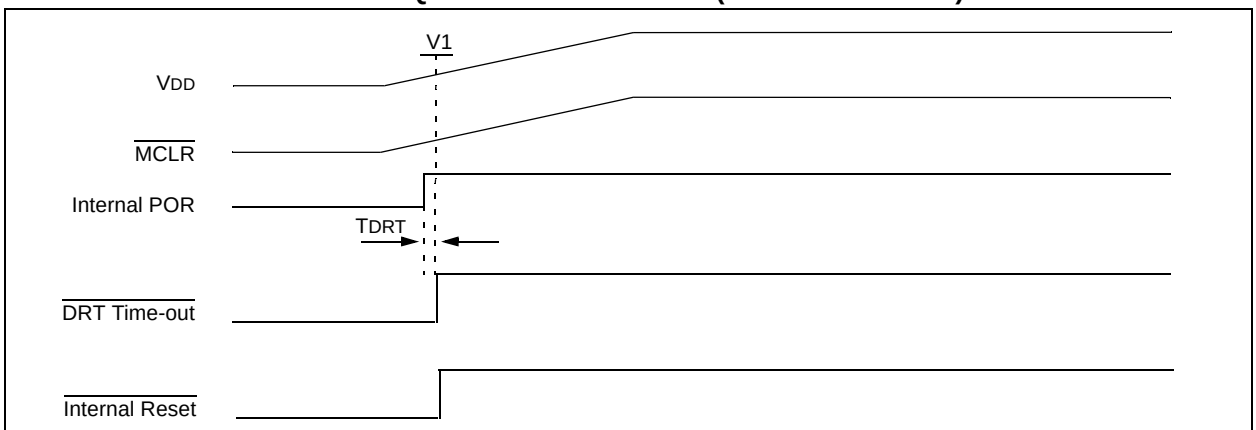


FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



Note : When V_{DD} rises slowly, the T_{DRT} time-out expires long before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ V_{DD} min.

7.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit Timer/Counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

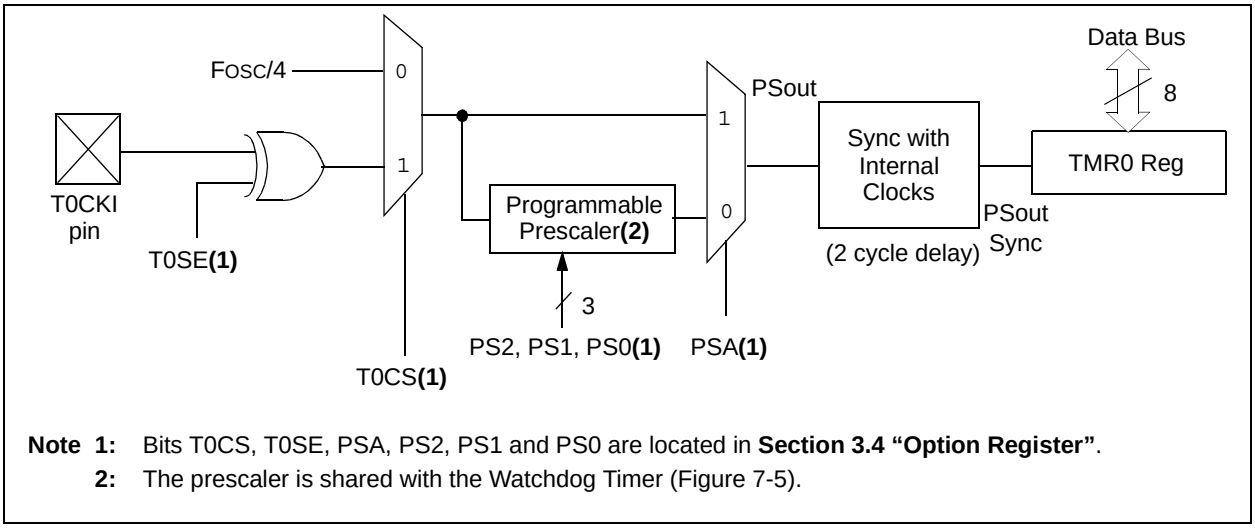
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 7.1 "Using Timer0 with an External Clock"**.

Note:	The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both.

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 7.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 7-1.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in **Section 3.4 "Option Register"**.

2: The prescaler is shared with the Watchdog Timer (Figure 7-5).

FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER

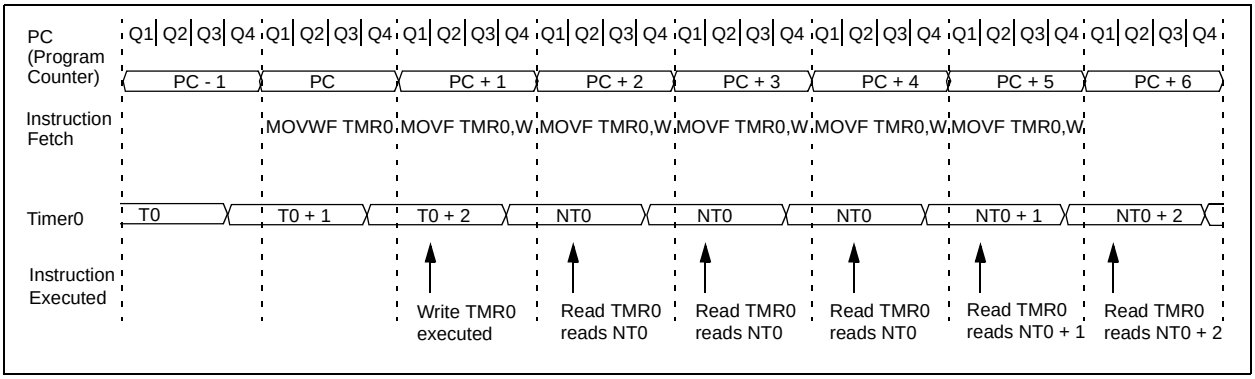


FIGURE 7-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2

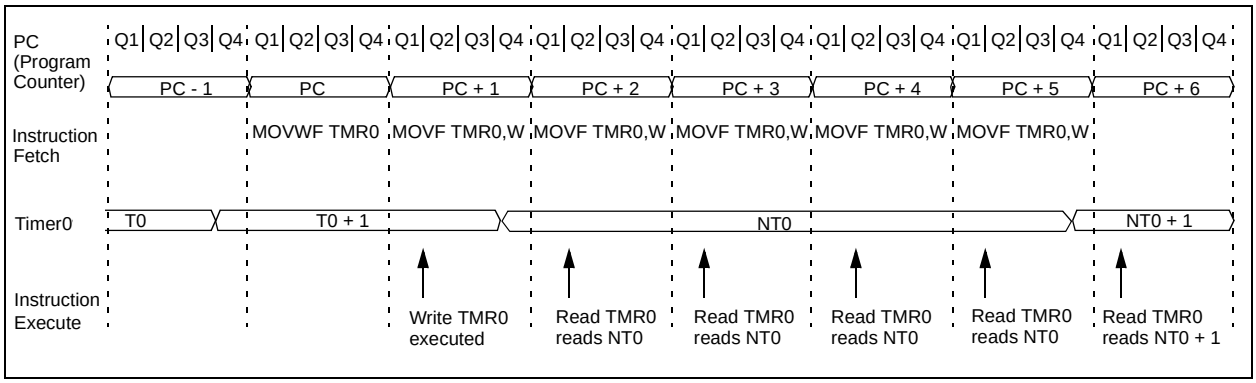


TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded cells not used by Timer0, - = unimplemented, x = unknown, u = unchanged.

7.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on-the-fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

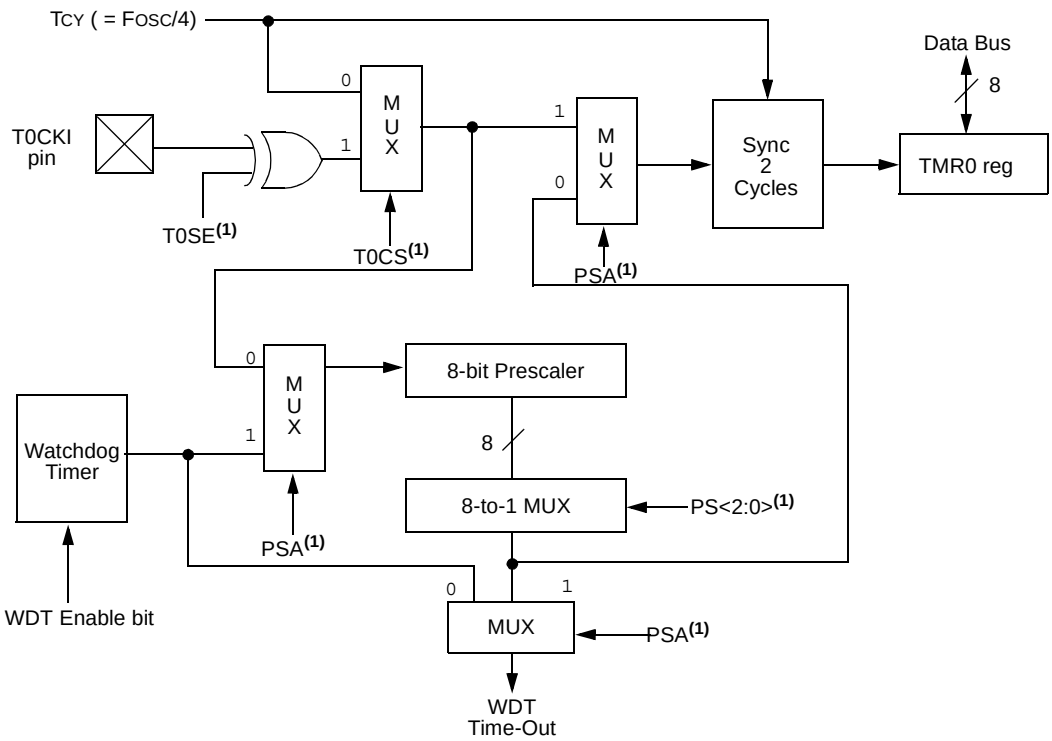
```
CLRWDT                ;Clear WDT
CLRF    TMR0          ;Clear TMR0 &  ;Prescaler
MOVLW   B'00xx1111'   ;Last 3 instructions
                      ;in this example
OPTION                ;are required only if
                      ;desired
CLRWDT                ;PS<2:0> are 000 or 001
MOVLW   B'00xx1xxx'   ;Set Prescaler to
OPTION                ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                ;Clear WDT and
                      ;prescaler
MOVLW   B'xxxx0xxx'   ;Select TMR0, new
                      ;prescale value and
                      ;clock source
OPTION
```

FIGURE 7-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA PS<2:0> are bits in the Option register.

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 31$

Operation: (W) → (f)

Status Affected: None

Encoding:

0000	001f	ffff

Description: Move data from the W register to register 'f'.

Words: 1

Cycles: 1

Example:

```
MOVWF  TEMP_REG
```

Before Instruction
TEMP_REG = 0xFF
W = 0x4F
After Instruction
TEMP_REG = 0x4F
W = 0x4F

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

0000	0000	0000

Description: No operation.

Words: 1

Cycles: 1

Example:

```
NOP
```

OPTION **Load OPTION Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

0000	0000	0010

Description: The content of the W register is loaded into the Option register.

Words: 1

Cycles: 1

Example:

```
OPTION
```

Before Instruction
W = 0x07
After Instruction
OPTION = 0x07

RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

1000	kkkk	kkkk

Description: The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Words: 1

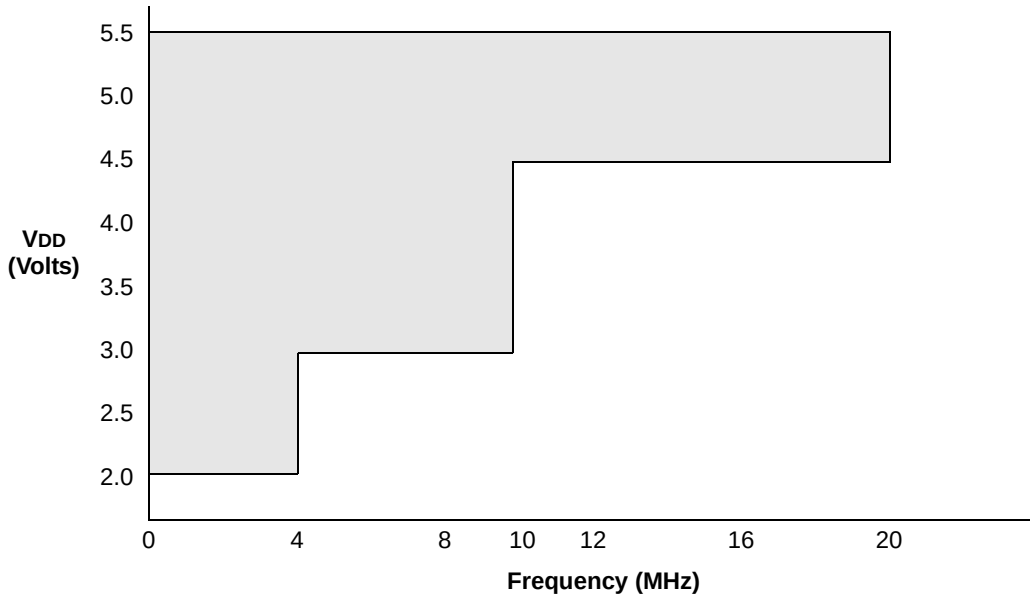
Cycles: 2

Example:

```
      CALL TABLE;W contains
                ;table offset
                ;value.
      •         ;W now has table
      •         ;value.
TABLE •
      ADDWF PC  ;W = offset
      RETLW k1  ;Begin table
      RETLW k2  ;
      •
      •
      •
      RETLW kn  ; End of table
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

FIGURE 11-1: PIC16F5X VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

11.2 DC Characteristics: PIC16F5X (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic/Device**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See **Section 5.1 "Power-on Reset (POR)"** for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See **Section 5.1 "Power-on Reset (POR)"** for details on Power-on Reset
D010	IDD	**Supply Current(2)**					
			— — — —	170 0.4 1.7 15	450 2.0 7.0 40	µA mA mA µA	FOSC = 4 MHz, VDD = 2.0V, XT or RC mode(3) FOSC = 10 MHz, VDD = 3.0V, HS mode FOSC = 20 MHz, VDD = 5.0V, HS mode FOSC = 32 kHz, VDD = 2.0V, LP mode, WDT disabled
D020	IPD	**Power-down Current(2)**					
			— —	1.0 0.5	15.0 8.0	µA µA	VDD = 2.0V, WDT enabled VDD = 2.0V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature, also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode. The Power-down Current in Sleep mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

11.3 DC Characteristics PIC16F5X

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
D030		I/O Ports	VSS	—	0.8V	V	4.5V <VDD ≤ 5.5V
		I/O Ports	VSS	—	0.15 VDD	V	VDD ≤ 4.5V
		$\overline{MCLR}$ (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		OSC1 (Schmitt Trigger)	VSS	—	0.15 VDD	V	RC mode(3)
		OSC1	VSS	—	0.3 VDD	V	HS mode
			VSS	—	0.3	V	XT mode
			VSS	—	0.3	V	LP mode
	VIH	**Input High Voltage**					
D040		I/O ports	2.0	—	VDD	V	4.5V < VDD ≤ 5.5V
		I/O ports	0.25 VDD + 0.8	—	VDD	V	VDD ≤ 4.5V
		$\overline{MCLR}$ (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1 (Schmitt Trigger)	0.85 VDD	—	VDD	V	RC mode(3)
		OSC1	0.7 VDD	—	VDD	V	HS mode
			1.6	—	VDD	V	XT mode
			1.6	—	VDD	V	LP mode
	IIL	**Input Leakage Current(1, 2)**					
D060		I/O ports	—	—	±1.0	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
		$\overline{MCLR}$	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD
		T0CKI	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD
		OSC1	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
D083		OSC2/CLKOUT (RC mode)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V
	VOH	**Output High Voltage(2)**					
D090		I/O ports(2)	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V

* These parameters are characterized but not tested.

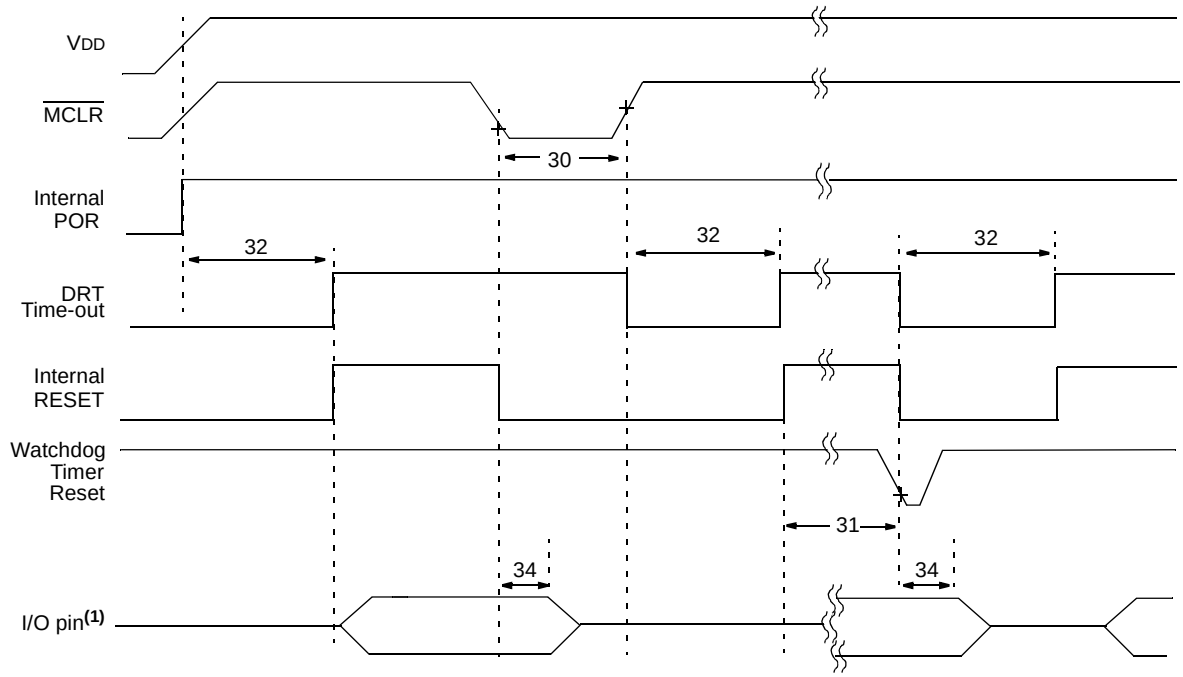
† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F5X be driven with external clock in RC mode.

FIGURE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING -– PIC16F5X



Note 1: Please refer to Figure 11-2 for load conditions.

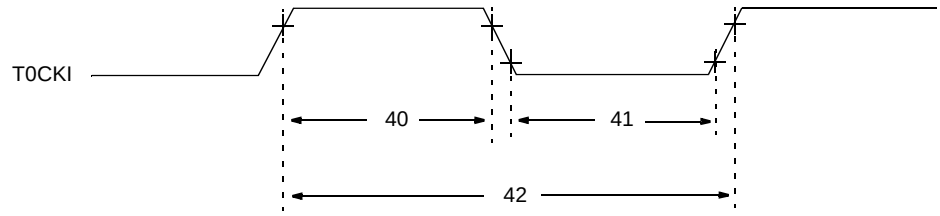
TABLE 11-3: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER – PIC16F5X

AC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2000*	—	—	ns	VDD = 5.0V
31	TWDT	Watchdog Timer Time-out Period (No Prescaler) Watchdog Timer Time-out Period (No Prescaler)	9.0* 9.0*	18* 18*	30* 40*	ms	VDD = 5.0V (industrial) VDD = 5.0V (extended)
32	TDRT	Device Reset Timer Period Device Reset Timer Period	9.0* 9.0*	18* 18*	30* 40*	ms	VDD = 5.0V (industrial) VDD = 5.0V (extended)
34	TIOZ	I/O high-impedance from $\overline{\text{MCLR}}$ Low	100*	300*	2000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-6: TIMER0 CLOCK TIMINGS – PIC16F5X



Note: Please refer to Figure 11-2 for load conditions.

TABLE 11-4: TIMER0 CLOCK REQUIREMENTS – PIC16F5X

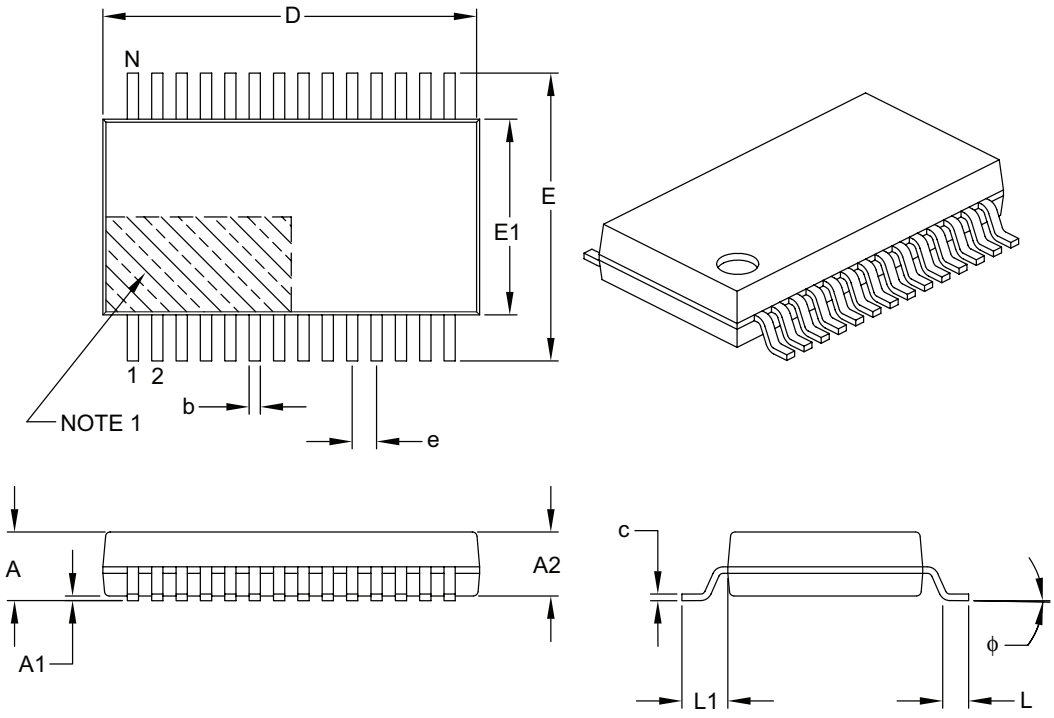
AC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width: No Prescaler	0.5 TCY + 20*	—	—	ns	
		With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width: No Prescaler	0.5 TCY + 20*	—	—	ns	
		With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision D (04/2007)

Changed PICmicro to PIC; Replaced Dev. Tool Section; Updated Package Marking Information and replaced Package Drawings (Rev. AP)