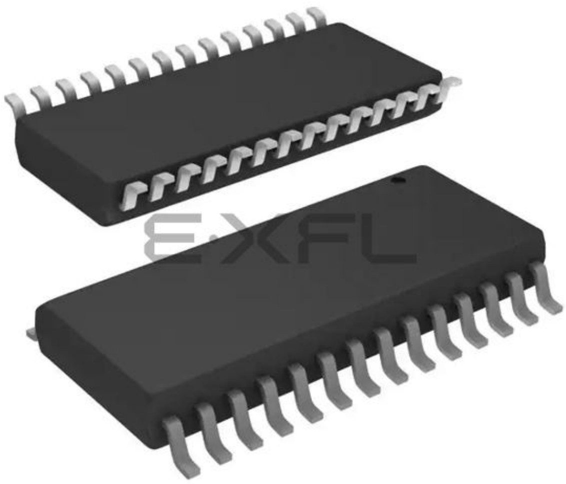

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f57-e-so

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TABLE 2-2: PIC16F57 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0	RA0	TTL	CMOS	Bidirectional I/O pin
RA1	RA1	TTL	CMOS	Bidirectional I/O pin
RA2	RA2	TTL	CMOS	Bidirectional I/O pin
RA3	RA3	TTL	CMOS	Bidirectional I/O pin
RB0	RB0	TTL	CMOS	Bidirectional I/O pin
RB1	RB1	TTL	CMOS	Bidirectional I/O pin
RB2	RB2	TTL	CMOS	Bidirectional I/O pin
RB3	RB3	TTL	CMOS	Bidirectional I/O pin
RB4	RB4	TTL	CMOS	Bidirectional I/O pin
RB5	RB5	TTL	CMOS	Bidirectional I/O pin
RB6/ICSPCLK	RB6	TTL	CMOS	Bidirectional I/O pin
	ICSPCLK	ST	—	Serial programming clock
RB7/ICSPDAT	RB7	TTL	CMOS	Bidirectional I/O pin
	ICSPDAT	ST	CMOS	Serial programming I/O
RC0	RC0	TTL	CMOS	Bidirectional I/O pin
RC1	RC1	TTL	CMOS	Bidirectional I/O pin
RC2	RC2	TTL	CMOS	Bidirectional I/O pin
RC3	RC3	TTL	CMOS	Bidirectional I/O pin
RC4	RC4	TTL	CMOS	Bidirectional I/O pin
RC5	RC5	TTL	CMOS	Bidirectional I/O pin
RC6	RC6	TTL	CMOS	Bidirectional I/O pin
RC7	RC7	TTL	CMOS	Bidirectional I/O pin
T0CKI	T0CKI	ST	—	Clock input to Timer0. Must be tied to VSS or VDD, if not in use, to reduce current consumption.
$\overline{MCLR}$/VPP	$\overline{MCLR}$	ST	—	Active-low Reset to device. Voltage on the $\overline{MCLR}$/VPP pin must not exceed VDD to avoid unintended entering of Programming mode.
	VPP	HV	—	Programming voltage input
OSC1/CLKIN	OSC1	XTAL	—	Oscillator crystal input
	CLKIN	ST	—	External clock source input
OSC2/CLKOUT	OSC2	—	XTAL	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
	CLKOUT	—	CMOS	In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1.
VDD	VDD	Power	—	Positive supply for logic and I/O pins
VSS	VSS	Power	—	Ground reference for logic and I/O pins
N/C	N/C	—	—	Unused, do not connect

Legend: I = input; O = output; ST = Schmitt Trigger input; I/O = input/output; — = Not Used; TTL = TTL input; CMOS = CMOS output; XTAL = Crystal input/output; HV = High Voltage

TABLE 2-3: PIC16F59 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0	RA0	TTL	CMOS	Bidirectional I/O pin
RA1	RA1	TTL	CMOS	Bidirectional I/O pin
RA2	RA2	TTL	CMOS	Bidirectional I/O pin
RA3	RA3	TTL	CMOS	Bidirectional I/O pin
RB0	RB0	TTL	CMOS	Bidirectional I/O pin
RB1	RB1	TTL	CMOS	Bidirectional I/O pin
RB2	RB2	TTL	CMOS	Bidirectional I/O pin
RB3	RB3	TTL	CMOS	Bidirectional I/O pin
RB4	RB4	TTL	CMOS	Bidirectional I/O pin
RB5	RB5	TTL	CMOS	Bidirectional I/O pin
RB6/ICSPCLK	RB6	TTL	CMOS	Bidirectional I/O pin
	ICSPCLK	ST	—	Serial programming clock
RB7/ICSPDAT	RB7	TTL	CMOS	Bidirectional I/O pin
	ICSPDAT	ST	CMOS	Serial programming I/O
RC0	RC0	TTL	CMOS	Bidirectional I/O pin
RC1	RC1	TTL	CMOS	Bidirectional I/O pin
RC2	RC2	TTL	CMOS	Bidirectional I/O pin
RC3	RC3	TTL	CMOS	Bidirectional I/O pin
RC4	RC4	TTL	CMOS	Bidirectional I/O pin
RC5	RC5	TTL	CMOS	Bidirectional I/O pin
RC6	RC6	TTL	CMOS	Bidirectional I/O pin
RC7	RC7	TTL	CMOS	Bidirectional I/O pin
RD0	RD0	TTL	CMOS	Bidirectional I/O pin
RD1	RD1	TTL	CMOS	Bidirectional I/O pin
RD2	RD2	TTL	CMOS	Bidirectional I/O pin
RD3	RD3	TTL	CMOS	Bidirectional I/O pin
RD4	RD4	TTL	CMOS	Bidirectional I/O pin
RD5	RD5	TTL	CMOS	Bidirectional I/O pin
RD6	RD6	TTL	CMOS	Bidirectional I/O pin
RD7	RD7	TTL	CMOS	Bidirectional I/O pin
RE4	RE4	TTL	CMOS	Bidirectional I/O pin
RE5	RE5	TTL	CMOS	Bidirectional I/O pin
RE6	RE6	TTL	CMOS	Bidirectional I/O pin
RE7	RE7	TTL	CMOS	Bidirectional I/O pin
T0CKI	T0CKI	ST	—	Clock input to Timer0. Must be tied to VSS or VDD, if not in use, to reduce current consumption.
$\overline{\text{MCLR}}$/VPP	$\overline{\text{MCLR}}$	ST	—	Active-low Reset to device. Voltage on the $\overline{\text{MCLR}}$/VPP pin must not exceed VDD to avoid unintended entering of Programming mode.
	VPP	HV	—	Programming voltage input
OSC1/CLKIN	OSC1	XTAL	—	Oscillator crystal input
	CLKIN	ST	—	External clock source input
OSC2/CLKOUT	OSC2	—	XTAL	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
	CLKOUT	—	CMOS	In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1.
VDD	VDD	Power	—	Positive supply for logic and I/O pins
VSS	VSS	Power	—	Ground reference for logic and I/O pins

Legend: I = input; O = output; ST = Schmitt Trigger input; I/O = input/output; — = Not Used; TTL = TTL input; CMOS = CMOS output; XTAL = Crystal input/output; HV = High Voltage

3.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFR) are registers used by the CPU and peripheral functions to control the operation of the device (Table 3-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 3-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC, TRISD, TRISE)								`1111 1111`	29
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								`--11 1111`	18
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								`xxxx xxxx`	20
01h	TMR0	Timer0 Module Register								`xxxx xxxx`	34
02h	PCL(1)	Low order 8 bits of PC								`1111 1111`	19
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	`0001 1xxx`	17
04h	FSR(3)	Indirect data memory Address Pointer								`111x xxxx`	20
04h	FSR(4)	Indirect data memory Address Pointer								`1xxx xxxx`	20
04h	FSR(5)	Indirect data memory Address Pointer								`xxxx xxxx`	20
05h	PORTA(6)	—	—	—	—	RA3	RA2	RA1	RA0	`---- xxxx`	29
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	`xxxx xxxx`	29
07h	PORTC(2)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	`xxxx xxxx`	29
08h	PORTD(7)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	`xxxx xxxx`	29
09h	PORTE(6), (7)	RE7	RE6	RE5	RE4	—	—	—	—	`xxxx ----`	29

Legend: Shaded cells = unimplemented or unused, – = unimplemented, read as ‘0’ (if applicable), x = unknown, u = unchanged

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 3.5 “Program Counter”** for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16F54.

3: PIC16F54 only.

4: PIC16F57 only.

5: PIC16F59 only.

6: Unimplemented bits are read as ‘0’s.

7: File address 08h and 09h are General Purpose Registers on the PIC16F54 and PIC16F57.

3.6 Stack

The PIC16F54 device has a 9-bit wide, two-level hardware PUSH/POP stack. The PIC16F57 and PIC16F59 devices have an 11-bit wide, two-level hardware PUSH/POP stack.

A `CALL` instruction will PUSH the current value of stack 1 into stack 2 and then PUSH the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will POP the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2.

Note:	The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the `RETLW` instruction, the PC is loaded with the Top-of-Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

3.7 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 3-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 09h)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = `0`) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although Status bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 3-2.

EXAMPLE 3-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
         MOVLW  H'10'  ;initialize pointer
         MOVWF  FSR    ;to RAM
NEXT     CLRF   INDF   ;clear INDF Register
         INCF   FSR,F  ;inc pointer
         BTFSC  FSR,4  ;all done?
         GOTO   NEXT   ;NO, clear next
CONTINUE
         :             ;YES, continue
```

The FSR is either a 5-bit (PIC16F54), 7-bit (PIC16F57) or 8-bit (PIC16F59) wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16F54: This does not use banking. FSR<7:5> bits are unimplemented and read as '`1`'s.

PIC16F57: FSR<7> bit is unimplemented and read as '`1`'. FSR<6:5> are the bank select bits and are used to select the bank to be addressed (`00` = Bank 0, `01` = Bank 1, `10` = Bank 2, `11` = Bank 3).

PIC16F59: FSR<7:5> are the bank select bits and are used to select the bank to be addressed (`000` = Bank 0, `001` = Bank 1, `010` = Bank 2, `011` = Bank 3, `100` = Bank 4, `101` = Bank 5, `110` = Bank 6, `111` = Bank 7).

Note:	A `CLRF FSR` instruction may not result in an FSR value of 00h if there are unimplemented bits present in the FSR.

5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on Reset regardless of the oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in Reset as long as the DRT is active. The DRT delay allows V_{DD} to rise above V_{DD} min. and for the chosen oscillator to stabilize.

Oscillator circuits, based on crystals or ceramic resonators, require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a Reset condition for approximately 18 ms after the voltage on the $\overline{MCLR}/V_{PP}$ pin has reached a logic high (V_{IH}) level. Thus, external RC networks connected to the $\overline{MCLR}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The device Reset time delay will vary from chip-to-chip due to V_{DD}, temperature and process variation. See AC parameters for details.

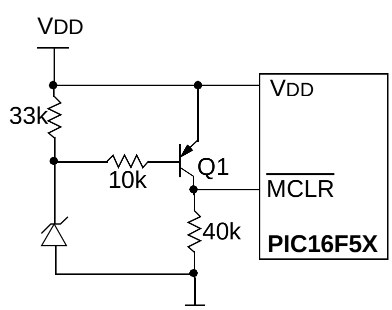
The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16F5X from Sleep mode automatically.

5.3 Reset on Brown-Out

A Brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a Brown-out.

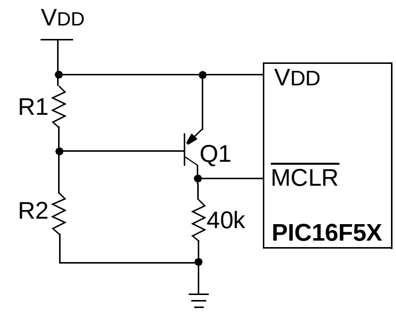
To reset PIC16F5X devices when a Brown-out occurs, external Brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.

FIGURE 5-6: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate Reset when V_{DD} goes below $V_Z + 0.7V$ (where V_Z = Zener voltage).

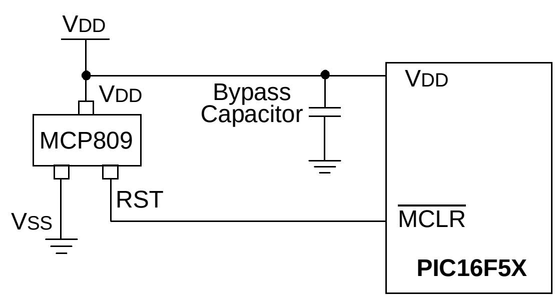
FIGURE 5-7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

FIGURE 5-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both "active-high and active-low" Reset pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

NOTES:

ADDWF — Add W and f

Syntax:	[*label*] ADDWF f, d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) + (f) → (dest)
Status Affected:	C, DC, Z
Encoding:	`0001` | `11df` | `ffff`
Description:	Add the contents of the W register and register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	`ADDWF TEMP_REG, 0`

Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0xD9
TEMP_REG = 0xC2

ANDWF — AND W with f

Syntax:	[*label*] ANDWF f, d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (dest)
Status Affected:	Z
Encoding:	`0001` | `01df` | `ffff`
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	`ANDWF TEMP_REG, 1`

Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0x17
TEMP_REG = 0x02

ANDLW — AND literal with W

Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W).AND. (k) → (W)
Status Affected:	Z
Encoding:	`1110` | `kkkk` | `kkkk`
Description:	The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	`ANDLW H'5F'`

Before Instruction
W = 0xA3
After Instruction
W = 0x03

BCF — Bit Clear f

Syntax:	[*label*] BCF f, b
Operands:	$0 \le f \le 31$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Encoding:	`0100` | `bbbf` | `ffff`
Description:	Bit 'b' in register 'f' is cleared.
Words:	1
Cycles:	1
Example:	`BCF FLAG_REG, 7`

Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

XORLW — Exclusive OR literal with W

Syntax:	[*label*] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. k $\rightarrow$ (W)
Status Affected:	Z
Encoding:	`1111` `kkkk` `kkkk`
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	`XORLW` 0xAF

Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF — Exclusive OR W with f

Syntax:	[*label*] XORWF f, d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)
Status Affected:	Z
Encoding:	`0001` `10df` `ffff`
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '`0`', the result is stored in the W register. If 'd' is '`1`', the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	`XORWF REG,1`

Before Instruction
REG = 0xAF
W = 0xB5
After Instruction
REG = 0x1A
W = 0xB5

11.1 DC Characteristics: PIC16F5X (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym.**	**Characteristic/Device**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage**(1)	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See **Section 5.1 "Power-on Reset (POR)"** for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See **Section 5.1 "Power-on Reset (POR)"** for details on Power-on Reset
D010	IDD	**Supply Current**(2)					
			—	170	350	µA	FOSC = 4 MHz, VDD = 2.0V, XT or RC mode(3)
			—	0.4	1.0	mA	FOSC = 10 MHz, VDD = 3.0V, HS mode
			—	1.7	5.0	mA	FOSC = 20 MHz, VDD = 5.0V, HS mode
			—	15	22.5	µA	FOSC = 32 kHz, VDD = 2.0V, LP mode, WDT disabled
D020	IPD	**Power-down Current**(2)					
			—	1.0	6.0	µA	VDD = 2.0V, WDT enabled
			—	0.5	2.5	µA	VDD = 2.0V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature, also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode. The Power-down Current in Sleep mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

11.2 DC Characteristics: PIC16F5X (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ T_A ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic/Device**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage**(1)	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See **Section 5.1 "Power-on Reset (POR)"** for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See **Section 5.1 "Power-on Reset (POR)"** for details on Power-on Reset
D010	IDD	**Supply Current**(2)					
			—	170	450	μA	FOSC = 4 MHz, VDD = 2.0V, XT or RC mode(3)
			—	0.4	2.0	mA	FOSC = 10 MHz, VDD = 3.0V, HS mode
			—	1.7	7.0	mA	FOSC = 20 MHz, VDD = 5.0V, HS mode
			—	15	40	μA	FOSC = 32 kHz, VDD = 2.0V, LP mode, WDT disabled
D020	IPD	**Power-down Current**(2)					
			—	1.0	15.0	μA	VDD = 2.0V, WDT enabled
			—	0.5	8.0	μA	VDD = 2.0V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

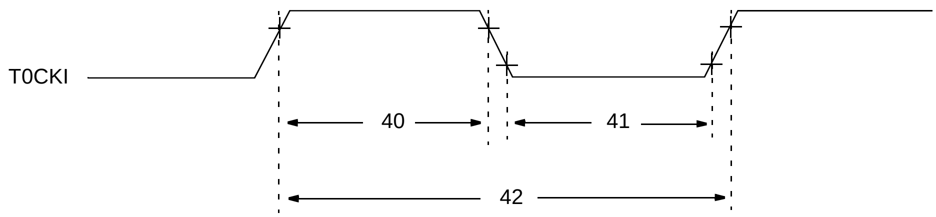
2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature, also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode. The Power-down Current in Sleep mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 11-6: TIMER0 CLOCK TIMINGS – PIC16F5X



Note: Please refer to Figure 11-2 for load conditions.

TABLE 11-4: TIMER0 CLOCK REQUIREMENTS – PIC16F5X

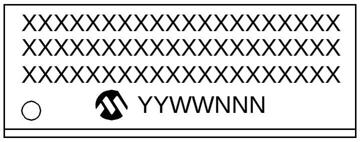
AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ T_A ≤ +85°C for industrial -40°C ≤ T_A ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width:					
		No Prescaler	0.5 T_{CY} + 20*	—	—	ns	
		With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width:					
		No Prescaler	0.5 T_{CY} + 20*	—	—	ns	
		With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

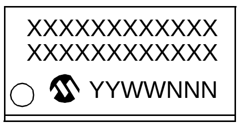
Package Marking Information (Continued)

28-Lead SOIC



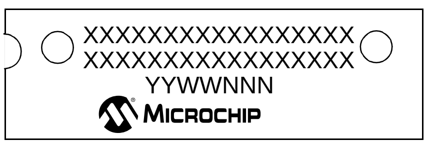
Example

28-Lead SSOP

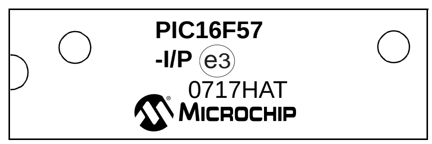


Example

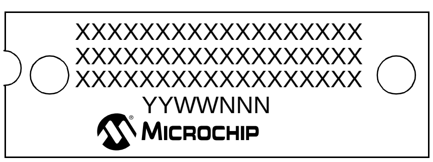
28-Lead SPDIP (.300")

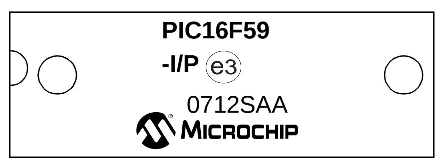


Example

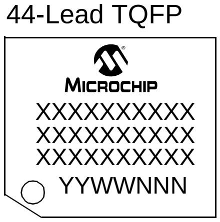


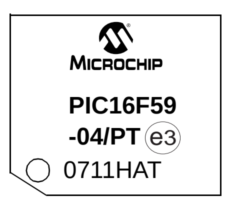
40-Lead PDIP (.600")





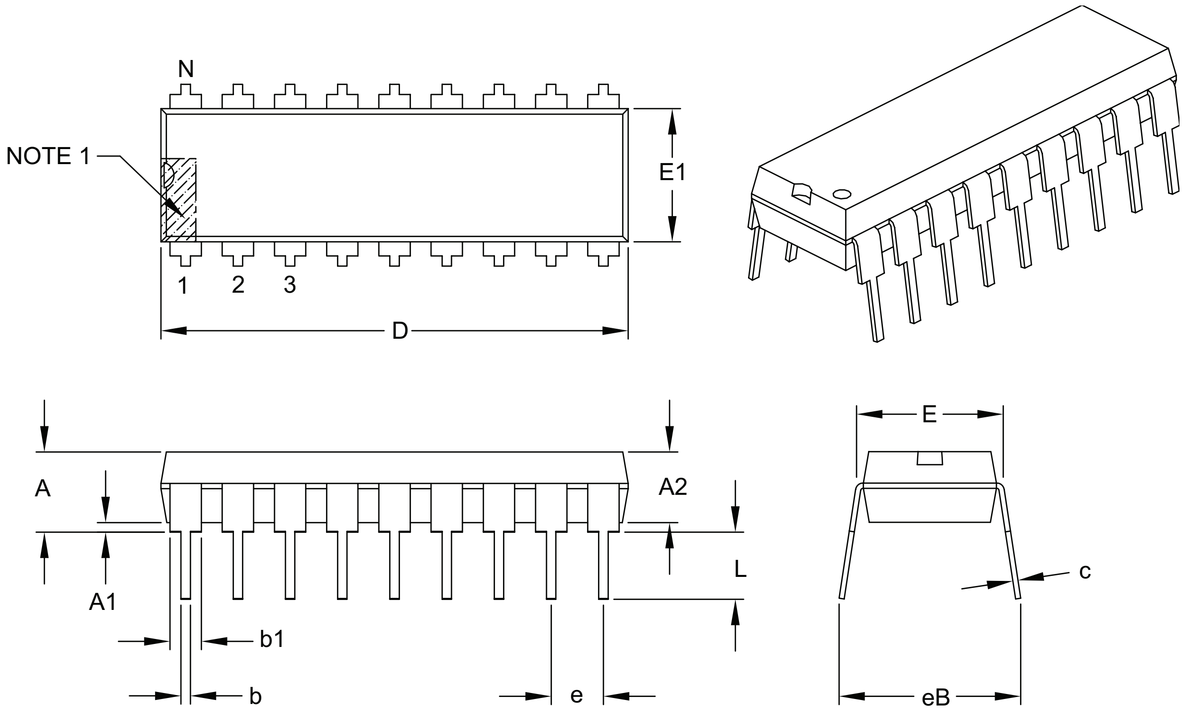
44-Lead TQFP





18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	18		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

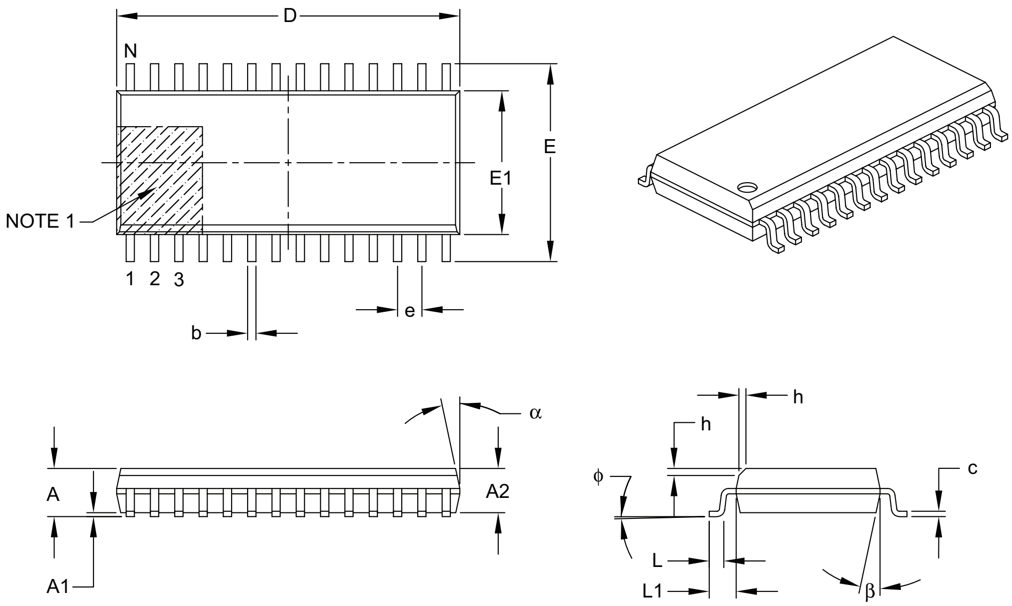
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS	
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	φ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision D (04/2007)

Changed PICmicro to PIC; Replaced Dev. Tool Section; Updated Package Marking Information and replaced Package Drawings (Rev. AP)

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16F54 PIC16F54T(1) PIC16F57 PIC16F57T(1)	– V_{DD} range 2.0V to 5.5V – V_{DD} range 2.0V to 5.5V – V_{DD} range 2.0V to 5.5V – V_{DD} range 2.0V to 5.5V
Temperature Range	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package	SO SS P SP SOG SSG PG SPG	= SOIC = SSOP = PDIP = Skinny Plastic DIP (SPDIP)(2) = SOIC (Pb-free) = SOIC (Pb-free) = SOIC (Pb-free) = SOIC (Pb-free)
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F54–I/P = Industrial temp, PDIP package
b) PIC16F54T–I/SSG = Industrial temp, SSOP package (Pb -free), tape and reel
c) PIC16F57–E/SP6 = Extended temp, Skinny Plastic DIP package (Pb-free)
d) PIC16F57T–E/SS = Extended temp, SSOP package, tape and reel
e) PIC16F54–I/SOG = Industrial temp, SOIC package (Pb-free)

Note 1: T = in tape and reel SOIC and SSOP packages only.
2: PIC16F57 only

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16F59 PIC16F59T(1)	– V_{DD} range 2.0V to 5.5V – V_{DD} range 2.0V to 5.5V
Temperature Range	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package	P PT	= PDIP = TQFP
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F59–I/P = Industrial temp, PDIP package (Pb-free).
b) PIC16F59T–I/PT = Industrial temp, TQFP package (Pb-free), tape and reel.

Note 1: T = in tape and reel TQFP packages only.

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