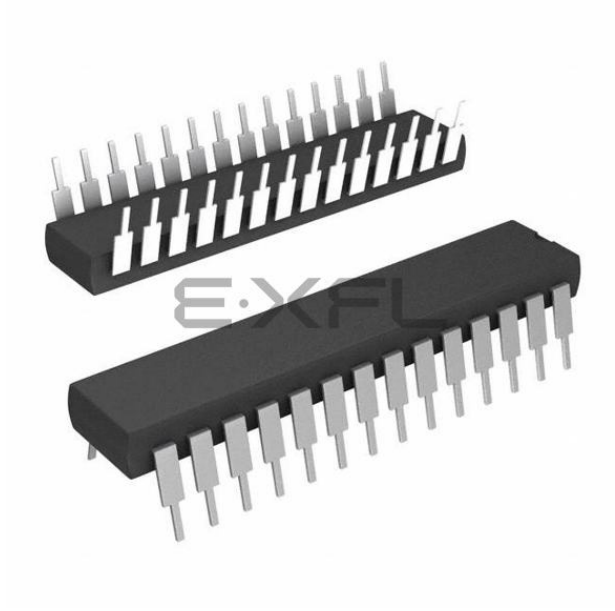

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f57-i-sp

PIC16F5X

Flash-Based, 8-Bit CMOS Microcontroller Series

High-Performance RISC CPU:

- Only 33 single-word instructions to learn
- All instructions are single cycle except for program branches which are two-cycle
- Two-level deep hardware stack
- Direct, Indirect and Relative Addressing modes for data and instructions
- Operating speed:
  - DC – 20 MHz clock speed
  - DC – 200 ns instruction cycle time
- On-chip Flash program memory:
  - 512 x 12 on PIC16F54
  - 2048 x 12 on PIC16F57
  - 2048 x 12 on PIC16F59
- General Purpose Registers (SRAM):
  - 25 x 8 on PIC16F54
  - 72 x 8 on PIC16F57
  - 134 x 8 on PIC16F59

Special Microcontroller Features:

- Power-on Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable Code Protection
- Power-Saving Sleep mode
- In-Circuit Serial Programming™ (ICSP™)
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power-saving, low-frequency crystal
- Packages:
  - 18-pin PDIP and SOIC for PIC16F54
  - 20-pin SSOP for PIC16F54
  - 28-pin PDIP, SOIC and SSOP for PIC16F57
  - 40-pin PDIP for PIC16F59
  - 44-pin TQFP for PIC16F59

Low-Power Features:

- Operating Current:
  - 170 μA @ 2V, 4 MHz, typical
  - 15 μA @ 2V, 32 kHz, typical
- Standby Current:
  - 500 nA @ 2V, typical

Peripheral Features:

- 12/20/32 I/O pins:
  - Individual direction control
  - High current source/sink
- 8-bit real-time clock/counter (TMR0) with 8-bit programmable prescaler

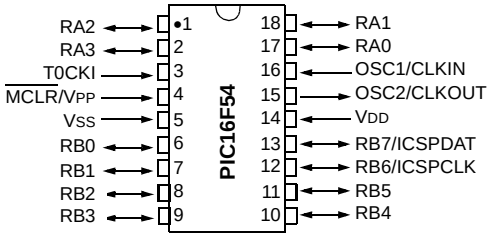
CMOS Technology:

- Wide operating voltage range:
  - Industrial: 2.0V to 5.5V
  - Extended: 2.0V to 5.5V
- Wide temperature range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C
- High-endurance Flash:
  - 100K write/erase cycles
  - > 40-year retention

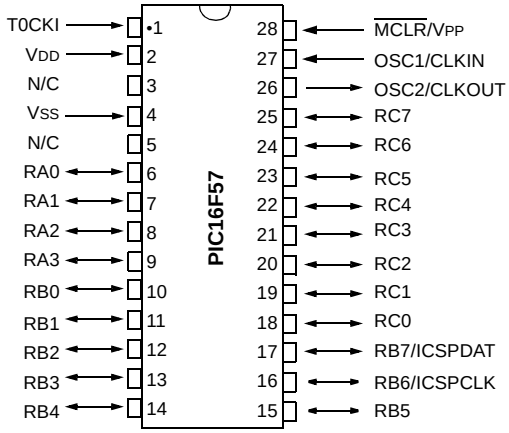
Device	Program Memory	Data Memory	I/O	Timers 8-bit
	Flash (words)	SRAM (bytes)		
PIC16F54	512	25	12	1
PIC16F57	2048	72	20	1
PIC16F59	2048	134	32	1

Pin Diagrams

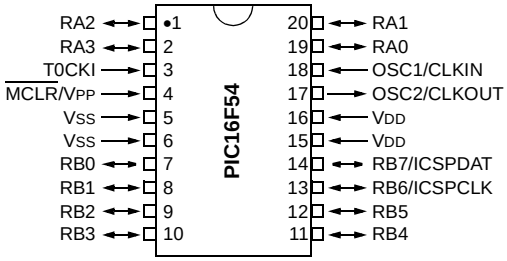
PDIP, SOIC



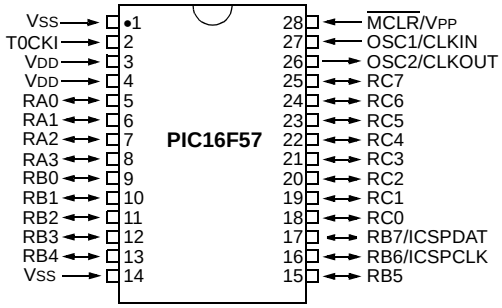
PDIP, SOIC



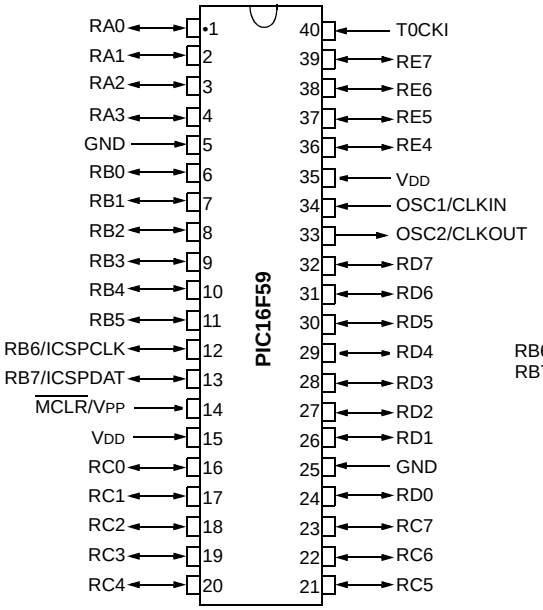
SSOP



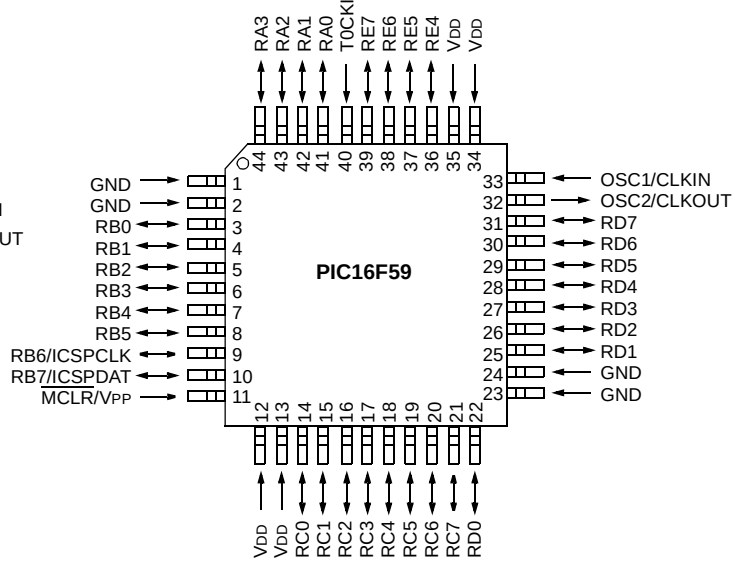
SSOP



PDIP, 0.600"



TQFP



NOTES:

TABLE 2-2: PIC16F57 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0	RA0	TTL	CMOS	Bidirectional I/O pin
RA1	RA1	TTL	CMOS	Bidirectional I/O pin
RA2	RA2	TTL	CMOS	Bidirectional I/O pin
RA3	RA3	TTL	CMOS	Bidirectional I/O pin
RB0	RB0	TTL	CMOS	Bidirectional I/O pin
RB1	RB1	TTL	CMOS	Bidirectional I/O pin
RB2	RB2	TTL	CMOS	Bidirectional I/O pin
RB3	RB3	TTL	CMOS	Bidirectional I/O pin
RB4	RB4	TTL	CMOS	Bidirectional I/O pin
RB5	RB5	TTL	CMOS	Bidirectional I/O pin
RB6/ICSPCLK	RB6	TTL	CMOS	Bidirectional I/O pin
	ICSPCLK	ST	—	Serial programming clock
RB7/ICSPDAT	RB7	TTL	CMOS	Bidirectional I/O pin
	ICSPDAT	ST	CMOS	Serial programming I/O
RC0	RC0	TTL	CMOS	Bidirectional I/O pin
RC1	RC1	TTL	CMOS	Bidirectional I/O pin
RC2	RC2	TTL	CMOS	Bidirectional I/O pin
RC3	RC3	TTL	CMOS	Bidirectional I/O pin
RC4	RC4	TTL	CMOS	Bidirectional I/O pin
RC5	RC5	TTL	CMOS	Bidirectional I/O pin
RC6	RC6	TTL	CMOS	Bidirectional I/O pin
RC7	RC7	TTL	CMOS	Bidirectional I/O pin
T0CKI	T0CKI	ST	—	Clock input to Timer0. Must be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.
$\overline{MCLR}/V_{PP}$	$\overline{MCLR}$	ST	—	Active-low Reset to device. Voltage on the $\overline{MCLR}/V_{PP}$ pin must not exceed V_{DD} to avoid unintended entering of Programming mode.
	V_{PP}	HV	—	Programming voltage input
OSC1/CLKIN	OSC1	XTAL	—	Oscillator crystal input
	CLKIN	ST	—	External clock source input
OSC2/CLKOUT	OSC2	—	XTAL	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
	CLKOUT	—	CMOS	In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1.
V_{DD}	V_{DD}	Power	—	Positive supply for logic and I/O pins
V_{SS}	V_{SS}	Power	—	Ground reference for logic and I/O pins
N/C	N/C	—	—	Unused, do not connect

Legend: I = input, O = output, ST = Schmitt Trigger input, I/O = input/output, — = Not Used, TTL = TTL input, CMOS = CMOS output, XTAL = Crystal input/output, HV = High Voltage

3.0 MEMORY ORGANIZATION

PIC16F5X memory is organized into program memory and data memory. For the PIC16F57 and PIC16F59, which have more than 512 words of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS register bits. For the PIC16F57 and PIC16F59, which have a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

3.1 Program Memory Organization

The PIC16F54 has a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 3-1). The PIC16F57 and PIC16F59 have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 3-2). Accessing a location above the physically implemented address will cause a wraparound.

A NOP at the Reset vector location will cause a restart at location 000h. The Reset vector for the PIC16F54 is at 1FFh. The Reset vector for the PIC16F57 and PIC16F59 is at 7FFh. See **Section 3.5 "Program Counter"** for additional information using CALL and GOTO instructions.

FIGURE 3-1: PIC16F54 PROGRAM MEMORY MAP AND STACK

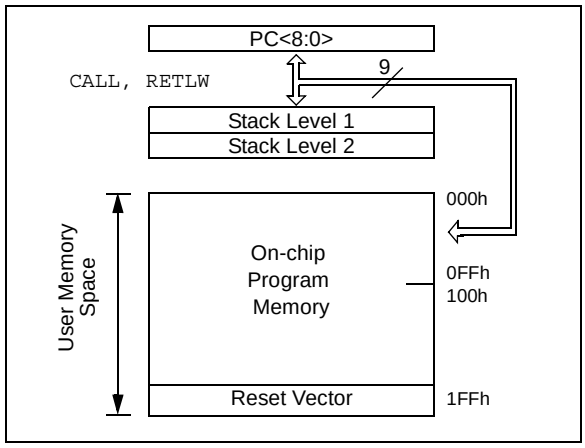


FIGURE 3-2: PIC16F57/PIC16F59 PROGRAM MEMORY MAP AND STACK

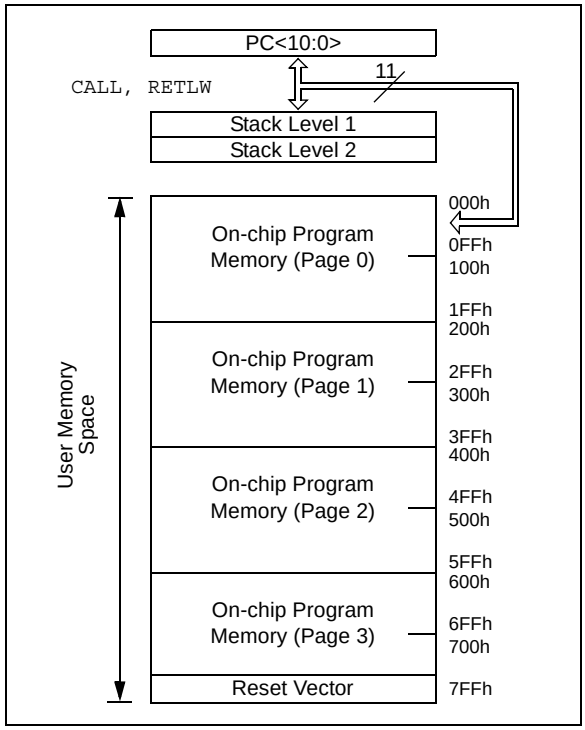
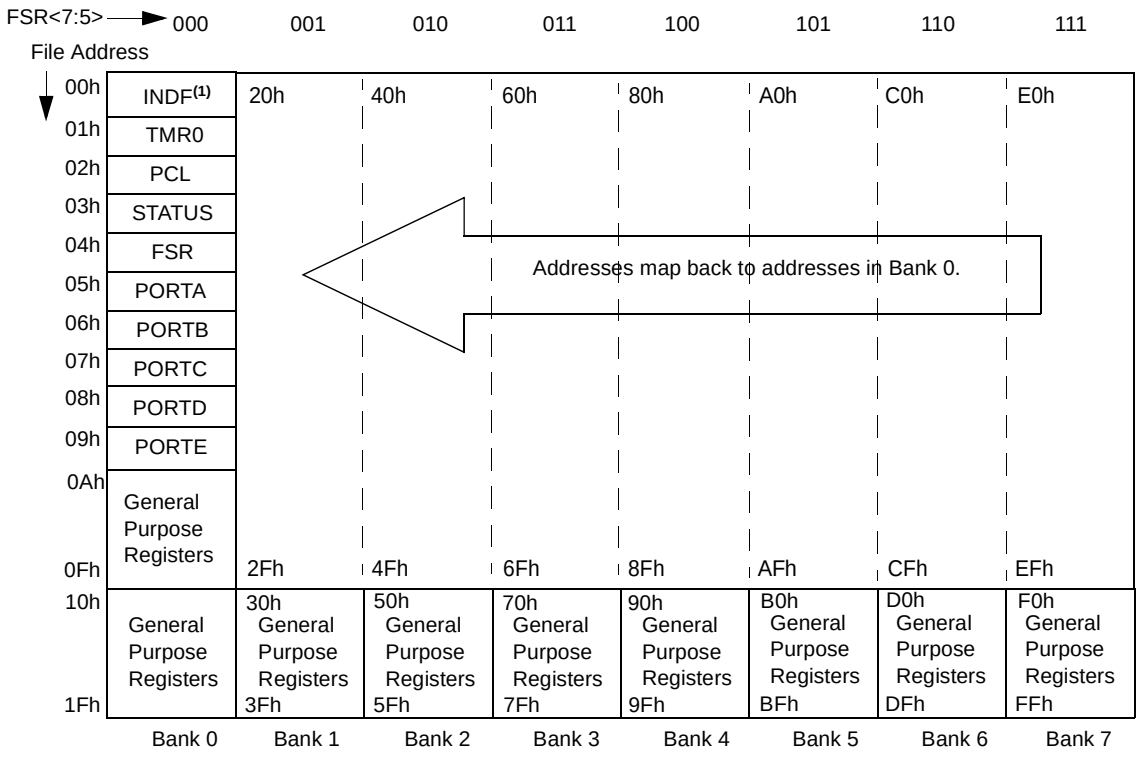


FIGURE 3-5: PIC16F59 REGISTER FILE MAP



Note 1: Not a physical register.

3.4 Option Register

The Option register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the Option register. A Reset sets the Option<5:0> bits.

REGISTER 3-2: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7-6 **Unimplemented**: Read as '0'

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 3-6 and Figure 3-7).

For the PIC16F57 and PIC16F59, a page number must be supplied as well. Bit 5 and bit 6 of the STATUS register provide page information to bit 9 and bit 10 of the PC (Figure 3-6 and Figure 3-7).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 3-6 and Figure 3-7).

Instructions where the PCL is the destination or modify PCL instructions, include MOVWF PCL, ADDWF PCL, and BSF PCL,5.

For the PIC16F57 and PIC16F59, a page number again must be supplied. Bit 5 and bit 6 of the STATUS register provide page information to bit 9 and bit 10 of the PC (Figure 3-6 and Figure 3-7).

Note:	Because PC<8> is cleared in the CALL instruction or any modified PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 3-6: LOADING OF PC BRANCH INSTRUCTIONS – PIC16F54

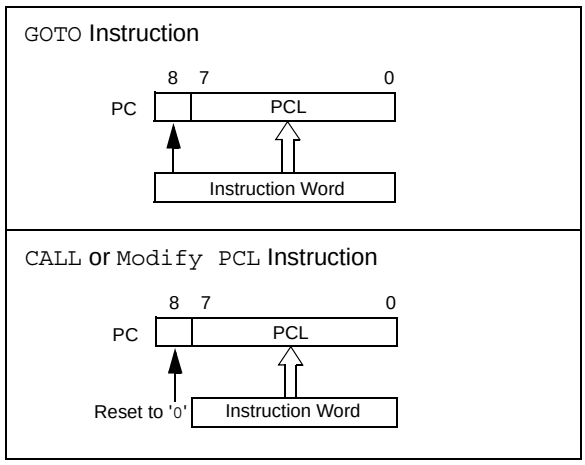
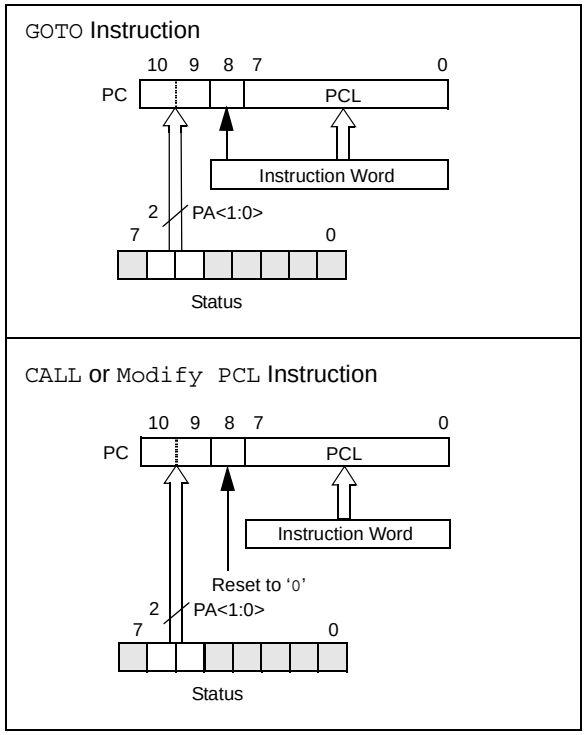


FIGURE 3-7: LOADING OF PC BRANCH INSTRUCTIONS – PIC16F57 AND PIC16F59



3.5.1 PAGING CONSIDERATIONS PIC16F57 AND PIC16F59

If the PC is pointing to the last address of a selected memory page, when it increments, it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS register will not be updated. Therefore, the next GOTO, CALL or MODIFY PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

3.5.2 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in the last page (i.e., the Reset vector).

The STATUS register page preselect bits are cleared upon a Reset, which means that page 0 is preselected.

Therefore, upon a Reset, a GOTO instruction at the Reset vector location will automatically cause the program to jump to page 0.

4.3 External Crystal Oscillator Circuit

Either a pre-packaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Pre-packaged oscillators provide a wide operating range and better stability. A well designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance or one with series resonance.

Figure 4-3 shows an implementation example of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 4-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)

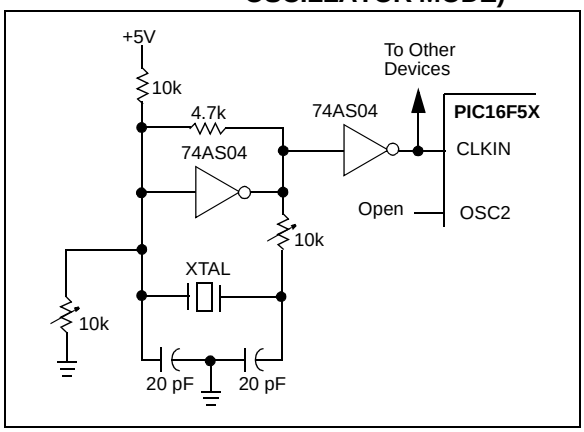
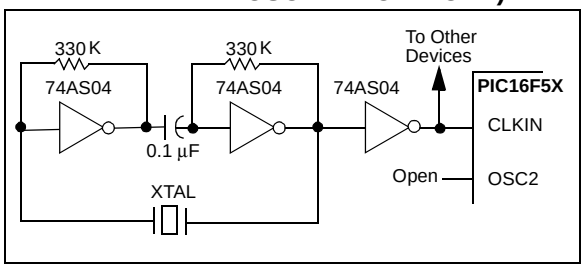


Figure 4-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverters perform a 360° phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 4-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



4.4 RC Oscillator

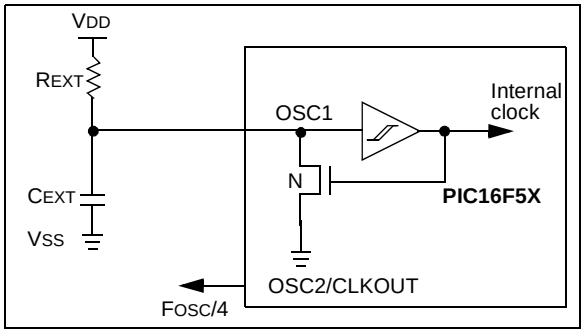
For applications where precise timing is not a requirement, the RC oscillator option is available. The operation and functionality of the RC oscillator is dependent upon a number of variables. The RC oscillator frequency is a function of:

- Supply voltage
- Resistor (REXT) and capacitor (CEXT) values
- Operating temperature.

The oscillator frequency will vary from unit to unit due to normal process parameter variation. The difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to account for the tolerance of the external R and C components. Figure 4-5 shows how the R/C combination is connected.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin and can be used for test purposes or to synchronize other logic.

FIGURE 4-5: RC OSCILLATOR MODE



5.0 RESET

The PIC16F5X devices may be reset in one of the following ways:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset (normal operation)
- $\overline{\text{MCLR}}$ Wake-up Reset (from Sleep)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from Sleep)

Table 5-1 shows these Reset conditions for the PCL and STATUS registers.

Some registers are not affected in any Reset condition. Their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on Power-on Reset (POR), $\overline{\text{MCLR}}$ or WDT Reset. A $\overline{\text{MCLR}}$ or WDT wake-up from Sleep also results in a device Reset and not a continuation of operation before Sleep.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different Reset conditions (Table 5-1). These bits may be used to determine the nature of the Reset.

Table 5-3 lists a full description of Reset states of all registers. Figure 5-1 shows a simplified block diagram of the on-chip Reset circuit.

TABLE 5-1: STATUS BITS AND THEIR SIGNIFICANCE

Condition	$\overline{\text{TO}}$	$\overline{\text{PD}}$
Power-on Reset	1	1
$\overline{\text{MCLR}}$ Reset (normal operation)	u	u
$\overline{\text{MCLR}}$ Wake-up (from Sleep)	1	0
WDT Reset (normal operation)	0	1
WDT Wake-up (from Sleep)	0	0

Legend: u = unchanged, x = unknown, — = unimplemented read as '0'.

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH RESET

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on $\overline{\text{MCLR}}$ and WDT Reset
03h	STATUS	PA2	PA1	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, q = see Table 5-1 for possible values.

7.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on-the-fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

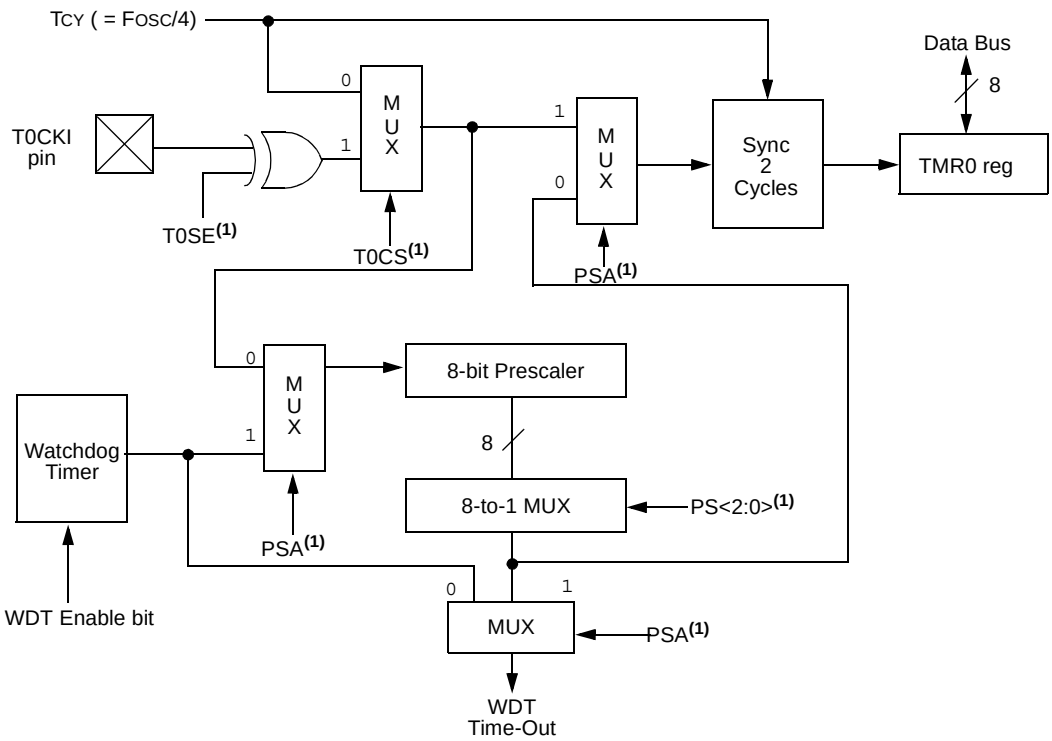
```
CLRWDT                ;Clear WDT
CLRF    TMR0          ;Clear TMR0 &  ;Prescaler
MOVLW   B'00xx1111'   ;Last 3 instructions
                      ;in this example
OPTION                ;are required only if
                      ;desired
CLRWDT                ;PS<2:0> are 000 or 001
MOVLW   B'00xx1xxx'   ;Set Prescaler to
OPTION                ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

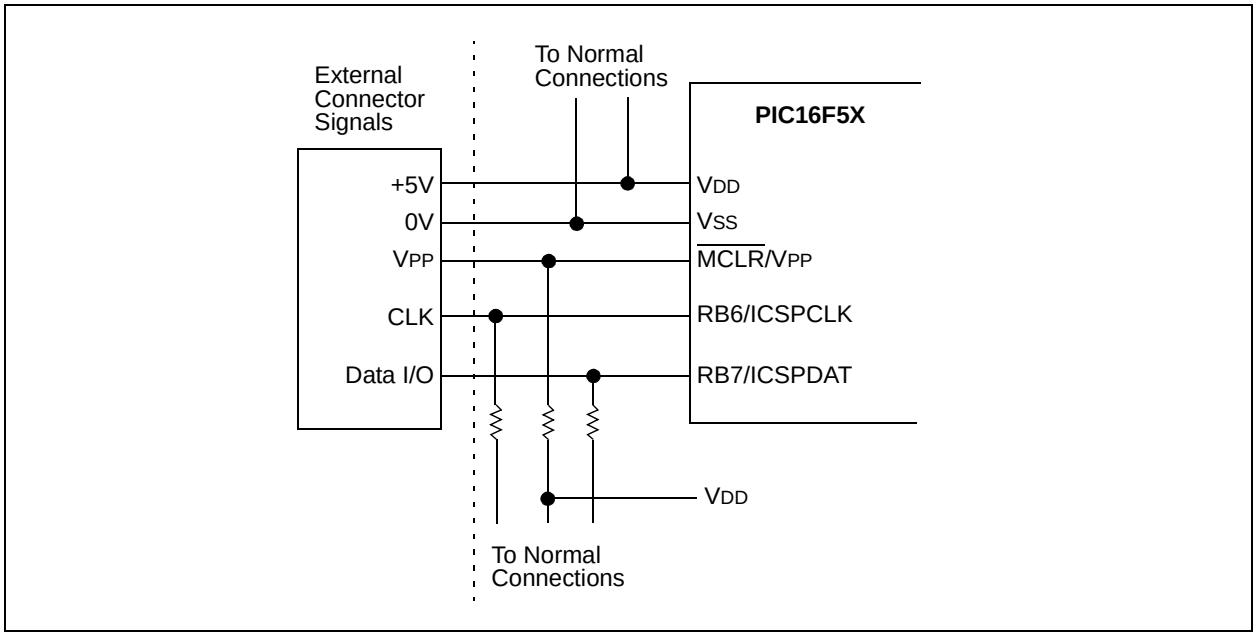
```
CLRWDT                ;Clear WDT and
                      ;prescaler
MOVLW   B'xxxx0xxx'   ;Select TMR0, new
                      ;prescale value and
                      ;clock source
OPTION
```

FIGURE 7-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA PS<2:0> are bits in the Option register.

FIGURE 8-1: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING™ CONNECTION



11.0 ELECTRICAL SPECIFICATIONS FOR PIC16F54/57

Absolute Maximum Ratings(†)

Ambient Temperature under bias ..... -40°C to +125°C

Storage Temperature ..... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0V to +6.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS}(1) ..... 0V to +13.5V

Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)

Total power dissipation(2) ..... 800 mW

Max. current out of V_{SS} pin ..... 150 mA

Max. current into V_{DD} pin ..... 100 mA

Max. current into an input pin (T0CKI only) ..... ±500 µA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 25 mA

Max. output current sourced by a single I/O port (PORTA, B or C) ..... 50 mA

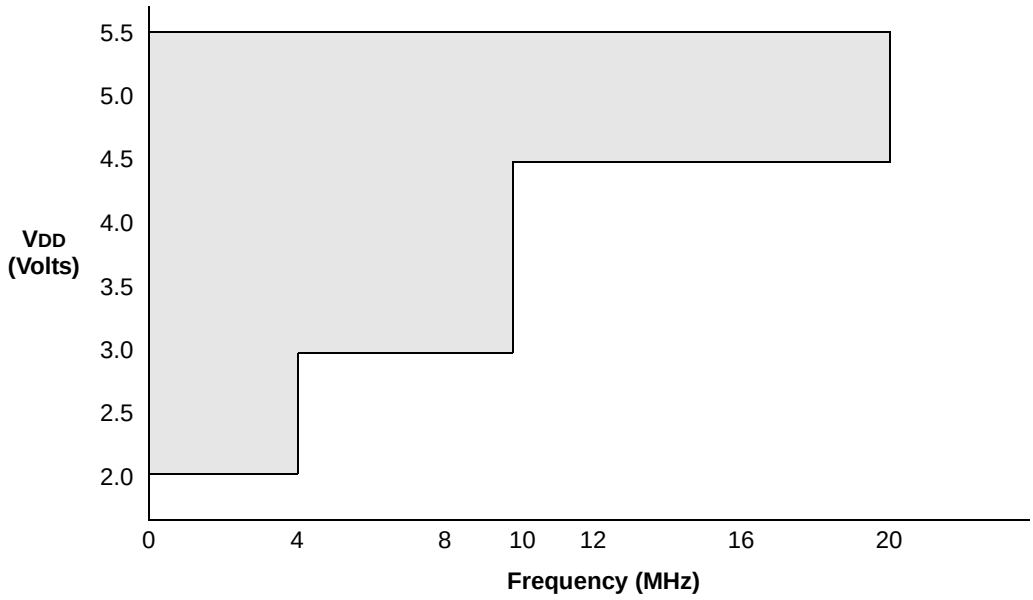
Max. output current sunk by a single I/O port (PORTA, B or C) ..... 50 mA

Note 1: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

2: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

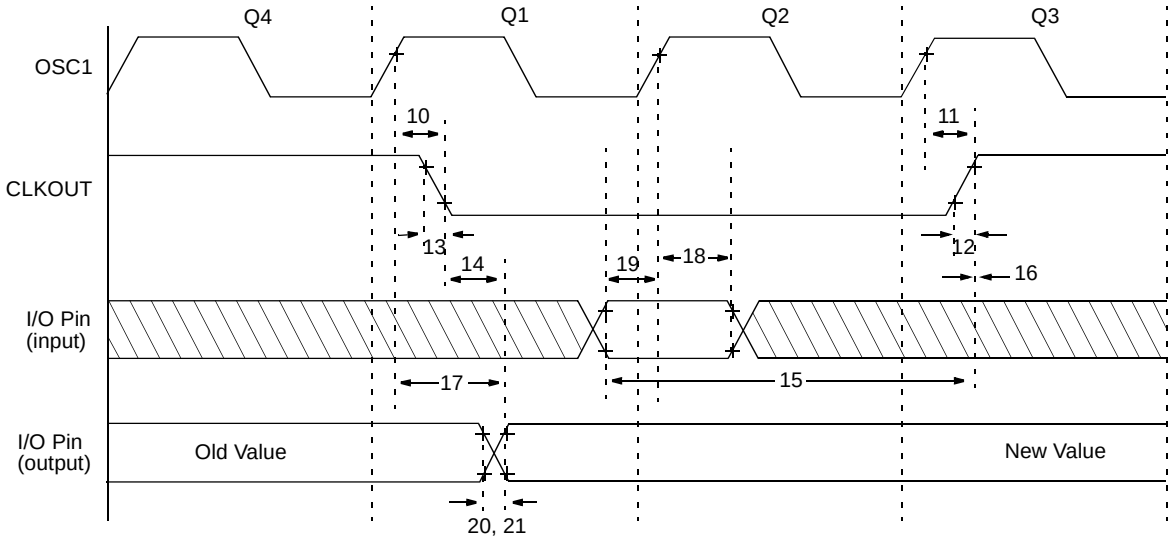
†NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 11-1: PIC16F5X VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 11-4: CLKOUT AND I/O TIMING – PIC16F5X



Note: Please refer to Figure 11-2 for load conditions.

TABLE 11-2: CLKOUT AND I/O TIMING REQUIREMENTS – PIC16F5X

Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ **(1)**	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ **(1)**	—	15	30**	ns
12	TckR	CLKOUT rise time **(1)**	—	5.0	15**	ns
13	TckF	CLKOUT fall time **(1)**	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid **(1)**	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ **(1)**	0.25 Tcy+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ **(1)**	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid **(2)**	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time **(2, 3)**	—	10	25**	ns
20	TioR	Port output rise time **(2, 4)**	—	10	50**	ns
21	TioF	Port output fall time **(2, 3)**	—	10	25**	ns
21	TioF	Port output fall time **(2, 4)**	—	10	50**	ns

Legend: TBD = To Be Determined.

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 11-2 for load conditions.

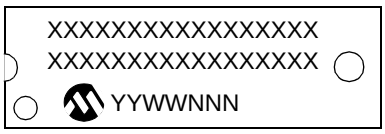
3: PIC16F54/57 only.

4: PIC16F59 only.

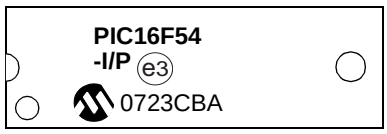
12.0 PACKAGING INFORMATION

12.1 Package Marketing Information

18-Lead PDIP



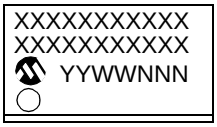
Example



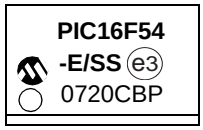
18-Lead SOIC

Example

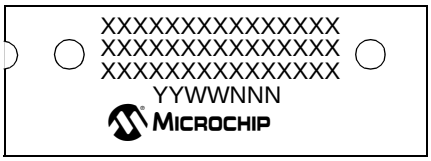
20-Lead SSOP



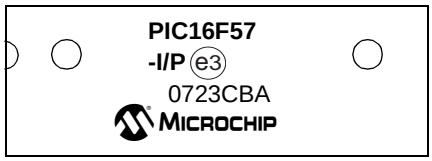
Example



28-Lead PDIP



Example



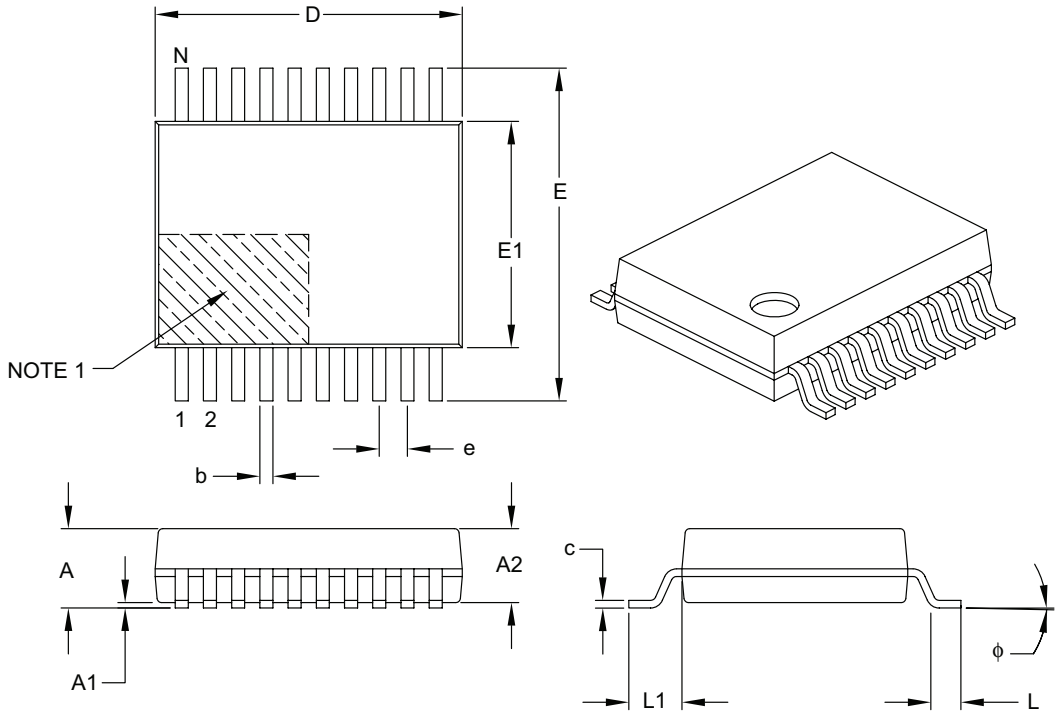
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

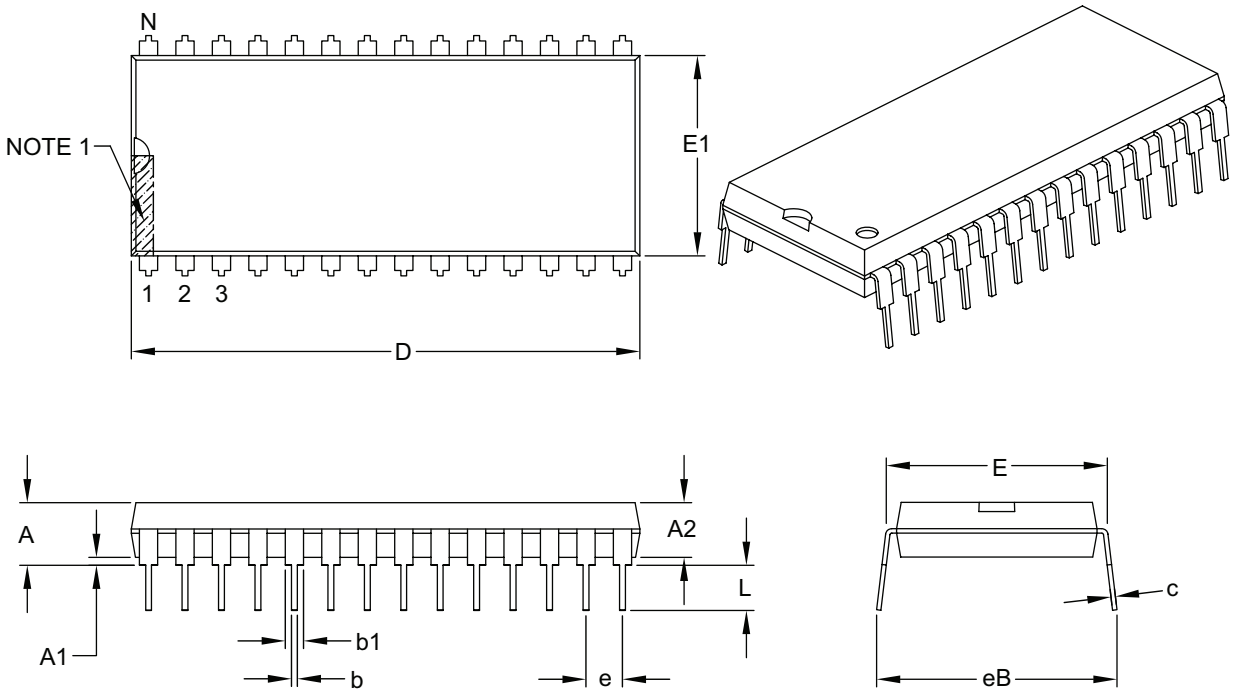
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

28-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.380	–	1.565
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.022
Overall Row Spacing §	eB	–	–	.700

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-079B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16F54	– VDD range 2.0V to 5.5V
	PIC16F54T(1)	– VDD range 2.0V to 5.5V
	PIC16F57	– VDD range 2.0V to 5.5V
	PIC16F57T(1)	– VDD range 2.0V to 5.5V
Temperature Range	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package	SO	= SOIC
	SS	= SSOP
	P	= PDIP
	SP	= Skinny Plastic DIP (SPDIP)(2)
	SOG	= SOIC (Pb-free)
	SSG	= SOIC (Pb-free)
	PG	= SOIC (Pb-free)
	SPG	= SOIC (Pb-free)
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F54–I/P = Industrial temp, PDIP package
b) PIC16F54T–I/SSG = Industrial temp, SSOP package (Pb -free), tape and reel
c) PIC16F57–E/SP6 = Extended temp, Skinny Plastic DIP package (Pb-free)
d) PIC16F57T–E/SS = Extended temp, SSOP package, tape and reel
e) PIC16F54–I/SOG = Industrial temp, SOIC package (Pb-free)

Note 1: T = in tape and reel SOIC and SSOP packages only.
2: PIC16F57 only

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16F59	– VDD range 2.0V to 5.5V
	PIC16F59T(1)	– VDD range 2.0V to 5.5V
Temperature Range	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package	P	= PDIP
	PT	= TQFP
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F59–I/P = Industrial temp, PDIP package (Pb-free).
b) PIC16F59T–I/PT = Industrial temp, TQFP package (Pb-free), tape and reel.

Note 1: T = in tape and reel TQFP packages only.