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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb210-i-pt

PIC24FJ256GB210 FAMILY

2.4 Voltage Regulator Pins (ENVREG and VCAP)

Note: This section applies only to PIC24FJ devices with an on-chip voltage regulator.

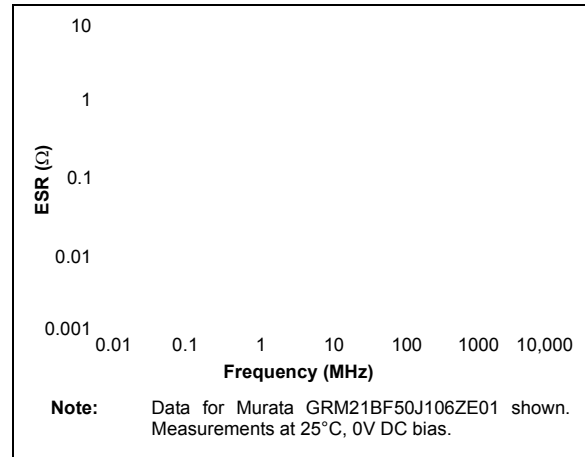
The on-chip voltage regulator enable pin (ENVREG) must always be connected directly to a supply voltage.

Refer to **Section 26.2 “On-Chip Voltage Regulator”** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR (<5Ω) capacitor is required on the VCAP pin to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must use a capacitor of 10 μF connected to ground. The type can be ceramic or tantalum. A suitable example is the Murata GRM21BF50J106ZE01 (10 μF, 6.3V) or equivalent. Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 “Electrical Characteristics”** for additional information.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 27.0 “Development Support”**.

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4.0 MEMORY ORGANIZATION

As Harvard architecture devices, PIC24F micro-controllers feature separate program and data memory spaces and busses. This architecture also allows direct access of program memory from the data space during code execution.

4.1 Program Memory Space

The program address memory space of the PIC24FJ256GB210 family devices is 4M instructions. The space is addressable by a 24-bit value derived

from either the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping, as described in **Section 4.3 “Interfacing Program and Data Memory Spaces”**.

User access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFFh). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for the PIC24FJ256GB210 family of devices are shown in Figure 4-1.

FIGURE 4-1: PROGRAM SPACE MEMORY MAP FOR PIC24FJ256GB210 FAMILY DEVICES

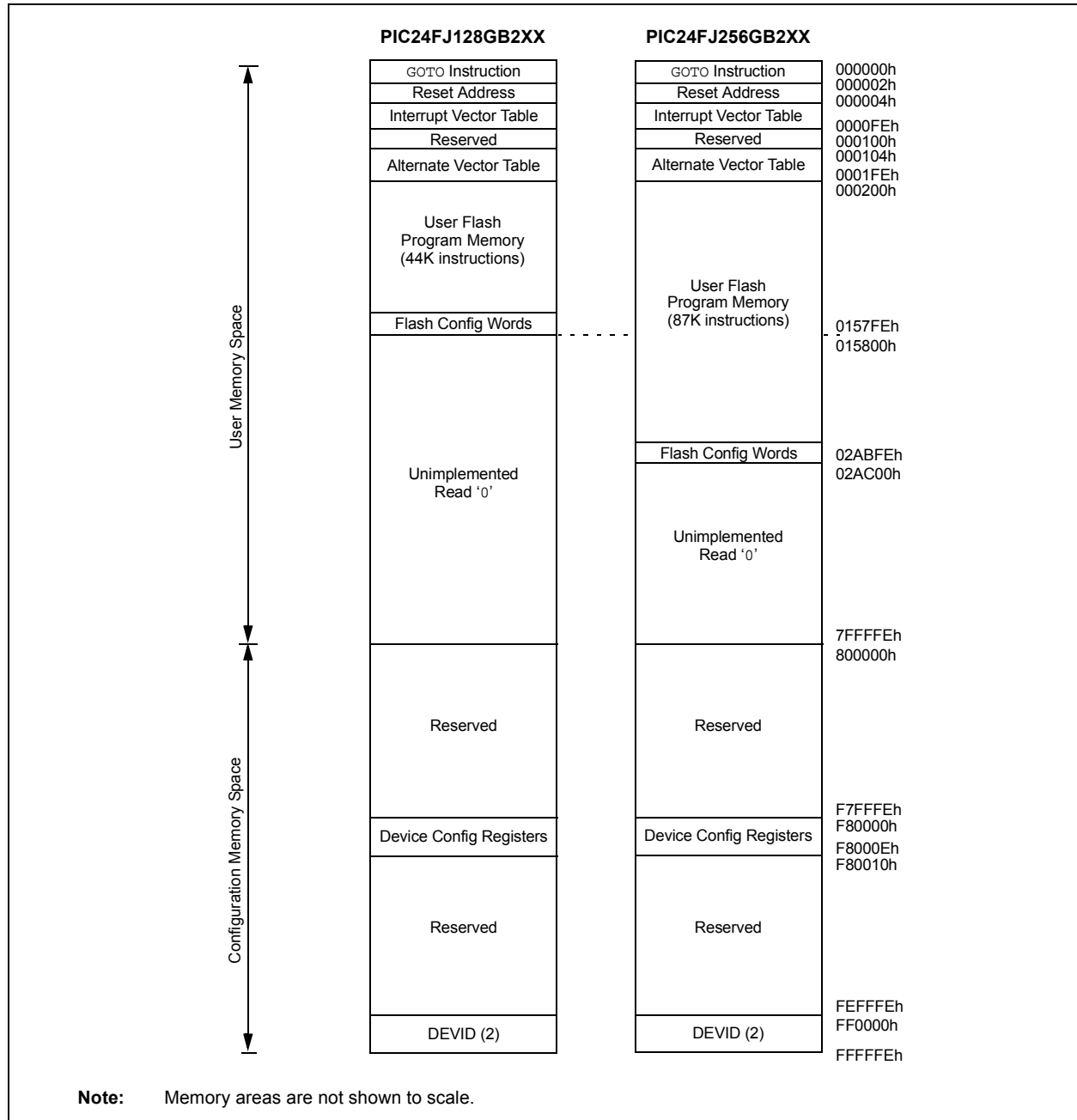


TABLE 4-26: ENHANCED PARALLEL MASTER/SLAVE PORT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON1	0600	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0	CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0	0000
PMCON2	0602	BUSY	—	ERROR	TIMEOUT	r	r	r	r	RADDR23	RADDR22	RADDR21	RADDR20	RADDR19	RADDR18	RADDR17	RADDR16	0000
PMCON3	0604	PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE	—	PTEN22 ⁽¹⁾	PTEN21 ⁽¹⁾	PTEN20 ⁽¹⁾	PTEN19 ⁽¹⁾	PTEN18 ⁽¹⁾	PTEN17 ⁽¹⁾	PTEN16 ⁽¹⁾	0000
PMCON4	0606	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000
PMCS1CF	0608	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS1BS	060A	BASE23	BASE22	BASE21	BASE20	BASE19	BASE18	BASE17	BASE16	BASE15	—	—	—	BASE11	—	—	—	0200
PMCS1MD	060C	ACKM1	ACKM0	r	r	r	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMCS2CF	060E	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS2BS	0610	BASE23	BASE22	BASE21	BASE20	BASE19	BASE18	BASE17	BASE16	BASE15	—	—	—	BASE11	—	—	—	0600
PMCS2MD	0612	ACKM1	ACKM0	r	r	r	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMDOUT1	0614	EPMP Data Out Register 1<15:8>									EPMP Data Out Register 1<7:0>							xxxx
PMDOUT2	0616	EPMP Data Out Register 2<15:8>									EPMP Data Out Register 2<7:0>							xxxx
PMDIN1	0618	EPMP Data In Register 1<15:8>									EPMP Data In Register 1<7:0>							xxxx
PMDIN2	061A	EPMP Data In Register 2<15:8>									EPMP Data In Register 2<7:0>							xxxx
PMSTAT	061C	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: — = unimplemented, read as '0', r = Reserved. Reset values are shown in hexadecimal.

Note 1: Unimplemented in 64-pin devices, read as '0'.

TABLE 4-27: REAL-TIME CLOCK AND CALENDAR REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	0620	Alarm Value Register Window Based on ALRMPTR<1:0>																xxxx
ALCFGRPT	0622	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000
RTCVAL	0624	RTCC Value Register Window Based on RTCPTR<1:0>																xxxx
RCFGCAL	0626	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOC	RTCPTR1	RTCPTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	(Note 1)

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The status of the RCFGAL register on POR is '0000' and on other Resets is unchanged.

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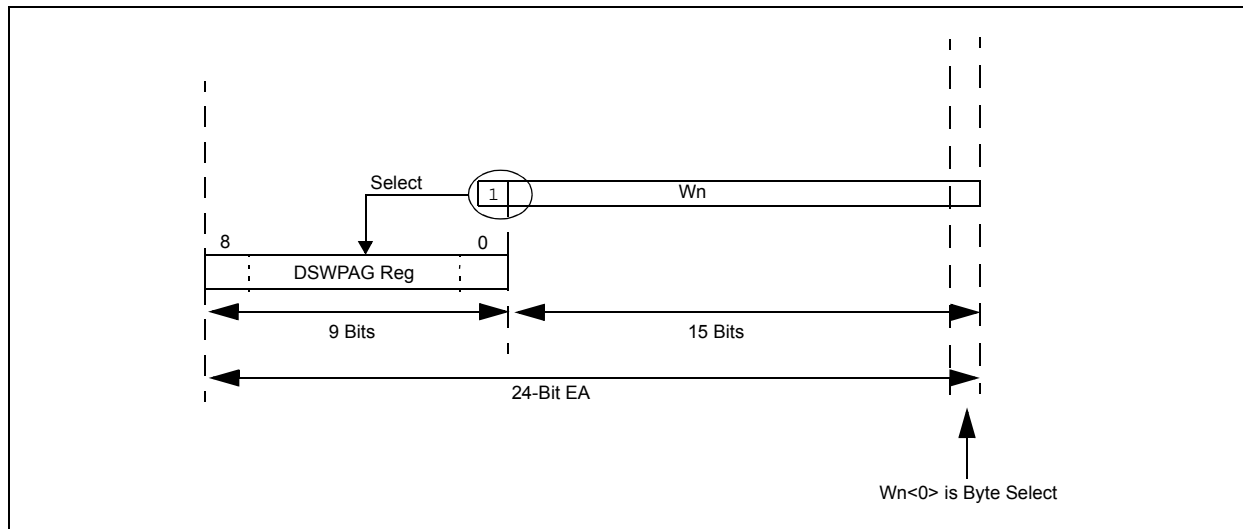
4.2.5.2 Data Write into EDS Space

In order to write data to EDS space, such as in EDS reads, an Address Pointer is set up by loading the required EDS page number into the DSWPAG register and assigning the offset address to one of the W registers. Once the above assignment is done, then the

EDS window is enabled by setting bit 15 of the working register, assigned with the offset address, and the accessed location can be written.

Figure 4-2 illustrates how the EDS space address is generated for write operations.

FIGURE 4-6: EDS ADDRESS GENERATION FOR WRITE OPERATIONS



When the MSb of EA is '1', the lower 9 bits of DSWPAG are concatenated to the lower 15 bits of EA to form a 24-bit EDS address for write operations. Example 4-2 shows how to write a byte, word and double-word to EDS.

EXAMPLE 4-2: EDS WRITE CODE IN ASSEMBLY

```
; Set the EDS page where the data to be written
mov    #0x0002 , w0
mov    w0 , DSWPAG    ;page 2 is selected for write
mov    #0x0800 , w1    ;select the location (0x800) to be written
bset   w1 , #15       ;set the MSB of the base address, enable EDS mode

;Write a byte to the selected location
mov    #0x00A5 , w2
mov    #0x003C , w3
mov.b  w2 , [w1++]    ;write Low byte
mov.b  w3 , [w1++]    ;write High byte

;Write a word to the selected location
mov    #0x1234 , w2 ;
mov    w2 , [w1] ;

;Write a Double - word to the selected location
mov    #0x1122 , w2
mov    #0x4455 , w3
mov.d  w2 , [w1] ;2 EDS writes
```

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6.1 Special Function Register Reset States

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of four registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the FNOSC bits in Flash Configuration Word 2 (CW2) (see Table 6-2). The RCFGAL and NVMCON registers are only affected by a POR.

6.2 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 6-3. Note that the system Reset signal, SYSRST, is released after the POR delay time expires.

The time at which the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable SYSRST delay times.

The Fail-Safe Clock Monitor (FSCM) delay determines the time at which the FSCM begins to monitor the system clock source after the SYSRST signal is released.

6.3 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen, as shown in Table 6-2. If clock switching is disabled, the system clock source is always selected according to the oscillator Configuration bits. Refer to Section 8.0 “Oscillator Configuration” for further details.

TABLE 6-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant
POR	FNOSC Configuration bits (CW2<10:8>)
BOR	
$\overline{\text{MCLR}}$	COSC Control bits (OSCCON<14:12>)
WDTO	
SWR	

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TABLE 6-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Reset Type	Clock Source	<u>SYSRST</u> Delay	System Clock Delay	Notes
POR ⁽⁷⁾	EC	TPOR + TSTARTUP + TRST	—	1, 2, 3
	ECPLL	TPOR + TSTARTUP + TRST	TLOCK	1, 2, 3, 5
	XT, HS, SOSC	TPOR + TSTARTUP + TRST	TOST	1, 2, 3, 4
	XTPLL, HSPLL	TPOR + TSTARTUP + TRST	TOST + TLOCK	1, 2, 3, 4, 5
	FRC, FRCDIV	TPOR + TSTARTUP + TRST	TFRC	1, 2, 3, 6, 7
	FRCPLL	TPOR + TSTARTUP + TRST	TFRC + TLOCK	1, 2, 3, 5, 6
	LPRC	TPOR + TSTARTUP + TRST	TLPRC	1, 2, 3, 6
BOR	EC	TSTARTUP + TRST	—	2, 3
	ECPLL	TSTARTUP + TRST	TLOCK	2, 3, 5
	XT, HS, SOSC	TSTARTUP + TRST	TOST	2, 3, 4
	XTPLL, HSPLL	TSTARTUP + TRST	TOST + TLOCK	2, 3, 4, 5
	FRC, FRCDIV	TSTARTUP + TRST	TFRC	2, 3, 6, 7
	FRCPLL	TSTARTUP + TRST	TFRC + TLOCK	2, 3, 5, 6
	LPRC	TSTARTUP + TRST	TLPRC	2, 3, 6
MCLR	Any Clock	TRST	—	3
WDT	Any Clock	TRST	—	3
Software	Any clock	TRST	—	3
Illegal Opcode	Any Clock	TRST	—	3
Uninitialized W	Any Clock	TRST	—	3
Trap Conflict	Any Clock	TRST	—	3

Note 1: TPOR = Power-on Reset delay (10 μs nominal).

2: TSTARTUP = TVREG (10 μs nominal when VREGS = 1 and when VREGS = 0; depends upon WUTSEL<1:0> bits setting).

3: TRST = Internal State Reset time (32 μs nominal).

4: TOST = Oscillator Start-up Timer. A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

5: TLOCK = PLL lock time.

6: TFRC and TLPRC = RC Oscillator start-up times.

7: If Two-speed Start-up is enabled, regardless of the primary oscillator selected, the device starts with FRC so the system clock delay is just TFRC, and in such cases, FRC start-up time is valid. It switches to the primary oscillator after its respective clock delay.

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TABLE 7-2: IMPLEMENTED INTERRUPT VECTORS (CONTINUED)

Interrupt Source	Vector Number	IVT Address	AIVT Address	Interrupt Bit Locations		
				Flag	Enable	Priority
Timer1	3	00001Ah	00011Ah	IFS0<3>	IEC0<3>	IPC0<14:12>
Timer2	7	000022h	000122h	IFS0<7>	IEC0<7>	IPC1<14:12>
Timer3	8	000024h	000124h	IFS0<8>	IEC0<8>	IPC2<2:0>
Timer4	27	00004Ah	00014Ah	IFS1<11>	IEC1<11>	IPC6<14:12>
Timer5	28	00004Ch	00014Ch	IFS1<12>	IEC1<12>	IPC7<2:0>
UART1 Error	65	000096h	000196h	IFS4<1>	IEC4<1>	IPC16<6:4>
UART1 Receiver	11	00002Ah	00012Ah	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1 Transmitter	12	00002Ch	00012Ch	IFS0<12>	IEC0<12>	IPC3<2:0>
UART2 Error	66	000098h	000198h	IFS4<2>	IEC4<2>	IPC16<10:8>
UART2 Receiver	30	000050h	000150h	IFS1<14>	IEC1<14>	IPC7<10:8>
UART2 Transmitter	31	000052h	000152h	IFS1<15>	IEC1<15>	IPC7<14:12>
UART3 Error	81	0000B6h	0001B6h	IFS5<1>	IEC5<1>	IPC20<6:4>
UART3 Receiver	82	0000B8h	0001B8h	IFS5<2>	IEC5<2>	IPC20<10:8>
UART3 Transmitter	83	0000BAh	0001BAh	IFS5<3>	IEC5<3>	IPC20<14:12>
UART4 Error	87	0000C2h	0001C2h	IFS5<7>	IEC5<7>	IPC21<14:12>
UART4 Receiver	88	0000C4h	0001C4h	IFS5<8>	IEC5<8>	IPC22<2:0>
UART4 Transmitter	89	0000C6h	0001C6h	IFS5<9>	IEC5<9>	IPC22<6:4>
USB Interrupt	86	0000C0h	0001C0h	IFS5<6>	IEC5<6>	IPC21<10:8>

7.3 Interrupt Control and Status Registers

The PIC24FJ256GB210 family of devices implements a total of 37 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFS0 through IFS5
- IEC0 through IEC5
- IPC0 through IPC23 (except IPC14 and IPC17)
- INTTREG

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table (AIVT).

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or an external signal and is cleared via software.

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPCx registers are used to set the interrupt priority level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

The INTTREG register contains the associated interrupt vector number and the new CPU interrupt priority level, which are latched into the Vector Number (VECNUM<6:0>) and the Interrupt Priority Level (ILR<3:0>) bit fields in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the order of their vector numbers, as shown in Table 7-2. For example, the INT0 (External Interrupt 0) is shown as having a vector number and a natural order priority of 0. Thus, the INT0IF status bit is found in IFS0<0>, the INT0IE enable bit in IEC0<0> and the INT0IP<2:0> priority bits in the first position of IPC0 (IPC0<2:0>).

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. The ALU STATUS register (SR) contains the IPL<2:0> bits (SR<7:5>). These indicate the current CPU interrupt priority level. The user can change the current CPU priority level by writing to the IPL bits.

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8.5.3 CONSIDERATIONS FOR USB OPERATION

When using the USB On-The-Go module in PIC24FJ256GB210 family devices, users must always observe these rules in configuring the system clock:

- For USB operation, the selected clock source (EC, HS or XT) must meet the USB clock tolerance requirements.
- The Primary Oscillator/PLL modes are the only oscillator configurations that permit USB operation. There is no provision to provide a separate external clock source to the USB module.
- While the FRCPLL Oscillator mode is used for USB applications, users must always ensure that the FRC source is configured to provide a frequency of 4 MHz or 8 MHz (RCDIV<2:0> = 001 or 000) and that the USB PLL prescaler is configured appropriately.

All other oscillator modes are available; however, USB operation is not possible when these modes are selected. They may still be useful in cases where other power levels of operation are desirable and the USB module is not needed (e.g., the application is sleeping and waiting for a bus attachment).

8.6 Reference Clock Output

In addition to the CLKO output ($F_{osc}/2$) available in certain oscillator modes, the device clock in the PIC24FJ256GB210 family devices can also be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application.

This reference clock output is controlled by the REFOCON register (Register 8-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIV bits (REFOCON<11:8>) enable the selection of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON<13:12>) control the availability of the reference output during Sleep mode. The ROSEL bit determines if the oscillator on OSCI and OSCO, or the current system clock source, is used for the reference clock output. The ROSSLP bit determines if the reference source is available on REFO when the device is in Sleep mode.

To use the reference clock output in Sleep mode, both the ROSSLP and ROSEL bits must be set. The device clock must also be configured for one of the primary modes (EC, HS or XT); otherwise, if the POSCEN bit is not also set, the oscillator on OSCI and OSCO will be powered down when the device enters Sleep mode. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

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10.3 Input Change Notification

The input change notification function of the I/O ports allows the PIC24FJ256GB210 family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States, even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 84 external inputs that may be selected (enabled) for generating an interrupt request on a Change-of-State.

Registers, CNEN1 through CNEN6, contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin has a both a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source that is connected to the pin, while the pull-downs act as a current sink that is connected to the pin. These eliminate the need for external resistors

when push button or keypad devices are connected. The pull-ups and pull-downs are separately enabled using the CNPU1 through CNPU6 registers (for pull-ups), and the CNPD1 through CNPD6 registers (for pull-downs). Each CN pin has individual control bits for its pull-up and pull-down. Setting a control bit enables the weak pull-up or pull-down for the corresponding pin.

When the internal pull-up is selected, the pin pulls up to $V_{DD} - 1.1V$ (typical). When the internal pull-down is selected, the pin pulls down to V_{SS} .

Note: Pull-ups on change notification pins should always be disabled whenever the port pin is configured as a digital output.

Note: To use CN83 and CN84, which are on the D+ and D- pins, the UTRDIS bit (U1CNFG2<0>) should be set.

EXAMPLE 10-1: PORT WRITE/READ IN ASSEMBLY

```
MOV    0xFF00, W0    ; Configure PORTB<15:8> as inputs
MOV    W0, TRISB    ; and PORTB<7:0> as outputs
NOP                                ; Delay 1 cycle
BTSS   PORTB, #13   ; Next Instruction
```

EXAMPLE 10-2: PORT WRITE/READ IN 'C'

```
TRISB = 0xFF00;           //Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
Nop();                   //Delay 1 cycle
If (PORTBbits.RB13) { }; //Next Instruction
```

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REGISTER 10-26: RPINR27: PERIPHERAL PIN SELECT INPUT REGISTER 27

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U4CTSR5	U4CTSR4	U4CTSR3	U4CTSR2	U4CTSR1	U4CTSR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U4RXR5	U4RXR4	U4RXR3	U4RXR2	U4RXR1	U4RXR0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **U4CTSR<5:0>:** Assign UART4 Clear to Send (U4CTS) to the Corresponding RPn or RPIIn Pin bits
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **U4RXR<5:0>:** Assign UART4 Receive (U4RX) to the Corresponding RPn or RPIIn Pin bits

REGISTER 10-27: RPINR28: PERIPHERAL PIN SELECT INPUT REGISTER 28

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK3R5	SCK3R4	SCK3R3	SCK3R2	SCK3R1	SCK3R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI3R5	SDI3R4	SDI3R3	SDI3R2	SDI3R1	SDI3R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **SCK3R<5:0>:** Assign SPI3 Clock Input (SCK3IN) to the Corresponding RPn or RPIIn Pin bits
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **SDI3R<5:0>:** Assign SPI3 Data Input (SDI3) to the Corresponding RPn or RPIIn Pin bits

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REGISTER 10-31: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP5R5 ⁽¹⁾	RP5R4 ⁽¹⁾	RP5R3 ⁽¹⁾	RP5R2 ⁽¹⁾	RP5R1 ⁽¹⁾	RP5R0 ⁽¹⁾
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP4R5	RP4R4	RP4R3	RP4R2	RP4R1	RP4R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP5R<5:0>:** RP5 Output Pin Mapping bits⁽¹⁾
 Peripheral output number n is assigned to pin, RP5 (see Table 10-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP4R<5:0>:** RP4 Output Pin Mapping bits
 Peripheral output number n is assigned to pin, RP4 (see Table 10-4 for peripheral function numbers).

Note 1: Unimplemented in 64-pin devices; read as '0'.

REGISTER 10-32: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP7R5	RP7R4	RP7R3	RP7R2	RP7R1	RP7R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP6R5	RP6R4	RP6R3	RP6R2	RP6R1	RP6R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

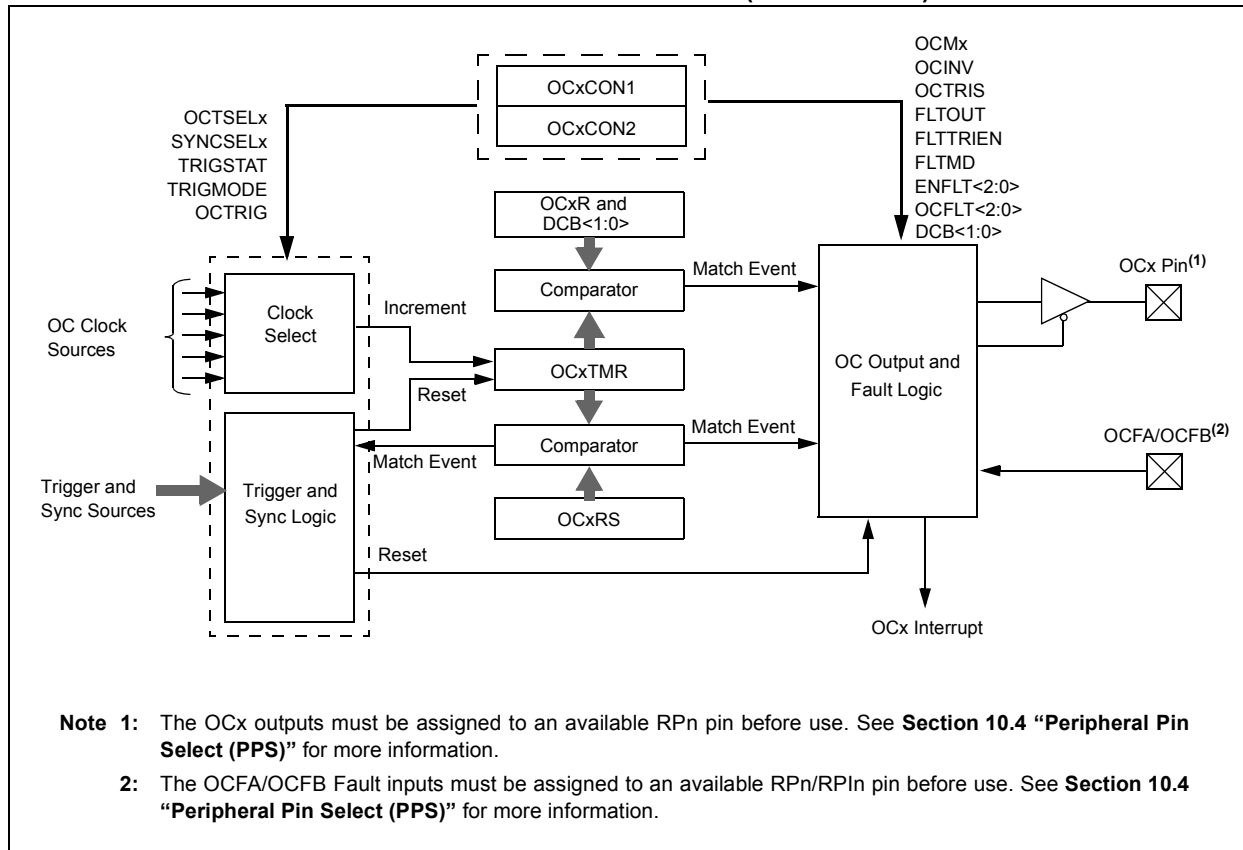
bit 13-8 **RP7R<5:0>:** RP7 Output Pin Mapping bits
 Peripheral output number n is assigned to pin, RP7 (see Table 10-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP6R<5:0>:** RP6 Output Pin Mapping bits
 Peripheral output number n is assigned to pin, RP6 (see Table 10-4 for peripheral function numbers).

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FIGURE 14-1: OUTPUT COMPARE BLOCK DIAGRAM (16-BIT MODE)



14.2 Compare Operations

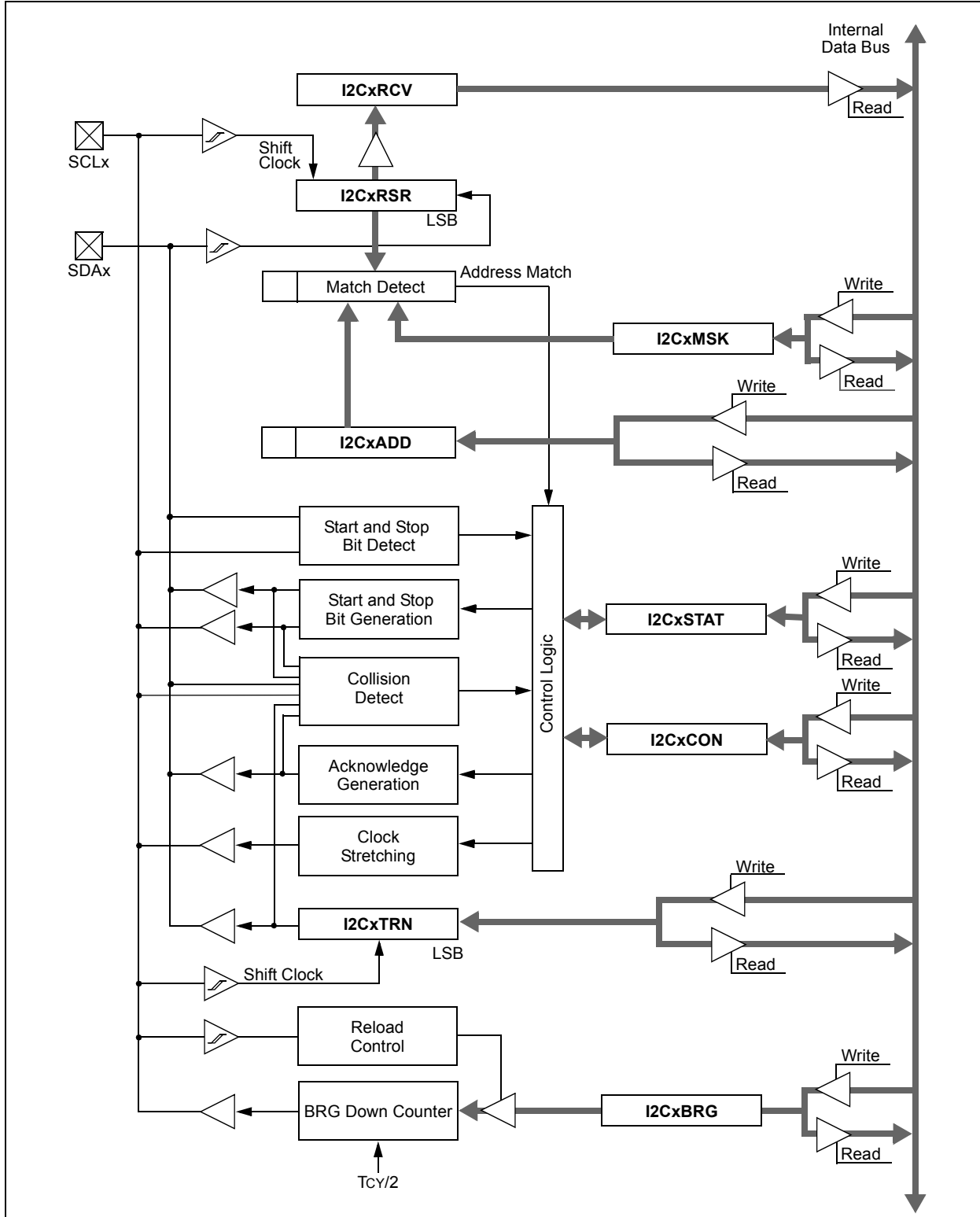
In Compare mode (Figure 14-1), the output compare module can be configured for single-shot or continuous pulse generation. It can also repeatedly toggle an output pin on each timer event.

To set up the module for compare operations:

1. Configure the OCx output for one of the available Peripheral Pin Select pins.
2. Calculate the required values for the OCxR and (for Double Compare modes) OCxRS Duty Cycle registers:
 - a) Determine the instruction clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
 - b) Calculate time to the rising edge of the output pulse relative to the timer start value (0000h).
 - c) Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
3. Write the rising edge value to OCxR and the falling edge value to OCxRS.
4. Set the Timer Period register, PRy, to a value equal to or greater than the value in OCxRS.
5. Set the OCM<2:0> bits for the appropriate compare operation (= 0xx).
6. For Trigger mode operations, set OCTRIG to enable Trigger mode. Set or clear TRIGMODE to configure trigger operation and TRIGSTAT to select a hardware or software trigger. For Synchronous mode, clear OCTRIG.
7. Set the SYNCSEL<4:0> bits to configure the trigger or synchronization source. If free-running timer operation is required, set the SYNCSEL bits to '00000' (no sync/trigger source).
8. Select the time base source with the OCTSEL<2:0> bits. If necessary, set the TON bits for the selected timer, which enables the compare time base to count. Synchronous mode operation starts as soon as the time base is enabled; Trigger mode operation starts after a trigger source event occurs.

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FIGURE 16-1: I²C™ BLOCK DIAGRAM



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REGISTER 18-4: U1OTGCON: USB ON-THE-GO CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DPPULUP	DMPULUP	DPPULDWN ⁽¹⁾	DMPULDWN ⁽¹⁾	VBUSON ⁽¹⁾	OTGEN ⁽¹⁾	VBUSCHG ⁽¹⁾	VBUSDIS ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **DPPULUP:** D+ Pull-up Enable bit
 1 = D+ data line pull-up resistor is enabled
 0 = D+ data line pull-up resistor is disabled
- bit 6 **DMPULUP:** D- Pull-up Enable bit
 1 = D- data line pull-up resistor is enabled
 0 = D- data line pull-up resistor is disabled
- bit 5 **DPPULDWN:** D+ Pull-Down Enable bit⁽¹⁾
 1 = D+ data line pull-down resistor is enabled
 0 = D+ data line pull-down resistor is disabled
- bit 4 **DMPULDWN:** D- Pull-Down Enable bit⁽¹⁾
 1 = D- data line pull-down resistor is enabled
 0 = D- data line pull-down resistor is disabled
- bit 3 **VBUSON:** VBUS Power-on bit⁽¹⁾
 1 = VBUS line is powered
 0 = VBUS line is not powered
- bit 2 **OTGEN:** OTG Features Enable bit⁽¹⁾
 1 = USB OTG is enabled; all D+/D- pull-up and pull-down bits are enabled
 0 = USB OTG is disabled; D+/D- pull-up and pull-down bits are controlled in hardware by the settings of the HOSTEN and USBEN (U1CON<3,0>) bits
- bit 1 **VBUSCHG:** VBUS Charge Select bit⁽¹⁾
 1 = VBUS line is set to charge to 3.3V
 0 = VBUS line is set to charge to 5V
- bit 0 **VBUSDIS:** VBUS Discharge Enable bit⁽¹⁾
 1 = VBUS line is discharged through a resistor
 0 = VBUS line is not discharged

Note 1: These bits are only used in Host mode; do not use in Device mode.

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TABLE 28-2: INSTRUCTION SET OVERVIEW

Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
ADD	ADD f	$f = f + WREG$	1	1	C, DC, N, OV, Z
	ADD f, WREG	$WREG = f + WREG$	1	1	C, DC, N, OV, Z
	ADD #lit10, Wn	$Wd = lit10 + Wd$	1	1	C, DC, N, OV, Z
	ADD Wb, Ws, Wd	$Wd = Wb + Ws$	1	1	C, DC, N, OV, Z
	ADD Wb, #lit5, Wd	$Wd = Wb + lit5$	1	1	C, DC, N, OV, Z
ADDC	ADDC f	$f = f + WREG + (C)$	1	1	C, DC, N, OV, Z
	ADDC f, WREG	$WREG = f + WREG + (C)$	1	1	C, DC, N, OV, Z
	ADDC #lit10, Wn	$Wd = lit10 + Wd + (C)$	1	1	C, DC, N, OV, Z
	ADDC Wb, Ws, Wd	$Wd = Wb + Ws + (C)$	1	1	C, DC, N, OV, Z
	ADDC Wb, #lit5, Wd	$Wd = Wb + lit5 + (C)$	1	1	C, DC, N, OV, Z
AND	AND f	$f = f .AND. WREG$	1	1	N, Z
	AND f, WREG	$WREG = f .AND. WREG$	1	1	N, Z
	AND #lit10, Wn	$Wd = lit10 .AND. Wd$	1	1	N, Z
	AND Wb, Ws, Wd	$Wd = Wb .AND. Ws$	1	1	N, Z
	AND Wb, #lit5, Wd	$Wd = Wb .AND. lit5$	1	1	N, Z
ASR	ASR f	f = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR f, WREG	WREG = Arithmetic Right Shift f	1	1	C, N, OV, Z
	ASR Ws, Wd	Wd = Arithmetic Right Shift Ws	1	1	C, N, OV, Z
	ASR Wb, Wns, Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N, Z
	ASR Wb, #lit5, Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N, Z
BCLR	BCLR f, #bit4	Bit Clear f	1	1	None
	BCLR Ws, #bit4	Bit Clear Ws	1	1	None
BRA	BRA C, Expr	Branch if Carry	1	1 (2)	None
	BRA GE, Expr	Branch if Greater than or Equal	1	1 (2)	None
	BRA GEU, Expr	Branch if Unsigned Greater than or Equal	1	1 (2)	None
	BRA GT, Expr	Branch if Greater than	1	1 (2)	None
	BRA GTU, Expr	Branch if Unsigned Greater than	1	1 (2)	None
	BRA LE, Expr	Branch if Less than or Equal	1	1 (2)	None
	BRA LEU, Expr	Branch if Unsigned Less than or Equal	1	1 (2)	None
	BRA LT, Expr	Branch if Less than	1	1 (2)	None
	BRA LTU, Expr	Branch if Unsigned Less than	1	1 (2)	None
	BRA N, Expr	Branch if Negative	1	1 (2)	None
	BRA NC, Expr	Branch if Not Carry	1	1 (2)	None
	BRA NN, Expr	Branch if Not Negative	1	1 (2)	None
	BRA NOV, Expr	Branch if Not Overflow	1	1 (2)	None
	BRA NZ, Expr	Branch if Not Zero	1	1 (2)	None
	BRA OV, Expr	Branch if Overflow	1	1 (2)	None
	BRA Expr	Branch Unconditionally	1	2	None
	BRA Z, Expr	Branch if Zero	1	1 (2)	None
BRA Wn	Computed Branch	1	2	None	
BSET	BSET f, #bit4	Bit Set f	1	1	None
	BSET Ws, #bit4	Bit Set Ws	1	1	None
BSW	BSW.C Ws, Wb	Write C bit to Ws<Wb>	1	1	None
	BSW.Z Ws, Wb	Write Z bit to Ws<Wb>	1	1	None
BTG	BTG f, #bit4	Bit Toggle f	1	1	None
	BTG Ws, #bit4	Bit Toggle Ws	1	1	None
BTSC	BTSC f, #bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
	BTSC Ws, #bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None

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FIGURE 29-4: CLKO AND I/O TIMING CHARACTERISTICS

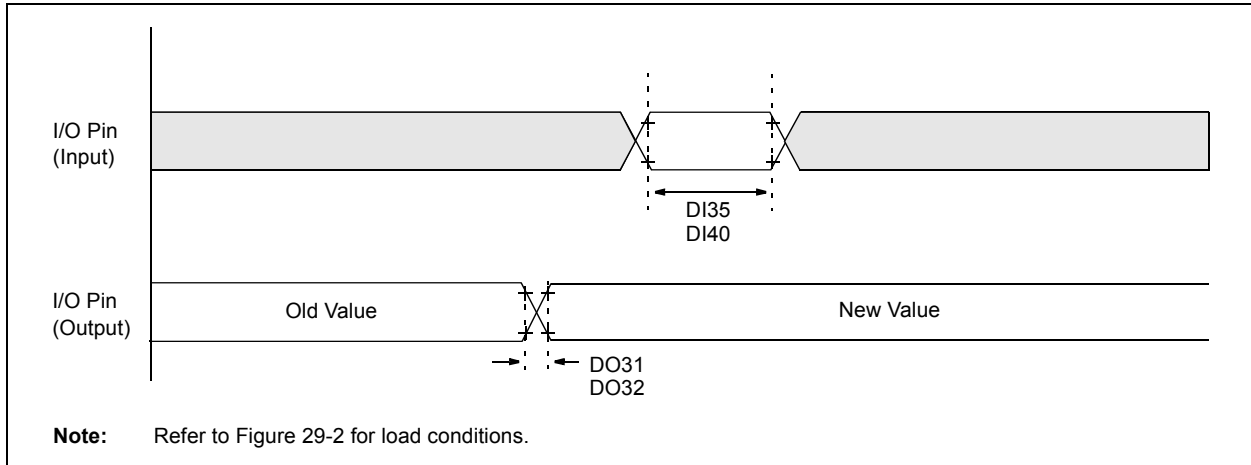


TABLE 29-18: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO31	TioR	Port Output Rise Time	—	10	25	ns	
DO32	TioF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	T _{CY}	

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.