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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb210t-i-bg

PIC24FJ256GB210 FAMILY

TABLE 1-3: PIC24FJ256GB210 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	64-Pin TQFP/QFN	100-Pin TQFP	121-Pin BGA			
RG0	—	90	A5	I/O	ST	PORTG Digital I/O.
RG1	—	89	E6	I/O	ST	
RG2	37	57	H10	I/O	ST	
RG3	36	56	J11	I/O	ST	
RG6	4	10	E3	I/O	ST	
RG7	5	11	F4	I/O	ST	
RG8	6	12	F2	I/O	ST	
RG9	8	14	F3	I/O	ST	
RG12	—	96	C3	I/O	ST	
RG13	—	97	A3	I/O	ST	
RG14	—	95	C4	I/O	ST	
RG15	—	1	B2	I/O	ST	
RP0	16	25	K2	I/O	ST	Remappable Peripheral (input or output).
RP1	15	24	K1	I/O	ST	
RP2	42	68	E9	I/O	ST	
RP3	44	70	D11	I/O	ST	
RP4	43	69	E10	I/O	ST	
RP5	—	48	K9	I/O	ST	
RP6	17	26	L1	I/O	ST	
RP7	18	27	J3	I/O	ST	
RP8	21	32	K4	I/O	ST	
RP9	22	33	L4	I/O	ST	
RP10	31	49	L10	I/O	ST	
RP11	46	72	D9	I/O	ST	
RP12	45	71	C11	I/O	ST	
RP13	14	23	J2	I/O	ST	
RP14	29	43	K7	I/O	ST	
RP15	—	53	J10	I/O	ST	
RP16	33	51	K10	I/O	ST	
RP17	32	50	L11	I/O	ST	
RP18	11	20	H1	I/O	ST	
RP19	6	12	F2	I/O	ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output

ST = Schmitt Trigger input buffer
I²C™ = I²C/SMBus input buffer

- Note** 1: The alternate EPMP pins are selected when the ALTPMP (CW3<12>) bit is programmed to '0'.
2: The PMSC2 signal will replace the PMA15 signal on the 15-pin PMA when CSF<1:0> = 01 or 10.
3: The PMCS1 signal will replace the PMA14 signal on the 14-pin PMA when CSF<1:0> = 10.
4: The alternate VREF pins selected when the ALTVREF (CW1<5>) bit is programmed to '0'.

PIC24FJ256GB210 FAMILY

The CORCON register contains the IPL3 bit, which, together with IPL<2:0>, indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

The interrupt controller has the Interrupt Controller Test register, INTTREG, which displays the status of the interrupt controller. When an interrupt request occurs, it's associated vector number and the new interrupt priority level are latched into INTTREG. This information can be used to determine a specific interrupt source if

a generic ISR is used for multiple vectors (such as when ISR remapping is used in bootloader applications) or to check if another interrupt is pending while in an ISR.

All interrupt registers are described in Register 7-1 through Register 7-38 in the succeeding pages.

REGISTER 7-1: SR: ALU STATUS REGISTER (IN CPU)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC
—	—	—	—	—	—	—	DC ⁽¹⁾
bit 15							bit 8

R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC
IPL2 ^(2,3)	IPL1 ^(2,3)	IPL0 ^(2,3)	RA ⁽¹⁾	N ⁽¹⁾	OV ⁽¹⁾	Z ⁽¹⁾	C ⁽¹⁾
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits^(2,3)

- 111 = CPU interrupt priority level is 7 (15); user interrupts are disabled
- 110 = CPU interrupt priority level is 6 (14)
- 101 = CPU interrupt priority level is 5 (13)
- 100 = CPU interrupt priority level is 4 (12)
- 011 = CPU interrupt priority level is 3 (11)
- 010 = CPU interrupt priority level is 2 (10)
- 001 = CPU interrupt priority level is 1 (9)
- 000 = CPU interrupt priority level is 0 (8)

Note 1: See Register 3-1 for the description of the remaining bits (bits 8, 4, 3, 2, 1 and 0) that are not dedicated to interrupt control functions.

2: The IPL bits are concatenated with the IPL3 (CORCON<3>) bit to form the CPU interrupt priority level. The value in parentheses indicates the interrupt priority level if IPL3 = 1.

3: The IPL Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

PIC24FJ256GB210 FAMILY

REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3

U-0	R/W-0, HS	U-0	U-0	U-0	U-0	U-0	U-0
—	RTCIF	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0, HS	R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
—	INT4IF	INT3IF	—	—	MI2C2IF	SI2C2IF	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14	RTCIF: Real-Time Clock/Calendar Interrupt Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 13-7	Unimplemented: Read as '0'
bit 6	INT4IF: External Interrupt 4 Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 5	INT3IF: External Interrupt 3 Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 4-3	Unimplemented: Read as '0'
bit 2	MI2C2IF: Master I2C2 Event Interrupt Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 1	SI2C2IF: Slave I2C2 Event Interrupt Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 0	Unimplemented: Read as '0'

PIC24FJ256GB210 FAMILY

REGISTER 7-29: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	MI2C2IP2	MI2C2IP1	MI2C2IP0
bit 15						bit 8	

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **MI2C2IP<2:0>:** Master I2C2 Event Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SI2C2IP<2:0>:** Slave I2C2 Event Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)

•

•

•

001 = Interrupt is priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

7.4 Interrupt Setup Procedures

7.4.1 INITIALIZATION

To configure an interrupt source:

1. Set the NSTDIS (INTCON1<15>) control bit if nested interrupts are not desired.
2. Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources may be programmed to the same non-zero value.

Note: At a device Reset, the IPCx registers are initialized, such that all user interrupt sources are assigned to Priority Level 4.

3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

7.4.2 INTERRUPT SERVICE ROUTINE (ISR)

The method that is used to declare an Interrupt Service Routine (ISR) and initialize the IVT with the correct vector address will depend on the programming language (i.e., 'C' or assembler) and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of the interrupt that the ISR handles. Otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a `RETFIE` instruction to unstack the saved PC value, SRL value and old CPU priority level.

7.4.3 TRAP SERVICE ROUTINE (TSR)

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

7.4.4 INTERRUPT DISABLE

All user interrupts can be disabled using the following procedure:

1. Push the current SR value onto the software stack using the `PUSH` instruction.
2. Force the CPU to Priority Level 7 by inclusive ORing the value 0Eh with SRL.

To enable user interrupts, the `POP` instruction may be used to restore the previous SR value.

Note that only user interrupts with a priority level of 7 or less can be disabled. Trap sources (Levels 8-15) cannot be disabled.

The `DISI` instruction provides a convenient way to disable interrupts of Priority Levels, 1-6, for a fixed period of time. Level 7 interrupt sources are not disabled by the `DISI` instruction.

PIC24FJ256GB210 FAMILY

REGISTER 8-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN	—	ROSSLP	ROSEL ⁽¹⁾	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ROEN:** Reference Oscillator Output Enable bit

1 = Reference oscillator is enabled on REFO pin

0 = Reference oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Output Stop in Sleep bit

1 = Reference oscillator continues to run in Sleep

0 = Reference oscillator is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit⁽¹⁾

1 = Primary oscillator is used as the base clock

0 = System clock is used as the base clock; base clock reflects any clock switching of the device

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divisor Select bits

1111 = Base clock value divided by 32,768

1110 = Base clock value divided by 16,384

1101 = Base clock value divided by 8,192

1100 = Base clock value divided by 4,096

1011 = Base clock value divided by 2,048

1010 = Base clock value divided by 1,024

1001 = Base clock value divided by 512

1000 = Base clock value divided by 256

0111 = Base clock value divided by 128

0110 = Base clock value divided by 64

0101 = Base clock value divided by 32

0100 = Base clock value divided by 16

0011 = Base clock value divided by 8

0010 = Base clock value divided by 4

0001 = Base clock value divided by 2

0000 = Base clock value

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Note that the crystal oscillator must be enabled using the FOSC<2:0> bits; the crystal maintains the operation in Sleep mode.

PIC24FJ256GB210 FAMILY

10.4.3.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains two 6-bit fields, with each field being associated with one RPN pin (see Register 10-29 through Register 10-44). The value of the bit field

corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 10-4).

Because of the mapping technique, the list of peripherals for output mapping also includes a null value of '000000'. This permits any given pin to remain disconnected from the output of any of the pin-selectable peripherals.

TABLE 10-4: SELECTABLE OUTPUT SOURCES (MAPS FUNCTION TO OUTPUT)

Output Function Number ⁽¹⁾	Function	Output Name
0	NULL ⁽²⁾	Null
1	C1OUT	Comparator 1 Output
2	C2OUT	Comparator 2 Output
3	U1TX	UART1 Transmit
4	$\overline{\text{U1RTS}}^{(3)}$	UART1 Request To Send
5	U2TX	UART2 Transmit
6	$\overline{\text{U2RTS}}^{(3)}$	UART2 Request To Send
7	SDO1	SPI1 Data Output
8	SCK1OUT	SPI1 Clock Output
9	SS1OUT	SPI1 Slave Select Output
10	SDO2	SPI2 Data Output
11	SCK2OUT	SPI2 Clock Output
12	SS2OUT	SPI2 Slave Select Output
18	OC1	Output Compare 1
19	OC2	Output Compare 2
20	OC3	Output Compare 3
21	OC4	Output Compare 4
22	OC5	Output Compare 5
23	OC6	Output Compare 6
24	OC7	Output Compare 7
25	OC8	Output Compare 8
28	U3TX	UART3 Transmit
29	$\overline{\text{U3RTS}}^{(3)}$	UART3 Request To Send
30	U4TX	UART4 Transmit
31	$\overline{\text{U4RTS}}^{(3)}$	UART4 Request To Send
32	SDO3	SPI3 Data Output
33	SCK3OUT	SPI3 Clock Output
34	SS3OUT	SPI3 Slave Select Output
35	OC9	Output Compare 9
36	C3OUT	Comparator 3 Output
37-63	(unused)	NC

- Note 1:** Setting the RPORx register with the listed value assigns that output function to the associated RPN pin.
Note 2: The NULL function is assigned to all RPN outputs at device Reset and disables the RPN output function.
Note 3: IrDA[®] BCLK functionality uses this output.

PIC24FJ256GB210 FAMILY

NOTES:

PIC24FJ256GB210 FAMILY

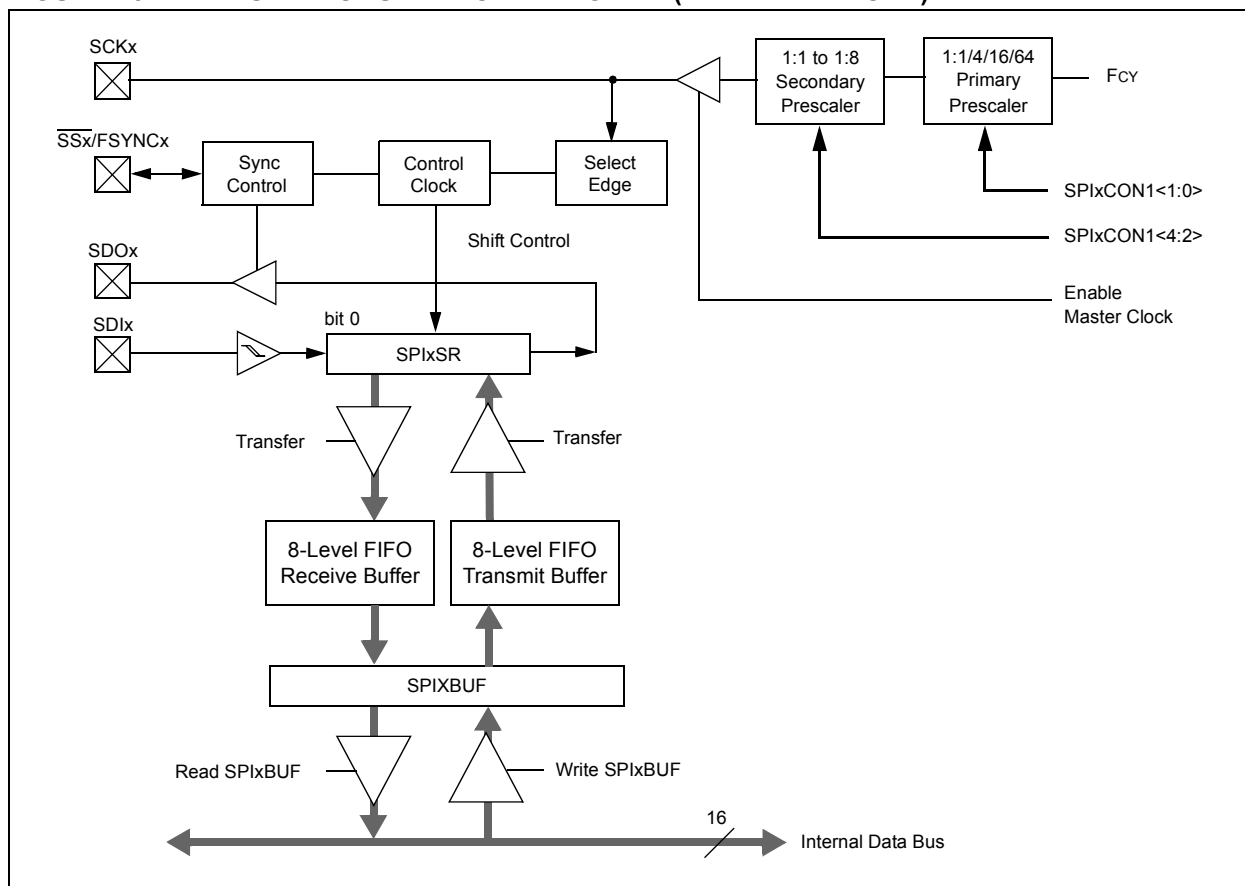
To set up the SPI module for the Enhanced Buffer Master mode of operation:

1. If using interrupts:
 - a) Clear the SPIxIF bit in the respective IFS register.
 - b) Set the SPIxIE bit in the respective IEC register.
 - c) Write the SPIxIP bits in the respective IPC register.
2. Write the desired settings to the SPIxCON1 and SPIxCON2 registers with MSTEN (SPIxCON1<5>) = 1.
3. Clear the SPIROV bit (SPIxSTAT<6>).
4. Select Enhanced Buffer mode by setting the SPIBEN bit (SPIxCON2<0>).
5. Enable SPI operation by setting the SPIEN bit (SPIxSTAT<15>).
6. Write the data to be transmitted to the SPIxBUF register. Transmission (and reception) will start as soon as data is written to the SPIxBUF register.

To set up the SPI module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPIxBUF register.
2. If using interrupts:
 - a) Clear the SPIxIF bit in the respective IFS register.
 - b) Set the SPIxIE bit in the respective IEC register.
 - c) Write the SPIxIP bits in the respective IPC register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1 and SPIxCON2 registers with MSTEN (SPIxCON1<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSx pin must be set, thus enabling the SSx pin.
6. Clear the SPIROV bit (SPIxSTAT<6>).
7. Select Enhanced Buffer mode by setting the SPIBEN bit (SPIxCON2<0>).
8. Enable SPI operation by setting the SPIEN bit (SPIxSTAT<15>).

FIGURE 15-2: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)



PIC24FJ256GB210 FAMILY

REGISTER 15-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	SPIFPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SPIFE	SPIBEN
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

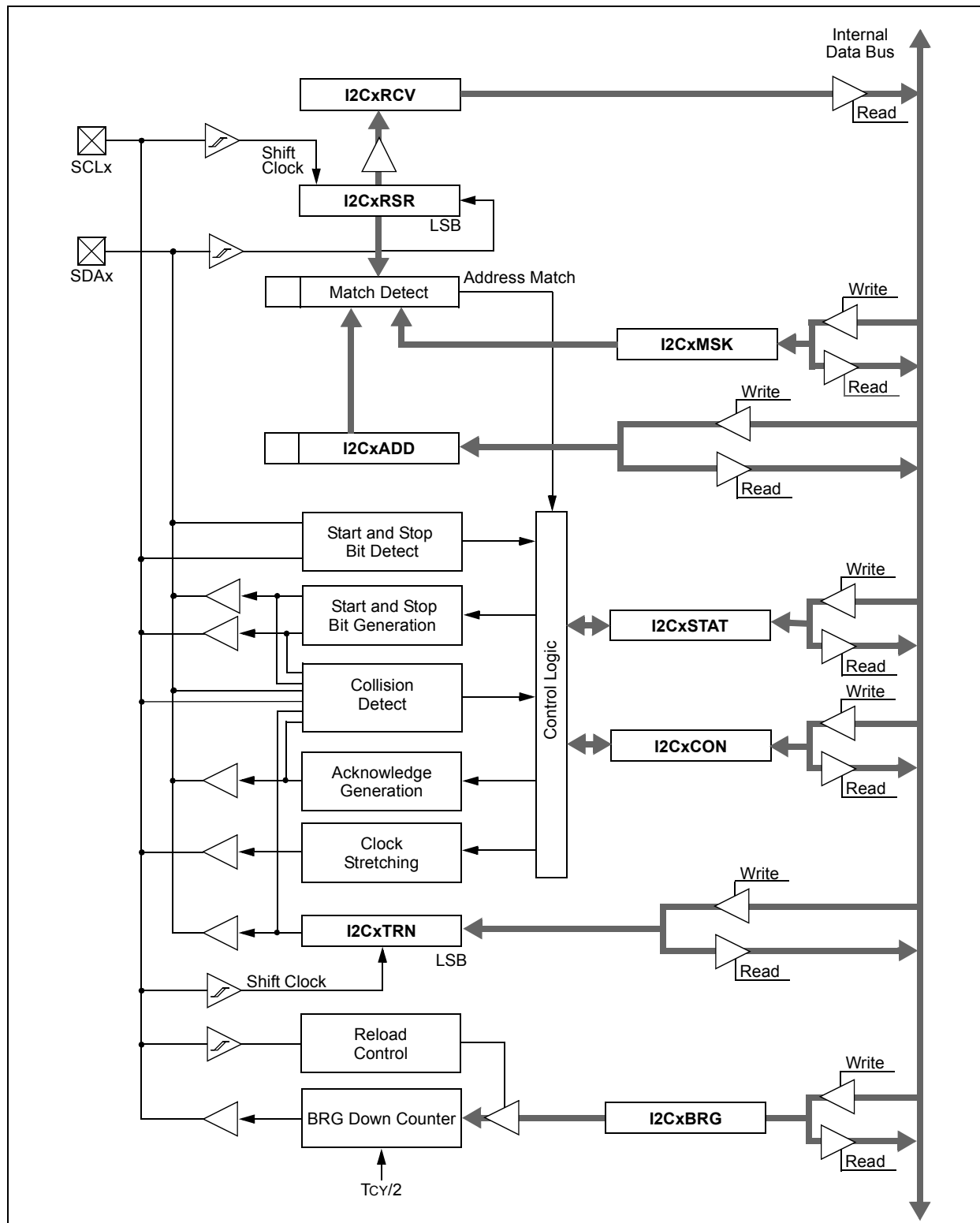
'0' = Bit is cleared

x = Bit is unknown

- bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled
0 = Framed SPIx support is disabled
- bit 14 **SPIFSD:** Frame Sync Pulse Direction Control on \overline{SSx} Pin bit
1 = Frame sync pulse input (slave)
0 = Frame sync pulse output (master)
- bit 13 **SPIFPOL:** Frame Sync Pulse Polarity bit (Frame mode only)
1 = Frame sync pulse is active-high
0 = Frame sync pulse is active-low
- bit 12-2 **Unimplemented:** Read as '0'
- bit 1 **SPIFE:** Frame Sync Pulse Edge Select bit
1 = Frame sync pulse coincides with the first bit clock
0 = Frame sync pulse precedes the first bit clock
- bit 0 **SPIBEN:** Enhanced Buffer Enable bit
1 = Enhanced buffer is enabled
0 = Enhanced buffer is disabled (Legacy mode)

PIC24FJ256GB210 FAMILY

FIGURE 16-1: I²C™ BLOCK DIAGRAM



PIC24FJ256GB210 FAMILY

REGISTER 16-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last Hardware is set or clear when Start, Repeated Start or Stop is detected.
bit 3	S: Start bit 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last Hardware is set or clear when Start, Repeated Start or Stop is detected.
bit 2	R/W: Read/Write Information bit (when operating as I ² C slave) 1 = Read – indicates data transfer is output from the slave 0 = Write – indicates data transfer is input to the slave Hardware is set or clear after the reception of an I ² C device address byte.
bit 1	RBF: Receive Buffer Full Status bit 1 = Receive is complete, I2CxRCV is full 0 = Receive not complete, I2CxRCV is empty Hardware is set when I2CxRCV is written with the received byte; hardware is clear when the software reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit 1 = Transmit is in progress, I2CxTRN is full 0 = Transmit is complete, I2CxTRN is empty Hardware is set when software writes to I2CxTRN; hardware is clear at the completion of data transmission.

PIC24FJ256GB210 FAMILY

REGISTER 17-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN ⁽¹⁾	—	USIDL	IREN ⁽²⁾	RTSMD	—	UEN1	UEN0
bit 15						bit 8	

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **UARTEN:** UARTx Enable bit⁽¹⁾
 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
 0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption is minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** Stop in Idle Mode bit
 1 = Discontinue module operation when device enters Idle mode
 0 = Continue module operation in Idle mode
- bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit⁽²⁾
 1 = IrDA encoder and decoder are enabled
 0 = IrDA encoder and decoder are disabled
- bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Enable bits
 11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and UxRTS pins are enabled and used
 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ /BCLKx pins are controlled by port latches
- bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
 1 = UARTx will continue to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
 0 = No wake-up is enabled
- bit 6 **LPBACK:** UARTx Loopback Mode Select bit
 1 = Enable Loopback mode
 0 = Loopback mode is disabled
- bit 5 **ABAUD:** Auto-Baud Enable bit
 1 = Enable baud rate measurement on the next character – requires reception of a sync field (55h); cleared in hardware upon completion
 0 = Baud rate measurement is disabled or completed

Note 1: If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPN/RPIN pin. See **Section 10.4 “Peripheral Pin Select (PPS)”** for more information.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

PIC24FJ256GB210 FAMILY

18.7.4 USB V_{Bus} POWER CONTROL REGISTER

REGISTER 18-22: U1PWMCON: USB V_{Bus} PWM GENERATOR CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PWMEN	—	—	—	—	—	PWMPOL	CNTEN
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **PWMEN:** PWM Enable bit
1 = PWM generator is enabled
0 = PWM generator is disabled; output is held in the Reset state specified by PWMPOL
- bit 14-10 **Unimplemented:** Read as '0'
- bit 9 **PWMPOL:** PWM Polarity bit
1 = PWM output is active-low and resets high
0 = PWM output is active-high and resets low
- bit 8 **CNTEN:** PWM Counter Enable bit
1 = Counter is enabled
0 = Counter is disabled
- bit 7-0 **Unimplemented:** Read as '0'

PIC24FJ256GB210 FAMILY

TABLE 19-2: PARALLEL MASTER PORT PIN DESCRIPTION

Pin Name	Type	Description
PMA<22:16> ⁽¹⁾	O	Address Bus Bits<22-16>
PMA<15>, PMCS2	O	Address Bus Bit<15>
	O	Chip Select 2 (alternate location)
	I/O	Data Bus Bit<15> when port size is 16 bits and address is multiplexed
PMA<14>, PMCS1	O	Address Bus Bit<14>
	O	Chip Select 1 (alternate location)
	I/O	Data Bus Bit<14> when port size is 16-bit and address is multiplexed
PMA<13:8>	O	Address Bus Bits<13-8>
	I/O	Data Bus Bits<13-8> when port size is 16 bits and address is multiplexed
PMA<7:3>	O	Address Bus Bits<7-3>
PMA<2>, PMALU ⁽¹⁾	O	Address Bus Bit<2>
	O	Address latch upper strobe for multiplexed address
PMA<1>, PMALH	I/O	Address Bus Bit<1>
	O	Address latch high strobe for multiplexed address
PMA<0>, PMALL	I/O	Address Bus Bit<0>
	O	Address latch low strobe for multiplexed address
PMD<15:8>	I/O	Data Bus Bits<15-8> when address is not multiplexed
PMD<7:4>	I/O	Data Bus Bits<7-4>
	O	Address Bus Bits<7-4> when port size is 4 bits and address is multiplexed with 1 address phase
PMD<3:0>	I/O	Data Bus Bits<3-0>
PMCS1	I/O	Chip Select 1
PMCS2	O	Chip Select 2
PMWR, PMENB	I/O	Write strobe or enable signal depending on Strobe mode
PMRD, PMRD/PMWR	I/O	Read strobe or Read/Write signal depending on Strobe mode
PMBE1 ⁽¹⁾	O	Byte indicator
PMBE0	O	Nibble or byte indicator
PMACK1	I	Acknowledgment 1
PMACK2	I	Acknowledgment 2

Note 1: Available only in 100-pin devices (PIC24FJXXGB210).

PIC24FJ256GB210 FAMILY

FIGURE 23-3: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 1 AND CVREFP = 0

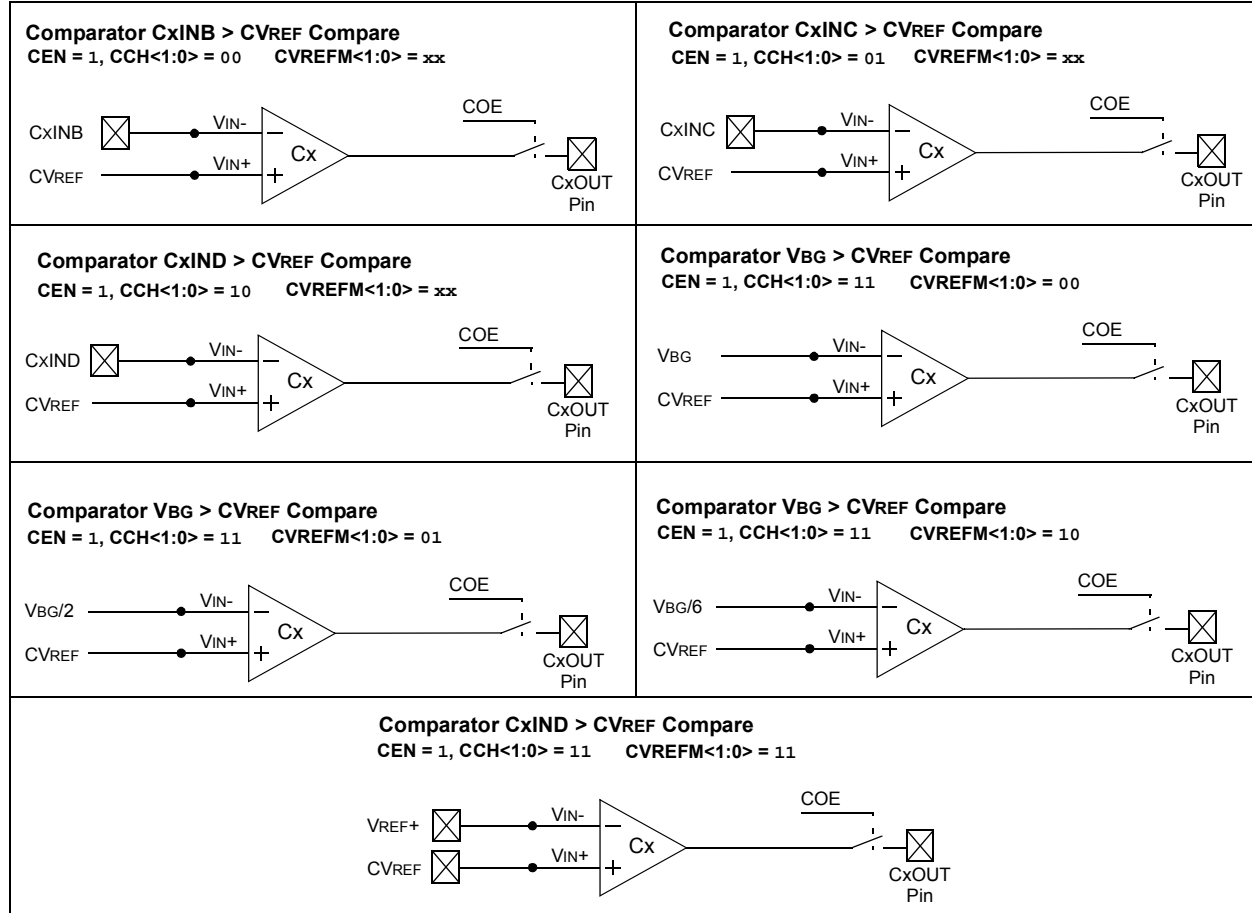
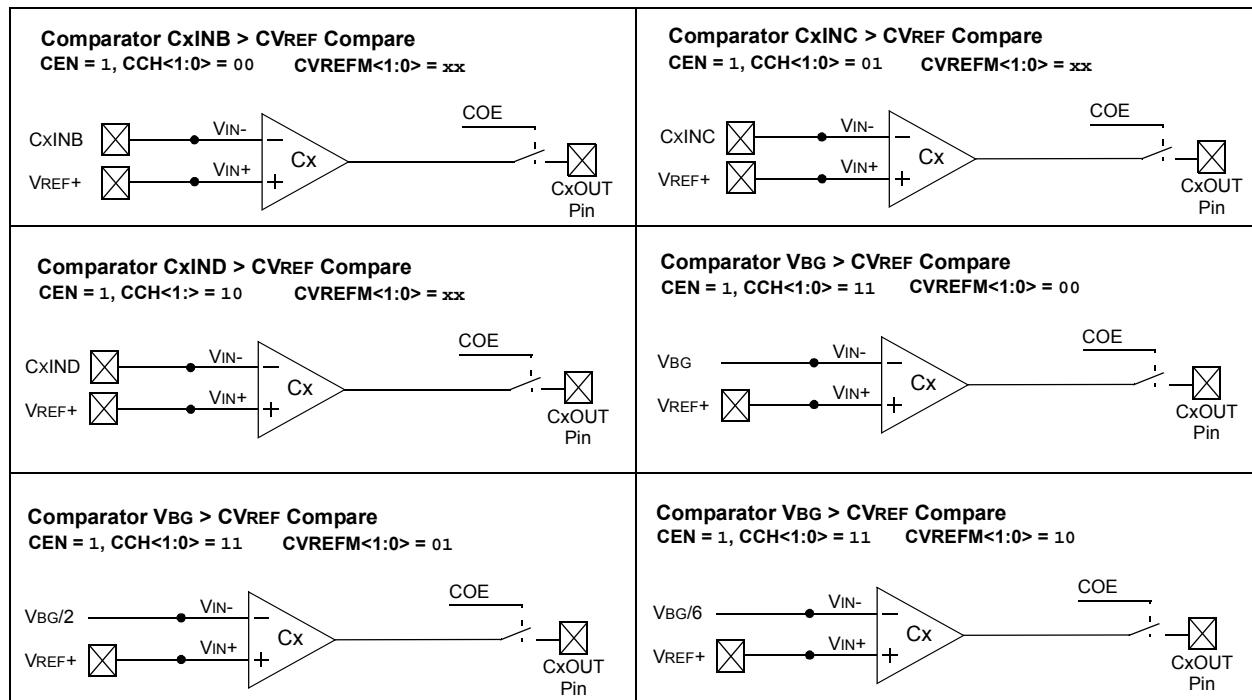


FIGURE 23-4: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 1 AND CVREFP = 1



PIC24FJ256GB210 FAMILY

26.2 On-Chip Voltage Regulator

All PIC24FJ256GB210 family devices power their core digital logic at a nominal 1.8V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the PIC24FJ256GB210 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator is controlled by the ENVREG pin. Tying VDD to the pin enables the regulator, which in turn, provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR capacitor (such as ceramic) must be connected to the VCAP pin (Figure 26-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor (CEFC) is provided in **Section 29.1 “DC Characteristics”**.

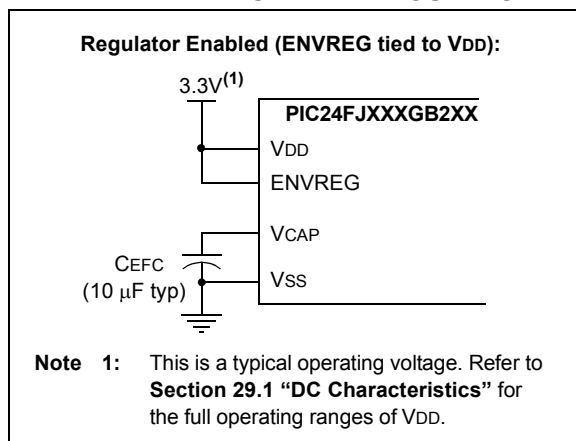
26.2.1 VOLTAGE REGULATOR LOW-VOLTAGE DETECTION

When the on-chip regulator is enabled, it provides a constant voltage of 1.8V nominal to the digital core logic.

The regulator can provide this level from a VDD of about 2.1V, all the way up to the device's VDDMAX. It does not have the capability to boost VDD levels. In order to prevent “brown-out” conditions when the voltage drops too low for the regulator, the Brown-out Reset occurs. Then the regulator output follows VDD with a typical voltage drop of 300 mV.

To provide information about when the regulator voltage starts reducing, the on-chip regulator includes a simple Low-Voltage Detect circuit, which sets the Low-Voltage Detect Interrupt Flag, LVDIF (IFS4<8>). This can be used to generate an interrupt to trigger an orderly shutdown.

FIGURE 26-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



26.2.2 ON-CHIP REGULATOR AND POR

When the voltage regulator is enabled, it takes approximately 10 µs for it to generate output. During this time, designated as TVREG, code execution is disabled. TVREG is applied every time the device resumes operation after any power-down, including Sleep mode. TVREG is determined by the status of the VREGS bit (RCON<8>) and the WUTSEL Configuration bits (CW3<11:10>). Refer to **Section 29.0 “Electrical Characteristics”** for more information on TVREG.

26.2.3 ON-CHIP REGULATOR AND BOR

When the on-chip regulator is enabled, PIC24FJ256GB210 family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain the output level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR (RCON<1>) flag bit. The brown-out voltage specifications are provided in **Section 7. “Reset”** (DS39712) in the “PIC24F Family Reference Manual”.

Note: For more information, see **Section 29.0 “Electrical Characteristics”**. The information in this data sheet supersedes the information in the FRM.

26.2.4 VOLTAGE REGULATOR STANDBY MODE

When enabled, the on-chip regulator always consumes a small incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode on its own whenever the device goes into Sleep mode. This feature is controlled by the VREGS bit (RCON<8>). Clearing the VREGS bit enables the Standby mode. When waking up from Standby mode, the regulator needs to wait for TVREG to expire before wake-up.

The regulator wake-up time required for Standby mode is controlled by the WUTSEL<1:0> (CW3<11:10>) Configuration bits. The regulator wake-up time is lower when WUTSEL<1:0> = 01, and higher when WUTSEL<1:0> = 11. Refer to the TVREG specification in Table 29-10 for regulator wake-up time.

When the regulator's Standby mode is turned off (VREGS = 1), the device wakes up without waiting for TVREG. However, with the VREGS bit set, the power consumption while in Sleep mode will be approximately 40 µA higher than what it would be if the regulator was allowed to enter Standby mode.

PIC24FJ256GB210 FAMILY

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
TBLRDL	TBLRDL <i>Ws, Wd</i>	Read Prog<15:0> to Wd	1	2	None
TBLWTH	TBLWTH <i>Ws, Wd</i>	Write Ws<7:0> to Prog<23:16>	1	2	None
TBLWTL	TBLWTL <i>Ws, Wd</i>	Write Ws to Prog<15:0>	1	2	None
ULNK	ULNK	Unlink Frame Pointer	1	1	None
XOR	XOR <i>f</i>	$f = f .XOR. WREG$	1	1	N, Z
	XOR <i>f, WREG</i>	$WREG = f .XOR. WREG$	1	1	N, Z
	XOR <i>#lit10, Wn</i>	$Wd = lit10 .XOR. Wd$	1	1	N, Z
	XOR <i>Wb, Ws, Wd</i>	$Wd = Wb .XOR. Ws$	1	1	N, Z
	XOR <i>Wb, #lit5, Wd</i>	$Wd = Wb .XOR. lit5$	1	1	N, Z
ZE	ZE <i>Ws, Wnd</i>	$Wnd = Zero-Extend Ws$	1	1	C, Z, N

PIC24FJ256GB210 FAMILY

TABLE 29-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Operating Voltage							
DC10	Supply Voltage						
	VDD		VBOR	—	3.6	V	Regulator enabled
	VCAP ⁽²⁾		—	1.8V	—	V	Regulator enabled
DC12	VDR	RAM Data Retention Voltage⁽¹⁾	1.5	—	—	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	Vss	—	—	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 66 ms 0-2.5V in 50 ms
	VBOR	Brown-out Reset Voltage on VDD Transition, High-to-Low	2.0	2.10	2.2	V	Regulator enabled
	VLVD	LVD Trip Voltage	—	VBOR + 0.10	—	V	

Note 1: This is the limit to which the RAM data can be retained, while the on-chip regulator output voltage starts following the VDD.

2: This is the on-chip regulator output voltage specification.



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