



Welcome to E-XFL.COM

Understanding [Embedded - Microcontroller, Microprocessor, FPGA Modules](#)

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of [Embedded - Microcontroller,](#)

Details

Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Artix-7 A200T
Co-Processor	-
Speed	-
Flash Size	32MB
RAM Size	256KB
Connector Type	SO-DIMM-204
Size / Dimension	2.7" x 2.0" (68mm x 51mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/soc-technologies/dc-v-h264-8b-30-1080-mxc-sl

6. The H.264 4K Encoder Modules

- 6.1 Pin Assignments and Pin Voltages**
- 6.2 Signal Formats**
 - 6.2.1 Clock Signals (Input, Output)**
 - 6.2.2 Video Data Signals (Input)**
 - 6.2.3 Audio Data Signals (Input)**
 - 6.2.4 TS Signals (Output)**
 - 6.2.5 Encoder Control Signals (Input and Output)**
- 6.3 Power Rails of MCM-1000Z**
- 6.4 Power Requirement and Supply Amperage**

7. The H.264 4K Decoder Modules

- 7.1 Pin Assignments and Pin Voltages**
- 7.2 Signal Formats**
 - 7.2.1 Video Clock Signal (Input)**
 - 7.2.2 Video Data Signals (Output)**
 - 7.2.3 Audio Data Signals (Output)**
 - 7.2.4 TS Signals (Input)**
 - 7.2.5 Decoder Control Signals (Input and Output)**
- 7.3 Power Rails of MCM-1000Z**
- 7.4 Power Requirement and Supply Amperage**

8. The H.265 HD Encoder Modules

- 8.1 Pin Assignments and Pin Voltages**
- 8.2 Signal Formats**
 - 8.2.1 Clock Signal (Input)**
 - 8.2.2 Video Data Signals (Input)**
 - 8.2.3 Audio Data Signals (Input)**
 - 8.2.4 TS Signals (Output)**
 - 8.2.5 Encoder Control Signals (Input and Output)**
- 8.3 Power Rails of MCM-1000SX**
- 8.4 Power Requirement and Supply Amperage**

9. The H.265 HD Decoder Modules

- 9.1 Pin Assignments and Pin Voltages**
- 9.2 Signal Formats**
 - 9.2.1 Clock Signal (Input)**
 - 9.2.2 Video Data Signals (Output)**
 - 9.2.3 Audio Data Signals (Output)**
 - 9.2.4 TS Signals (Input)**
 - 9.2.5 Encoder Control Signals (Input and Output)**
- 9.3 Power Rails of MCM-1000SX**
- 9.4 Power Requirement and Supply Amperage**

10. The H.265 4K Encoder Modules

- 10.1 Pin Assignments and Pin Voltages**
- 10.2 Signal Formats**
 - 10.2.1 Clock Signals (Input, Output)**
 - 10.2.2 Video Data Signals (Input)**
 - 10.2.3 Audio Data Signals (Input)**
 - 10.2.4 TS Signals (Output)**
 - 10.2.5 Decoder Control Signals (Input and Output)**
- 10.3 Power Rails of MCM-1000SX**
- 10.4 Power Requirement and Supply Amperage**

11. The H.265 4K Decoder Modules

- 11.1 Pin Assignments and Pin Voltages**
- 11.2 Signal Formats**
 - 11.2.1 Clock Signals (Input, Output)**
 - 11.2.2 Video Data Signals (Output)**
 - 11.2.3 Audio Data Signals (Output)**
 - 11.2.4 TS Signals (Input)**
 - 11.2.5 Decoder Control Signals (Input and Output)**
- 11.3 Power Rails of MCM-1000SX**
- 11.4 Power Requirement and Supply Amperage**

1. Overview of SOC SOM Modules

The SOC SOMs are small circuit boards with FPGA, DDRs, Flash, and clocks in one module to support FPGA-based systems. A module can be configured into a SOM by using the applicable firmware. The module is connected to a user PCB through a standard DDR3 SODIMM connector. Customers can order the blank SOMs from SOC and use their own firmware to make SOM products.

SOC configures the modules into MPEG codec SOMs for video/audio compression, decompression, and transcoding functions. Currently available modules are:

	Hardware Product Code	FPGA Chip on the Module	SOC Codec module Resolution Capacity
1	MCM-1000S	Spartan-6 XC6SLX150	H.264 or MPEG-2 HD up to 1080@30
2	MCM-1000A	Artix-7 XC7A200T	H.264 or MPEG-2 HD up to 1080@60
3	MCM-1000Z	Zynq-7 XC7Z035/045	H.264 4k@30/60, or H.265 HD up to 1080@60
4	MCM-1000SX	Arria-10 SX220/270/320/480/570/660	H.264 HD 1080@30/60, or H.264 4k@30/60, or H.265 HD up to 1080@60), or H.265 4k@30/60

Fig. 1 shows a photo of the modules. Fig. 2-5 shows the dimensions of MCM-1000S, MCM-1000A, MCM-1000Z, and MCM-1000SX respectively.



Fig. 1 SOC codec modules

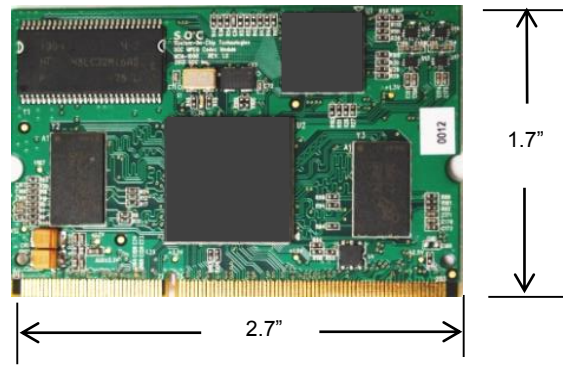


Fig. 2. Dimension of MCM-1000S

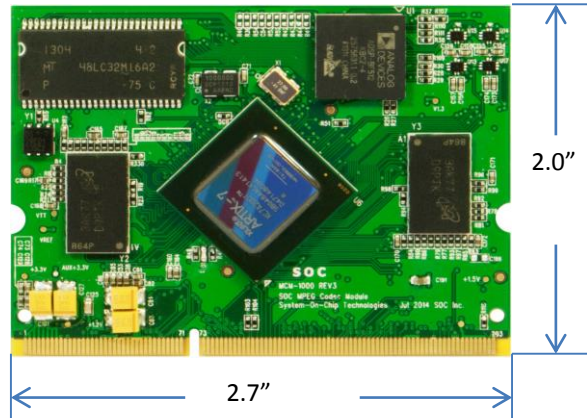


Fig. 3. Dimension of MCM-1000A

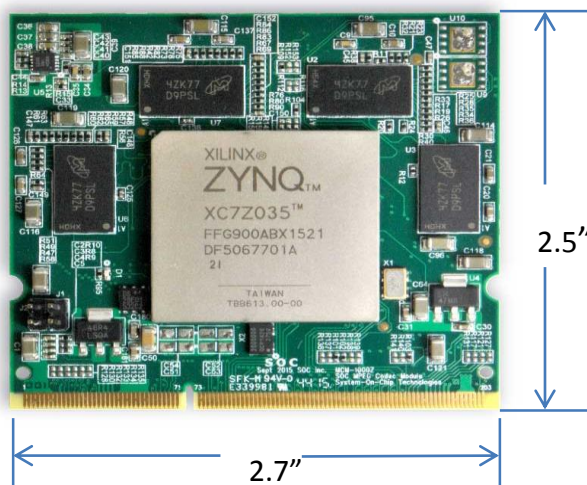


Fig. 4. Dimension of MCM-1000Z

Appendix-A provides the details of the Standard Codec Modules, including the product tables which list the product codes along with the specifications. Customers can order the modules according the specifications required by using the corresponding product code.

The pin assignments, pin voltages, and signal formats for standard encoder and decoder modules are detailed respectively in this Datasheet in the following sections:

- Section 4: The H.264 (and MPEG-2) HD Encoder Modules
- Section 5: The H.264 (and MPEG-2) HD Decoder Modules
- Section 6: The H.264 4k Encoder Modules
- Section 7: The H.264 4k Decoder Modules
- Section 8: The H.265 HD Encoder Modules
- Section 9: The H.265 HD Decoder Modules (will be available soon)
- Section 10: The H.265 4k Encoder Modules
- Section 11: The H.265 4k Encoder Modules (will be available soon)

It should be noted that not all of the modules listed in Appendix-A are discussed in this Datasheet. Pin assignments and electrical properties for the modules that are not provided in the document, will be provided on demand basis.

SOC also offers customized modules according to customer requirements, such as Transcoder modules, Multi-channel encoder or decoder modules, and modules with non-standard I/Os. For details, contact SOC sales at: sales@soctechnologies.com

One of the popular extended versions of the standard codec modules is the –NET version which integrates the SOC low latency network stack (UDP/IP over Ethernet) into the encoder or decoder module. The pin assignments, pin voltages, and signal formats for the –NET version encoder and decoder modules are detailed in the document:

[Datasheet – Encoder and Decoder Modules – NET Version](#)

4. The H.264 (and MPEG-2) HD Encoder Modules

4.1 Pin Assignments and Pin Voltages

The HD encoder modules for H.264 and MPEG-2 have the same pin assignments and electrical properties. The hardware module for HD resolution uses the MCM-1000A (the Artix-7 A200T FPGA), the hardware module MCM-1000Z is used for 4k resolutions (the Zynq-7035 for 4k@30, Zynq-7045 for 4k@60).

This Section provides the pin assignments and electrical properties for HD encoder (H.264, or MPEG-2) module which is based on the MCM-1000A. Table-1 lists the pin assignments and the pin voltages.

The schematics of MCM-1000A edge connector are attached in Appendix-B of this document, which shows the pin numbers for data, clock, control, and power. It should be noted that the encoder module uses only some of the edge pins, and not all of the edge pins are used.

Table-1 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Artix-7 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

Table 1: HD Encoder Module (based on MCM-1000A) Pin Assignment and Pin Voltages

Description	MCM-1000A Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
External Reset	121	Input	W21	3.3v	LVC MOS33
Video Clock	105	Input	Y11	3.3v	LVC MOS33
Video Horizontal Sync	146	Input	W16	3.3v	LVC MOS33
Video Vertical Sync	148	Input	V15	3.3v	LVC MOS33
Video Display Enable	150	Input	U15	3.3v	LVC MOS33
Video Data Luma[0]	50	Input	W14	3.3v	LVC MOS33
Video Data Luma[1]	52	Input	Y14	3.3v	LVC MOS33
Video Data Luma[2]	58	Input	V10	3.3v	LVC MOS33
Video Data Luma[3]	59	Input	Y13	3.3v	LVC MOS33
Video Data Luma[4]	60	Input	W10	3.3v	LVC MOS33
Video Data Luma[5]	61	Input	AA14	3.3v	LVC MOS33
Video Data Luma[6]	80	Input	AB13	3.3v	LVC MOS33
Video Data Luma[7]	82	Input	AA13	3.3v	LVC MOS33
Video Data Luma[8]	84	Input	AB17	3.3v	LVC MOS33
Video Data Luma[9]	86	Input	AB16	3.3v	LVC MOS33
Video Data Chroma[0]	92	Input	AA15	3.3v	LVC MOS33
Video Data Chroma[1]	94	Input	AB15	3.3v	LVC MOS33
Video Data Chroma[2]	96	Input	AB12	3.3v	LVC MOS33
Video Data Chroma[3]	98	Input	AB11	3.3v	LVC MOS33
Video Data Chroma[4]	107	Input	Y12	3.3v	LVC MOS33
Video Data Chroma[5]	108	Input	W12	3.3v	LVC MOS33
Video Data Chroma[6]	110	Input	Y17	3.3v	LVC MOS33
Video Data Chroma[7]	140	Input	T14	3.3v	LVC MOS33
Video Data Chroma[8]	142	Input	T15	3.3v	LVC MOS33
Video Data Chroma[9]	144	Input	W15	3.3v	LVC MOS33
SPDIF Audio	109	Input	Y21	3.3v	LVC MOS33

4.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** (pin # 69) is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

4.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**; along with the Transport Stream output data clock **Transport Stream Clock** (pin # 113). The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready (pin # 118) and **Transport Stream Data Valid** (pin # 135) are the signals to inform the user side to take over the signals.

4.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

An external reset pin (pin # 121) is available. This pin allows the user to reset the encoder when necessary. A high signal will trigger a reset. The reset signal should be maintained at low when in normal operation mode.

4.3 Power Rails of MCM-1000A

Table-2 lists the power and ground pins. Refer to Appendix-A for the pins of power and ground on the edge connector of the MCM-1000A module.

Table-2: MCM-1000A Power and Ground Pins

MCM-1000S Connector Pin	Voltage
1,3,5,7,9,11,13,15	3.3V
10,12,14,16	1.2V
22,24,26,28,30,32	1.5V
189,191,193,195,197,199	2.5V
188,190,192,194	1.3V
43,45,47,49,51,53,55,57	1.0V
2,4,6,8,18,20,34,36,42,44,62,72	Ground
17,35,37,39,41,71	Ground
73,75,129	Ground
74	Ground
163,165,167,169,175,177,185,187,203	Ground
168,170,172,174,176,184,186,200,202,204	Ground

5. The H.264 (and MPEG-2) HD Decoder Modules

5.1 Pin Assignments and Pin Voltages

The decoders for H.264 and MPEG-2 have the same pin assignment. The module for HD resolution decoding uses the MCM-1000A (with the Artix-7 A200T FPGA which is the same as the one used for the HD Encoder). The module MCM-1000Z is used for 4k decoding (the Zynq-7035 for 4k@30, Zynq-7045 for 4k@60).

This section details the pin assignments and pin voltages for the HD decoder (H.264, and MPEG-2) modules. Table-4 shows the pin assignments and the pin voltages.

The schematics of MCM-1000A edge connector are attached in Appendix-B of this document. Appendix-B shows the pin numbers for data, clock, control, and power, which are connected to the FPGA (Artix-7 XC7A200T). It should be noted that the decoder module uses only some of the available edge pins that are connected to the FPGA (some of the pins are not used).

It should also be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

Table-4: HD Decoder Module (based on MCM-1000A) Pin Assignment

Description	MCM-1000A Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
External Reset	121	Input	W21	3.3v	LVCMS33
Decoder Clock	115	Input	U20	3.3v	LVCMS33
Video Clock	105	Output	Y11	3.3v	LVCMS33
Video Horizontal Sync	146	Output	W16	3.3v	LVCMS33
Video Vertical Sync	148	Output	V15	3.3v	LVCMS33
Video Display Enable	150	Output	U15	3.3v	LVCMS33
Video Data Luma[0]	50	Output	W14	3.3v	LVCMS33
Video Data Luma[1]	52	Output	Y14	3.3v	LVCMS33
Video Data Luma[2]	58	Output	V10	3.3v	LVCMS33
Video Data Luma[3]	59	Output	Y13	3.3v	LVCMS33
Video Data Luma[4]	60	Output	W10	3.3v	LVCMS33
Video Data Luma[5]	61	Output	AA14	3.3v	LVCMS33
Video Data Luma[6]	80	Output	AB13	3.3v	LVCMS33
Video Data Luma[7]	82	Output	AA13	3.3v	LVCMS33
Video Data Luma[8]	84	Output	AB17	3.3v	LVCMS33
Video Data Luma[9]	86	Output	AB16	3.3v	LVCMS33
Video Data Chroma[0]	92	Output	AA15	3.3v	LVCMS33
Video Data Chroma[1]	94	Output	AB15	3.3v	LVCMS33
Video Data Chroma[2]	96	Output	AB12	3.3v	LVCMS33
Video Data Chroma[3]	98	Output	AB11	3.3v	LVCMS33
Video Data Chroma[4]	107	Output	Y12	3.3v	LVCMS33
Video Data Chroma[5]	108	Output	W12	3.3v	LVCMS33
Video Data Chroma[6]	110	Output	Y17	3.3v	LVCMS33
Video Data Chroma[7]	140	Output	T14	3.3v	LVCMS33
Video Data Chroma[8]	142	Output	T15	3.3v	LVCMS33
Video Data Chroma[9]	144	Output	W15	3.3v	LVCMS33
Video Frame Sync Relock	56	Input	AB21	3.3v	LVCMS33

to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]**, **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. A **Video Clock** (refer to Section 5.2.1 for the clock frequencies) is sent out, which provides the timing for the parallel inputs of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal (pin #150) is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

Output data are sampled at the rising edge of the clock. (The clock rates will correspond to the resolution and frame rate, as discussed in Section 5.2.1.)

5.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

5.2.4 TS Stream Signals (Input)

The input of the decoder module is an MPEG transport stream, which is sent into the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**. **Transport Stream Clock** (27MHz) is the clock for the **Transport Stream Data** lines. The **Transport Stream Data Valid** signal informs the decoder that the input is valid.

5.2.5 Decoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Decoder API User Manual](#) for details.

5.3 Power Rails of MCM-1000A

The power rails for the HD (H.264 or MPEG-2) decoder module is the same as the ones for the HD encoder module. Refer to Table-2 for the power and ground pins. Also, refer to Appendix-A for the power and ground pins on the edge connector of the MCM-1000A module.

5.4 Power Requirement and Supply Amperage

The total power at operation required by a given decoder ranges from 2 to 4 Watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail delivers only a portion of the total lower. However, the power is not evenly distributed among the rails. Table-5 lists the power

estimation by Xilinx Vivado FPGA software for each rail, at 1080p@60 resolution, and can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-5 is higher than the measured real power.

Again, the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-5.

Table-5: Power estimation for the decoder module (1080p@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	2.421	2.362	0.058
Vccaux	1.800	0.497	0.464	0.033
Vcco33	3.300	0.053	0.048	0.005
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.500	0.495	0.005
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.037	0.028	0.009
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.022	0.002	0.020

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 6 of this document. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for further details.

Chroma[9], for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization if embedded SAV/EAV are not used. The video clocks (refer to Section 6.2.1) provide the timing for the parallel input of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync** signals. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Video Display Enable** signal at high, when active pixels are being sent out.

The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section 6.2.1.

6.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

6.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**, along with the Transport Stream output data clock **Transport Stream Clock** (pin # 31). The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready (pin # 28) and **Transport Stream Data Valid** (pin # 33) are the signals to inform the user side to take over the signals.

6.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

An external reset **PS Soft Reset_B** (pin # 156) is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

6.3 Power Rails of MCM-1000Z

Refer to Appendix-B for the pins of power and ground on the edge connector of the MCM-1000Z module. The power rails are: 1.0V, 1.2V, 1.3V, 1.5V, 2.5V, and 3.3V.

6.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 3 to 6 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-7 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 4k@60 resolution, which can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-7 is higher than the measured real power of the module. However, for PCB design purposes, Table-7 is sufficient. It should also be noted that the power rails 1.8v and 2.0v are generated on the module, by using some of the input power rails. Carrier board PCB designers need not to consider these two rails.

Table-7: Power estimation for the H.264 4k encoder module (4k@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	5.462	5.351	0.111
Vccaux	1.800	0.558	0.500	0.058
Vcco33	3.300	0.006	0.005	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.001	0.000	0.001
Vcco15	1.500	0.429	0.428	0.001
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_jo	2.000	0.109	0.109	0.000
Vccbram	1.000	0.083	0.057	0.026
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
MGTVccaux	1.800	0.000	0.000	0.000
Vccpint	1.000	0.750	0.723	0.027
Vccpaux	1.800	0.061	0.051	0.010
Vccpll	1.800	0.019	0.016	0.003
Vcco_ddr	1.500	0.459	0.457	0.002
Vcco_mio0	1.800	0.007	0.006	0.001
Vcco_mio1	1.800	0.001	0.000	0.001
Vccadc	1.800	0.022	0.002	0.020

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 12 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for design licensing information.

6 of this document, is for 4k resolution. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for further details.

Table-10: Power estimation for the decoder module (4K@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	4.786	4.682	0.104
Vccaux	1.800	0.692	0.634	0.058
Vcco33	3.300	0.007	0.006	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.001	0.000	0.001
Vcco15	1.500	0.429	0.428	0.001
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	2.000	0.109	0.109	0.000
Vccbram	1.000	0.093	0.074	0.019
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
MGTVccaux	1.800	0.000	0.000	0.000
Vccpint	1.000	0.750	0.723	0.026
Vccpaux	1.800	0.061	0.051	0.010
Vccpll	1.800	0.019	0.016	0.003
Vcco_ddr	1.500	0.459	0.457	0.002
Vcco_mio0	1.800	0.007	0.006	0.001
Vcco_mio1	1.800	0.001	0.000	0.001
Vccadc	1.800	0.022	0.002	0.020

12. Carrier Board PCB Reference Designs

SOC has several evaluation boards for evaluating the standard encoder and decoder modules (and for evaluating the IP cores as well). These evaluation boards provide not only the DDR3 SODIMM connectors for connecting the encoder (and/or decoder) modules, but also the commonly used digital video/audio ports, such as SDI and HDMI. Ethernet port of tri-speed, 10/100/1000Mbps, as a network connection, is used in all of the SOC evaluation boards.

12.1 VTR-S1000 Evaluation Board

Fig. 11 shows a photo of the VTR-S1000 board. Major components and I/O ports are marked in the figure. Refer to the [User Guide of VTR -S1000](#) for further details.

SOC licenses the Schematics of VTR-S1000 to the customers that have purchased the eval kit VTR-S1000 and encoder (or decoder) Modules. Firmware of the VTR-S1000, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, sales@soctechnologies.com, for details.

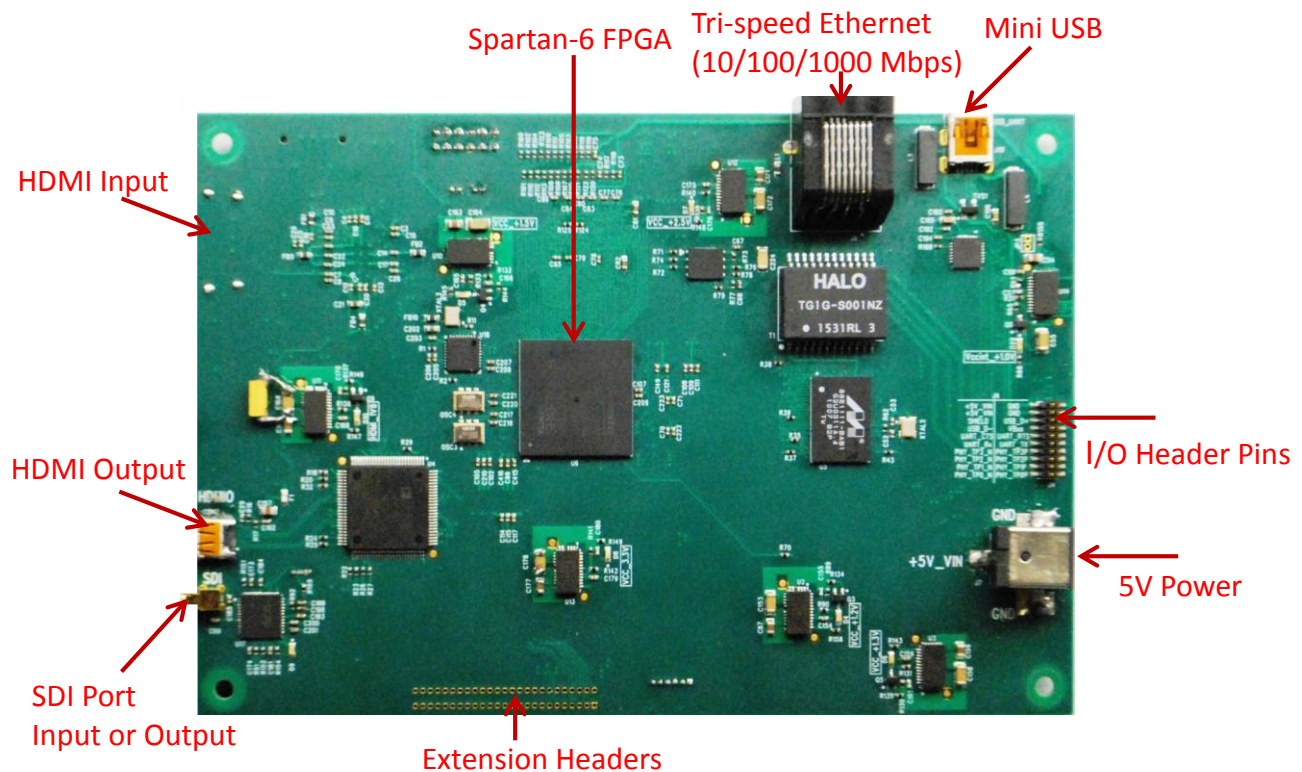


Fig. 11. FMC-MCM-1000 evaluation board

15. Document Revisions

Version #	Revision Date	Notes
V.1.0	10/05/2017	First release
V.1.1	19/05/2017	Minor revision
V.2.0	20/05/2017	Major revision (adding 4k)
V.2.1	05/06/2017	Minor revision

Table-A2: H.265 Video&Audio Encoder Modules (both video and audio):

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-VA-H265-8b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12bits	up to 60fps	AAC or MPEG2 Layer-2

A.2 H.264 Encoder Modules

The H.264 encoder modules are based on either the on the MCM-1000A hardware. The SOC H.264 encoder IP cores are used to configure the FPGAs on the hardware modules to produce the codec modules.

Table-A3 lists the product code of the factory standard video encoder modules (video only), along with the specifications for each module. Table-A4 lists the video/audio encoder modules (both video and audio). Customers can order the encoder modules using the product code, according to the specifications required by the application.

Table-A3: H.264 Video Encoder Modules (video only without audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H264-8b-30-720-MS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-H264-8b-60-720-MS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-H264-8b-30-1080-MS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-H264-10b-30-1080-MS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	MCM-1000A
EC-V-H264-8b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-H264-10b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	MCM-1000A
EC-V-H264-8b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 8 bits	up to 30fps	no	MCM-1000Z
EC-V-H264-10b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	MCM-1000Z
EC-V-H264-8b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 8 bits	up to 60fps	no	MCM-1000Z
EC-V-H264-10b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	MCM-1000Z

Table-A6: H.264 Video&Audio Decoder Modules (both video and audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H264-8b-30-720-MA	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-60-720-MA	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-30-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-10b-30-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-10b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-10b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	10 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-8b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-10b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	10 bits	up to 60fps	AAC/MPEG2 L-2 L	MCM-1000Z

A.4 MPEG-2 Encoder Modules

Table-A7 lists the standard MPEG-2 video encoder modules. Table-A8 lists the MPEG-2 video/audio encoder modules. The 8-bit precision and 60 frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A7: MPEG-2 Video Encoder Module (video only without audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-MPEG2-8b-30-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-MPEG2-8b-30-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A

Table-A8: MPEG-2 Video&Audio Encoder Modules (both video and audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-MPEG2-8b-30-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-30-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A

A.8 MPEG2-to-H.264 Transcoder Modules

Table-A15 lists the standard MPEG2-to-H.264 video transcoder modules, and Table-A16 lists the MPEG2-to-H.264 video/audio transcoder modules. The 60frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A15: MPEG2-to-H.264 Video Transcoder Modules (video only without audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-MPEG2-to-H.264-8b-30-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-60-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-30-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-60-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000A

Table-A16: MPEG2-to-H.264 Video&Audio Transcoder Modules (both video and audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-VA-MPEG2-to-H.264-8b-30-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-60-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-30-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-60-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC	MCM-1000A

A.9 Non-Standard Codec Modules

The previous section provides the information on SOC's factory standard MPEG codec modules. Customers can order modules based on customer specific requirements (non-standard modules). There is a Minimum Order Quantity (MOQ) required for customized configurations. Contact SOC sales sale@soctechologies.com for information.

Appendix - B MCM-1000A Edge Connector Schematics

