System On Chip (SOC) Technologies Inc. - DC-V-H264-8B-30-1080-MXC-ZL Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Artix-7 A200T
Co-Processor	-
Speed	-
Flash Size	32MB
RAM Size	256KB
Connector Type	SO-DIMM-204
Size / Dimension	2.7" x 2.0" (68mm x 51mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/soc-technologies/dc-v-h264-8b-30-1080-mxc-zl

9. The H.265 HD Decoder Modules

10. The H.265 4K Encoder Modules

11. The H.265 4K Decoder Modules

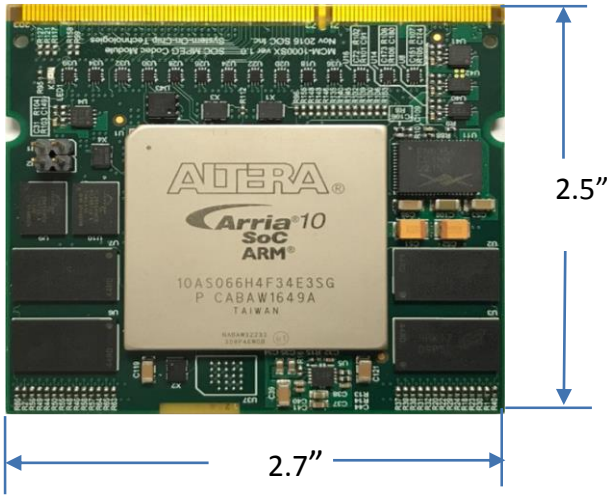


Fig. 5. Dimension of MCM-1000SX

2. Connecting the Module to a User PCB

The MCM-1000S/A/Z/SX modules have identical edge pins that are compatible with standard DDR3 SODIMM connectors. The following off-the-shelf DDR3 SODIMM connectors can be used to connect the SOC codec modules onto a user PCB:

1. MM80-204B1-1
2. MM80-204B1-1E
3. AS0A621-U2SN-7F
4. AS0A621-H2S6-7H

Fig. 6 shows a photo of a standard 204 pin DDR3 SODIMM PCB connector. Refer to the datasheet of the connector used for the physical dimension and PCB design requirements.

Fig. 6 A photo of the standard 204 pin DDR3 SODIMM connector

3. Overview SOC Standard Codec Modules

Each of the above described SOMs: the **MCM-1000S** (based on Spatran-6 FPGA), **MCM-1000A** (based on Artix-7 FPGA), **MCM-1000Z** (based on Zynq-7 FPGAs), and **MCM-1000SX** (based on Altera Arria-10 FPGAs); can be configured into different products by down-loading the desired firmware. At SOC, we produce encoder, decoder, transcoder, and multi-channel encoder or decoder SOMs for video compressions, by down-loading **SOC MPEG Codec IP** cores onto the modules.

The standard encoder modules: H.265, H.264, and MPEG-2, take raw video and audio as input and output TS streams, via the edge pins of the modules, as shown in Fig. 7. The standard decoder modules: H.265, H.264, and MPEG-2, take TS stream as inputs and output decoded video and audio, via the edge pins of the modules, as shown in Fig. 8. There are also control signal pins, to allow the user control of the encoder or decoder.

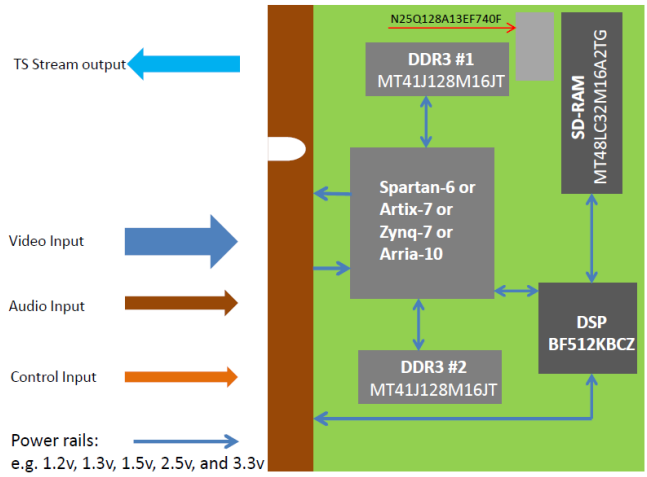


Fig. 7 SOC Standard encoder modules (H.265, H.264, or MPEG-2)

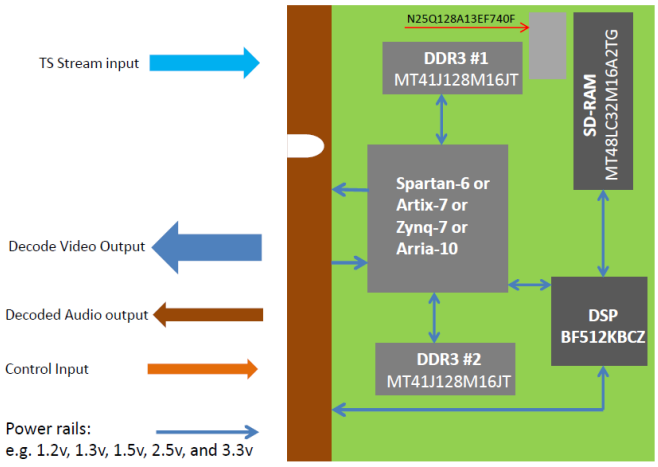


Fig. 8 SOC Standard decoder modules (H.265, H.264, or MPEG-2)

Appendix-A provides the details of the Standard Codec Modules, including the product tables which list the product codes along with the specifications. Customers can order the modules according the specifications required by using the corresponding product code.

The pin assignments, pin voltages, and signal formats for standard encoder and decoder modules are detailed respectively in this Datasheet in the following sections:

- Section 4: The H.264 (and MPEG-2) HD Encoder Modules
- Section 5: The H.264 (and MPEG-2) HD Decoder Modules
- Section 6: The H.264 4k Encoder Modules
- Section 7: The H.264 4k Decoder Modules
- Section 8: The H.265 HD Encoder Modules
- Section 9: The H.265 HD Decoder Modules (will be available soon)
- Section 10: The H.265 4k Encoder Modules
- Section 11: The H.265 4k Encoder Modules (will be available soon)

It should be noted that not all of the modules listed in Appendix-A are discussed in this Datasheet. Pin assignments and electrical properties for the modules that are not provided in the document, will be provided on demand basis.

SOC also offers customized modules according to customer requirements, such as Transcoder modules, Multi-channel encoder or decoder modules, and modules with non-standard I/Os. For details, contact SOC sales at: sales@soctechnologies.com

One of the popular extended versions of the standard codec modules is the –NET version which integrates the SOC low latency network stack (UDP/IP over Ethernet) into the encoder or decoder module. The pin assignments, pin voltages, and signal formats for the –NET version encoder and decoder modules are detailed in the document:

Datasheet – Encoder and Decoder Modules – NET Version

4.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 2 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-3 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 1080p@60 resolution, which can be used as a reference for PCB design. It should be noted that the measured real power consumption is about 20% lower than the estimated power consumption.

It should be noted that the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-2, as the 1.8v is generated on the module.

Table-3: Power estimation for the encoder module (1080p@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	3.792	3.723	0.069
Vccaux	1.800	0.454	0.421	0.034
Vcco33	3.300	0.013	0.008	0.005
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.499	0.494	0.005
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.063	0.052	0.011
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.022	0.002	0.020

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 12 of this document. The reference designs provide not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for design licensing details.

5. The H.264 (and MPEG-2) HD Decoder Modules

5.1 Pin Assignments and Pin Voltages

The decoders for H.264 and MPEG-2 have the same pin assignment. The module for HD resolution decoding uses the MCM-1000A (with the Artix-7 A200T FPGA which is the same as the one used for the HD Encoder). The module MCM-1000Z is used for 4k decoding (the Zynq-7035 for 4k@30, Zynq-7045 for 4k@60).

This section details the pin assignments and pin voltages for the HD decoder (H.264, and MPEG-2) modules. Table-4 shows the pin assignments and the pin voltages.

The schematics of MCM-1000A edge connector are attached in Appendix-B of this document. Appendix-B shows the pin numbers for data, clock, control, and power, which are connected to the FPGA (Artix-7 XC7A200T). It should be noted that the decoder module uses only some of the available edge pins that are connected to the FPGA (some of the pins are not used).

It should also be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

Table-4: HD Decoder Module (based on MCM-1000A) Pin Assignment

Description	MCM-1000A Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
External Reset	121	Input	W21	3.3v	LVCMOS33
Decoder Clock	115	Input	U20	3.3v	LVCMOS33
Video Clock	105	Output	Y11	3.3v	LVCMOS33
Video Horizontal Sync	146	Output	W16	3.3v	LVCMOS33
Video Vertical Sync	148	Output	V15	3.3v	LVCMOS33
Video Display Enable	150	Output	U15	3.3v	LVCMOS33
Video Data Luma[0]	50	Output	W14	3.3v	LVCMOS33
Video Data Luma[1]	52	Output	Y14	3.3v	LVCMOS33
Video Data Luma[2]	58	Output	V10	3.3v	LVCMOS33
Video Data Luma[3]	59	Output	Y13	3.3v	LVCMOS33
Video Data Luma[4]	60	Output	W10	3.3v	LVCMOS33
Video Data Luma[5]	61	Output	AA14	3.3v	LVCMOS33
Video Data Luma[6]	80	Output	AB13	3.3v	LVCMOS33
Video Data Luma[7]	82	Output	AA13	3.3v	LVCMOS33
Video Data Luma[8]	84	Output	AB17	3.3v	LVCMOS33
Video Data Luma[9]	86	Output	AB16	3.3v	LVCMOS33
Video Data Chroma[0]	92	Output	AA15	3.3v	LVCMOS33
Video Data Chroma[1]	94	Output	AB15	3.3v	LVCMOS33
Video Data Chroma[2]	96	Output	AB12	3.3v	LVCMOS33
Video Data Chroma[3]	98	Output	AB11	3.3v	LVCMOS33
Video Data Chroma[4]	107	Output	Y12	3.3v	LVCMOS33
Video Data Chroma[5]	108	Output	W12	3.3v	LVCMOS33
Video Data Chroma[6]	110	Output	Y17	3.3v	LVCMOS33
Video Data Chroma[7]	140	Output	T14	3.3v	LVCMOS33
Video Data Chroma[8]	142	Output	T15	3.3v	LVCMOS33
Video Data Chroma[9]	144	Output	W15	3.3v	LVCMOS33
Video Frame Sync Relock	56	Input	AB21	3.3v	LVCMOS33

SPDIF Audio	109	Output	Y21	3.3v	LVCMOS33
Transport Stream Clock **(27MHz)**	93	Output	Y18	3.3v	LVCMOS33
Transport Stream Data Valid	106	Output	R17	3.3v	LVCMOS33
Transport Stream Data[0]	77	Output	N13	3.3v	LVCMOS33
Transport Stream Data[1]	79	Output	N14	3.3v	LVCMOS33
Transport Stream Data[2]	81	Output	R18	3.3v	LVCMOS33
Transport Stream Data[3]	83	Output	T18	3.3v	LVCMOS33
Transport Stream Data[4]	85	Output	U17	3.3v	LVCMOS33
Transport Stream Data[5]	87	Output	U18	3.3v	LVCMOS33
Transport Stream Data[6]	89	Output	AB18	3.3v	LVCMOS33
Transport Stream Data[7]	91	Output	AA18	3.3v	LVCMOS33
Uart_tx	90	Output	AA16	3.3v	LVCMOS33
Uart_rx	88	Input	Y16	3.3v	LVCMOS33

5.2 Signal Formats

5.2.1 Clock Signals

The **Decoder Clock** signal (pin # 115) is an input clock for driving the decoder engine. The default frequency is **27MHz**. However, when an SDI port on the carrier board is used to send out the decoded video data, the SDI clock can be connected to the **Decoder Clock.** This will automatically synchronize the decoder outputs with the SDI interface.

The SDI clock frequencies are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

The **Video Clock** signal (pin # 105) is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

4. 27MHz, for SD resolution
5. 74.25MHz, for 720@60 and 1080@30
6. 148.5MHz, for 1080@60.

5.2.2 Video Data Signals (Output)

The output of the HD decoder module (H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma and 10 lines. And, **Video Data Chroma[0]**

to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. A **Video Clock** (refer to Section **5.2.1** for the clock frequencies) is sent out, which provides the timing for the parallel inputs of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal (pin #150) is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

Output data are sampled at the rising edge of the clock. (The clock rates will correspond to the resolution and frame rate, as discussed in Section **5.2.1.)**

5.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

5.2.4 TS Stream Signals (Input)

The input of the decoder module is an MPEG transport stream, which is sent into the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]. Transport Stream Clock** (27MHz) is the clock for the **Transport Stream Data** lines. The **Transport Stream Data Valid** signal informs the decoder that the input is valid.

5.2.5 Decoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

5.3 Power Rails of MCM-1000A

The power rails for the HD (H.264 or MPEG-2) decoder module is the same as the ones for the HD encoder module. Refer to Table-2 for the power and ground pins. Also, refer to Appendix-A for the power and ground pins on the edge connector of the MCM-1000A module.

5.4 Power Requirement and Supply Amperage

The total power at operation required by a given decoder ranges from 2 to 4 Watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail delivers only a portion of the total lower. However, the power is not evenly distributed among the rails. Table-5 lists the power

estimation by Xilinx Vivado FPGA software for each rail, at 1080p@60 resolution, and can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-5 is higher than the measured real power.

Again, the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-5.

Table-5: Power estimation for the decoder module (1080p@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	2.421	2.362	0.058
Vccaux	1.800	0.497	0.464	0.033
Vcco33	3.300	0.053	0.048	0.005
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.500	0.495	0.005
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.037	0.028	0.009
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.022	0.002	0.020

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 6 of this document. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for further details.

6.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 3 to 6 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-7 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 4k@60 resolution, which can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-7 is higher than the measured real power of the module. However, for PCB design purposes, Table-7 is sufficient. It should also be noted that the power rails 1.8v and 2.0v are generated on the module, by using some of the input power rails. Carrier board PCB designers need not to consider these two rails.

Table-7: Power estimation for the H.264 4k encoder module (4k@60 resolution)

Power Supply

Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	5.462	5.351	0.111
Vccaux	1.800	0.558	0.500	0.058
Vcco33	3.300	0.006	0.005	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.001	0.000	0.001
Vcco15	1.500	0.429	0.428	0.001
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	2.000	0.109	0.109	0.000
Vccbram	1.000	0.083	0.057	0.026
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
MGTVccaux	1.800	0.000	0.000	0.000
Vccpint	1.000	0.750	0.723	0.027
Vccpaux	1.800	0.061	0.051	0.010
Vccpll	1.800	0.019	0.016	0.003
Vcco_ddr	1.500	0.459	0.457	0.002
Vcco_mio0	1.800	0.007	0.006	0.001
Vcco_mio1	1.800	0.001	0.000	0.001
Vccadc	1.800	0.022	0.002	0.020

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 12 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for design licensing information.

Video Data 2 Chroma[1]	40	Output	AF12	3.3v	LVCMOS33
Video Data 2 Chroma[2]	50	Output	AG12	3.3v	LVCMOS33
Video Data 2 Chroma[3]	52	Output	AH12	3.3v	LVCMOS33
Video Data 2 Chroma[4]	54	Output	AH14	3.3v	LVCMOS33
Video Data 2 Chroma[5]	56	Output	AH13	3.3v	LVCMOS33
Video Data 2 Chroma[6]	58	Output	AJ14	3.3v	LVCMOS33
Video Data 2 Chroma[7]	60	Output	AJ13	3.3v	LVCMOS33
Video Data 2 Chroma[8]	59	Output	AK13	3.3v	LVCMOS33
Video Data 2 Chroma[9]	61	Output	AK12	3.3v	LVCMOS33
Video Data 3 Chroma[0]	108	Output	AJ26	3.3v	LVCMOS33
Video Data 3 Chroma[1]	110	Output	AK26	3.3v	LVCMOS33
Video Data 3 Chroma[2]	112	Output	AH26	3.3v	LVCMOS33
Video Data 3 Chroma[3]	114	Output	AH27	3.3v	LVCMOS33
Video Data 3 Chroma[4]	136	Output	AK27	3.3v	LVCMOS33
Video Data 3 Chroma[5]	138	Output	AK28	3.3v	LVCMOS33
Video Data 3 Chroma[6]	139	Output	AJ28	3.3v	LVCMOS33
Video Data 3 Chroma[7]	141	Output	AJ29	3.3v	LVCMOS33
Video Data 3 Chroma[8]	140	Output	AJ30	3.3v	LVCMOS33
Video Data 3 Chroma[9]	142	Output	AK30	3.3v	LVCMOS33
SPDIF Audio	27	Output	Y20	1.5v	LVCMOS15
Transport Stream Clock	31	Input	AA18	1.5v	LVCMOS15
Transport Stream Data Valid	33	input	AA19	1.5v	LVCMOS15
Transport Stream Data [0]	152	input	AF30	3.3v	LVCMOS33
Transport Stream Data [1]	154	input	AG30	3.3v	LVCMOS33
Transport Stream Data [2]	158	input	AE30	3.3v	LVCMOS33
Transport Stream Data [3]	160	input	AB29	3.3v	LVCMOS33
Transport Stream Data [4]	162	input	AB30	3.3v	LVCMOS33
Transport Stream Data [5]	164	input	AA27	3.3v	LVCMOS33
Transport Stream Data [6]	166	input	AA28	3.3v	LVCMOS33
Transport Stream Data [7]	120	input	AH28	3.3v	LVCMOS33
Uart_tx	90	Output	AK15	3.3v	LVCMOS33
Uart_rx	88	Input	AJ15	3.3v	LVCMOS33
Video Frame Sync Clock	80	Input	AF15	3.3v	LVCMOS33
Video Frame Sync Pause	63	Input	AC18	1.5v	LVCMOS15

7.2 Signal Formats

7.2.1 Video Clock Signal (Output)

The **Video Clock** signal (pin # 105) is the clock signal that provides the timing for the parallel luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The default is 148.5MHz for 4K@60 and 74.25MHz for 4K@30.

7.2.2 Video Data Signals (Output)

The output of the H.264 4k decoder module is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma. And, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The Video **Display Enable signal** is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

7.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

7.2.4 Decoder Control Signals (Input and output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

7.3 Power Rails of MCM-1000Z

The power rails for H.264 4K decoder for 4k@30 or 4k@60 are the same and are also the same as the H.264 4k encoder. Refer to Appendix-C for the pins of power and ground on the edge connector of the MCM-1000Z module.

7.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 3 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-10 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 4k@60 resolution, and can be used for PCB design. It should be noted that the power rails 1.8v and 2.0v are generated on the module using the input power rails. PCB designers for the carrier boards need not to consider these two rails.

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards. The VTR-4000C, discussed in Section

8. The H.265 HD Encoder Modules

To be added

9. The H.265 HD Decoder Modules

To be added

10. The H.265 4k Encoder Modules

To be added

11. The H.265 4k Decoder Modules

To be added

15. Document Revisions

Version #	Revision Date	Notes
V.1.0	10/05/2017	First release
V.1.1	19/05/2017	Minor revision
V.2.0	20/05/2017	Major revision (adding 4k)
V.2.1	05/06/2017	Minor revision

Table-A2: H.265 Video&Audio Encoder Modules (both video and audio)**:**

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-VA-H265-8b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12bits	up to 60fps	AAC or MPEG2 Layer-2

A.2 H.264 Encoder Modules

The H.264 encoder modules are based on either the on the MCM-1000A hardware. The SOC H.264 encoder IP cores are used to configure the FPGAs on the hardware modules to produce the codec modules.

Table-A3 lists the product code of the factory standard video encoder modules (video only), along with the specifications for each module. Table-A4 lists the video/audio encoder modules (both video and audio). Customers can order the encoder modules using the product code, according to the specifications required by the application.

Table-A3: H.264 Video Encoder Modules (video only without audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H264-8b-30-720-MS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-H264-8b-60-720-MS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-H264-8b-30-1080-MS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-H264-10b-30-1080-MS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	MCM-1000A
EC-V-H264-8b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-H264-10b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	MCM-1000A
EC-V-H264-8b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 8 bits	up to 30fps	no	MCM-1000Z
EC-V-H264-10b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	MCM-1000Z
EC-V-H264-8b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 8 bits	up to 60fps	no	MCM-1000Z
EC-V-H264-10b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	MCM-1000Z

A.5 MPEG-2 Decoder Modules

Table-A9 lists the standard MPEG-2 video decoder modules. Table-A10 lists the MPEG-2 video/audio decoder modules. The 10-bit precision and 60 frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A9: MPEG-2 Video Decoder Modules (video only without audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-MPEG2-8b-30-720-MS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000S
DC-V-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
DC-V-MPEG2-8b-30-1080-MS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000S
DC-V-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A

Table-A10: MPEG-2 Video&Audio Decoder Modules (both video and audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-MPEG2-8b-30-720-MS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000S
DC-V-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-V-MPEG2-8b-30-1080-MS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000S
DC-V-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A

A.6 H.264-to-H.265 Transcoder Modules

Table-A11 lists the standard H.264-to-H.265 video transcoder modules. Table-A12 lists the H.264-to-H.265 video/audio transcoder modules.

Table-A11: H.264-to-H.265 Video Transcoder Modules (video only without audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-H.264-to-H.265-8b-30-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000Z
TC-V-H.264-to-H.265-10b-30-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	no	MCM-1000Z
TC-V- H.264-to-H.265-8b-60-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000Z
TC-V- H.264-to-H.265-10b-60-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	no	MCM-1000Z
TC-V- H.264-to-H.265-8b-30-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000Z
TC-V- H.264-to-H.265-10b-30-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	no	MCM-1000Z
TC-V- H.264-to-H.265-8b-60-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000Z
TC-V- H.264-to-H.265-10b-60-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	no	MCM-1000Z

A.8 MPEG2-to-H.264 Transcoder Modules

Table-A15 lists the standard MPEG2-to-H.264 video transcoder modules, and Table-A16 lists the MPEG2-to-H.264 video/audio transcoder modules. The 60frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A15: MPEG2-to-H.264 Video Transcoder Modules (video only without audio)**:**

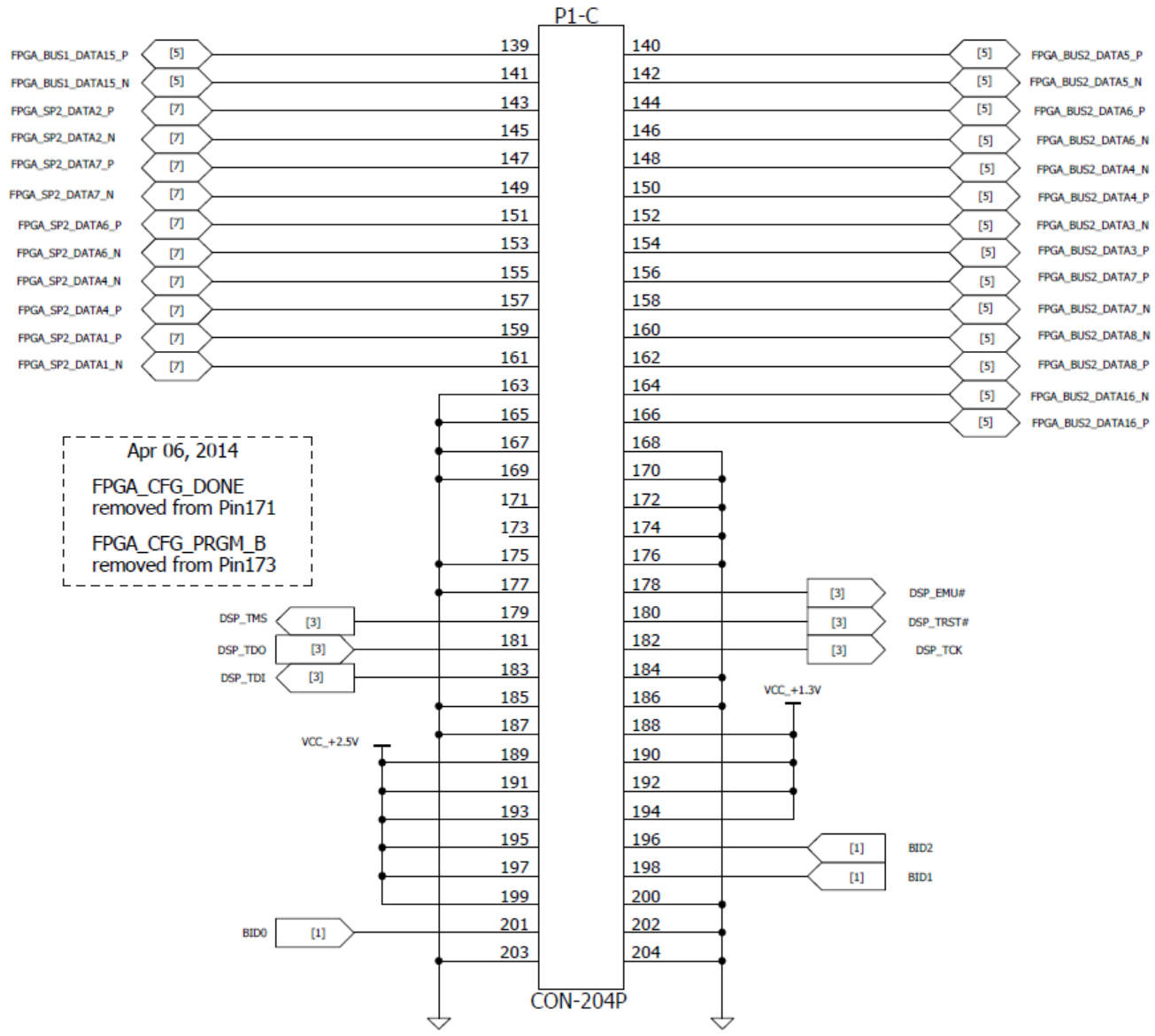
Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-MPEG2-to-H.264-8b-30-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-60-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-30-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-60-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000A

Table-A16: MPEG2-to-H.264 Video&Audio Transcoder Modules (both video and audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-VA-MPEG2-to-H.264-8b-30-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-60-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-30-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-60-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC	MCM-1000A

A.9 Non-Standard Codec Modules

The previous section provides the information on SOC's factory standard MPEG codec modules. Customers can order modules based on customer specific requirements (non-standard modules). There is a Minimum Order Quantity (MOQ) required for customized configurations. Contact SOC sales sale@soctechnologies.com for information.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FPGA_SP2_DATA6_N [7] 153
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FPGA_SP2_DATA1_N [7] 161
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154 [5] FPGA_BUS2_DATA3_P
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VCC_+1.3V
BID0 [1] 201
196 [1] BID2
198 [1] BID1
CON-204P

Appendix - C MCM-1000Z Edge Connector Schematics