



Welcome to [E-XFL.COM](http://E-XFL.COM)

## Understanding [Embedded - Microcontroller, Microprocessor, FPGA Modules](#)

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

## Applications of [Embedded - Microcontroller,](#)

### Details

|                       |                                                                                                                                                                                       |
|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status        | Discontinued at Digi-Key                                                                                                                                                              |
| Module/Board Type     | FPGA Core                                                                                                                                                                             |
| Core Processor        | Artix-7 A200T                                                                                                                                                                         |
| Co-Processor          | -                                                                                                                                                                                     |
| Speed                 | -                                                                                                                                                                                     |
| Flash Size            | 32MB                                                                                                                                                                                  |
| RAM Size              | 256KB                                                                                                                                                                                 |
| Connector Type        | SO-DIMM-204                                                                                                                                                                           |
| Size / Dimension      | 2.7" x 2.0" (68mm x 51mm)                                                                                                                                                             |
| Operating Temperature | 0°C ~ 85°C                                                                                                                                                                            |
| Purchase URL          | <a href="https://www.e-xfl.com/product-detail/soc-technologies/dc-va-h264-10b-60-1080-mxc-sl">https://www.e-xfl.com/product-detail/soc-technologies/dc-va-h264-10b-60-1080-mxc-sl</a> |

## **6. The H.264 4K Encoder Modules**

- 6.1 Pin Assignments and Pin Voltages**
- 6.2 Signal Formats**
  - 6.2.1 Clock Signals (Input, Output)**
  - 6.2.2 Video Data Signals (Input)**
  - 6.2.3 Audio Data Signals (Input)**
  - 6.2.4 TS Signals (Output)**
  - 6.2.5 Encoder Control Signals (Input and Output)**
- 6.3 Power Rails of MCM-1000Z**
- 6.4 Power Requirement and Supply Amperage**

## **7. The H.264 4K Decoder Modules**

- 7.1 Pin Assignments and Pin Voltages**
- 7.2 Signal Formats**
  - 7.2.1 Video Clock Signal (Input)**
  - 7.2.2 Video Data Signals (Output)**
  - 7.2.3 Audio Data Signals (Output)**
  - 7.2.4 TS Signals (Input)**
  - 7.2.5 Decoder Control Signals (Input and Output)**
- 7.3 Power Rails of MCM-1000Z**
- 7.4 Power Requirement and Supply Amperage**

## **8. The H.265 HD Encoder Modules**

- 8.1 Pin Assignments and Pin Voltages**
- 8.2 Signal Formats**
  - 8.2.1 Clock Signal (Input)**
  - 8.2.2 Video Data Signals (Input)**
  - 8.2.3 Audio Data Signals (Input)**
  - 8.2.4 TS Signals (Output)**
  - 8.2.5 Encoder Control Signals (Input and Output)**
- 8.3 Power Rails of MCM-1000SX**
- 8.4 Power Requirement and Supply Amperage**

## **9. The H.265 HD Decoder Modules**

- 9.1 Pin Assignments and Pin Voltages**
- 9.2 Signal Formats**
  - 9.2.1 Clock Signal (Input)**
  - 9.2.2 Video Data Signals (Output)**
  - 9.2.3 Audio Data Signals (Output)**
  - 9.2.4 TS Signals (Input)**
  - 9.2.5 Encoder Control Signals (Input and Output)**
- 9.3 Power Rails of MCM-1000SX**
- 9.4 Power Requirement and Supply Amperage**

## **10. The H.265 4K Encoder Modules**

- 10.1 Pin Assignments and Pin Voltages**
- 10.2 Signal Formats**
  - 10.2.1 Clock Signals (Input, Output)**
  - 10.2.2 Video Data Signals (Input)**
  - 10.2.3 Audio Data Signals (Input)**
  - 10.2.4 TS Signals (Output)**
  - 10.2.5 Decoder Control Signals (Input and Output)**
- 10.3 Power Rails of MCM-1000SX**
- 10.4 Power Requirement and Supply Amperage**

## **11. The H.265 4K Decoder Modules**

- 11.1 Pin Assignments and Pin Voltages**
- 11.2 Signal Formats**
  - 11.2.1 Clock Signals (Input, Output)**
  - 11.2.2 Video Data Signals (Output)**
  - 11.2.3 Audio Data Signals (Output)**
  - 11.2.4 TS Signals (Input)**
  - 11.2.5 Decoder Control Signals (Input and Output)**
- 11.3 Power Rails of MCM-1000SX**
- 11.4 Power Requirement and Supply Amperage**

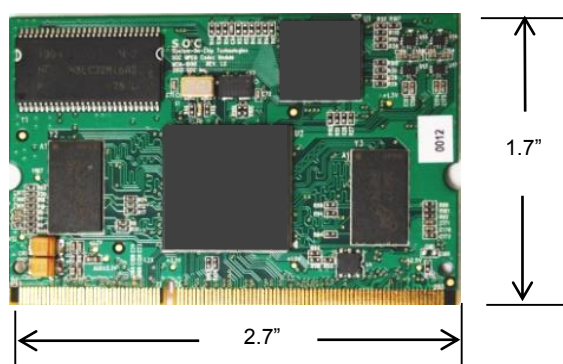


Fig. 2. Dimension of MCM-1000S

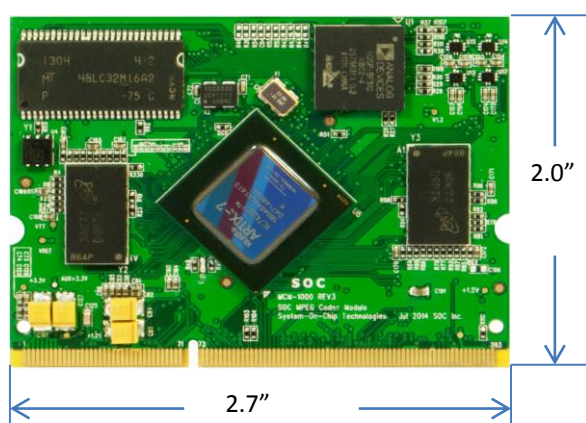


Fig. 3. Dimension of MCM-1000A

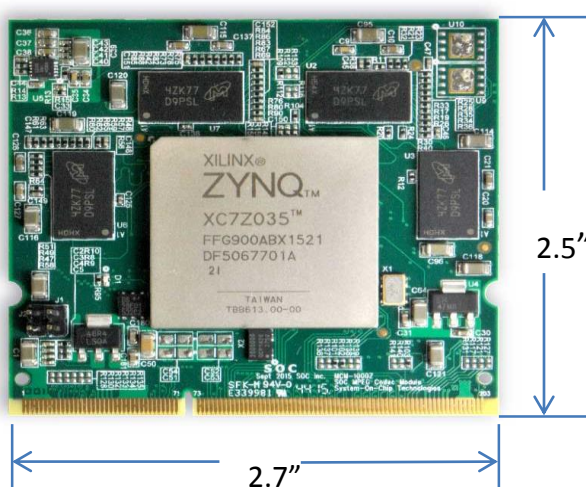


Fig. 4. Dimension of MCM-1000Z

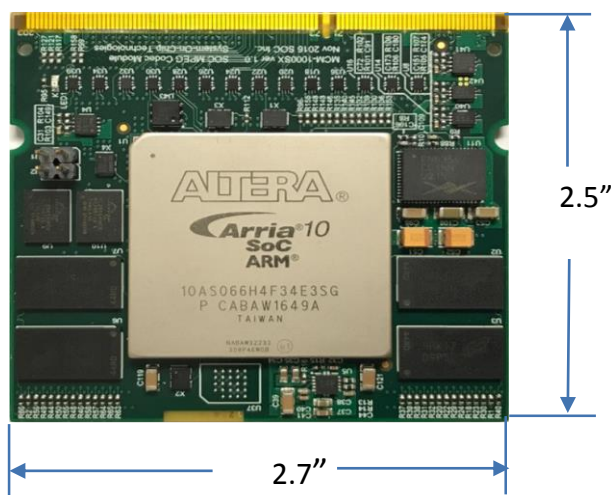


Fig. 5. Dimension of MCM-1000SX

## 2. Connecting the Module to a User PCB

The MCM-1000S/A/Z/SX modules have identical edge pins that are compatible with standard DDR3 SODIMM connectors. The following off-the-shelf DDR3 SODIMM connectors can be used to connect the SOC codec modules onto a user PCB:

1. MM80-204B1-1
2. MM80-204B1-1E
3. AS0A621-U2SN-7F
4. AS0A621-H2S6-7H

Fig. 6 shows a photo of a standard 204 pin DDR3 SODIMM PCB connector. Refer to the datasheet of the connector used for the physical dimension and PCB design requirements.



Fig. 6 A photo of the standard 204 pin DDR3 SODIMM connector

### 3. Overview SOC Standard Codec Modules

Each of the above described SOMs: the **MCM-1000S** (based on Spatran-6 FPGA), **MCM-1000A** (based on Artix-7 FPGA), **MCM-1000Z** (based on Zynq-7 FPGAs), and **MCM-1000SX** (based on Altera Arria-10 FPGAs); can be configured into different products by down-loading the desired firmware. At SOC, we produce encoder, decoder, transcoder, and multi-channel encoder or decoder SOMs for video compressions, by down-loading **SOC MPEG Codec IP** cores onto the modules.

The standard encoder modules: H.265, H.264, and MPEG-2, take raw video and audio as input and output TS streams, via the edge pins of the modules, as shown in Fig. 7. The standard decoder modules: H.265, H.264, and MPEG-2, take TS stream as inputs and output decoded video and audio, via the edge pins of the modules, as shown in Fig. 8. There are also control signal pins, to allow the user control of the encoder or decoder.

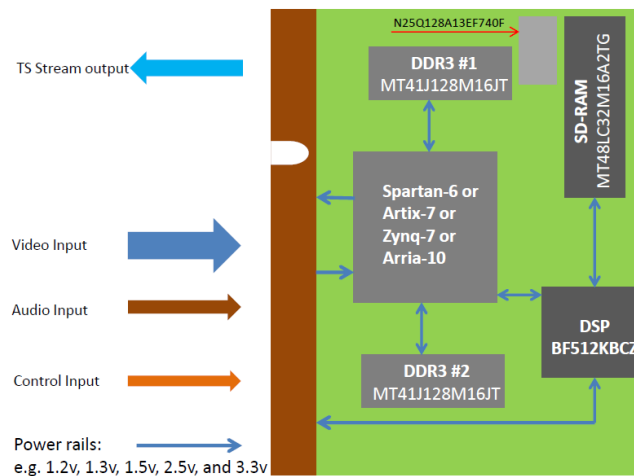


Fig. 7 SOC Standard encoder modules (H.265, H.264, or MPEG-2)

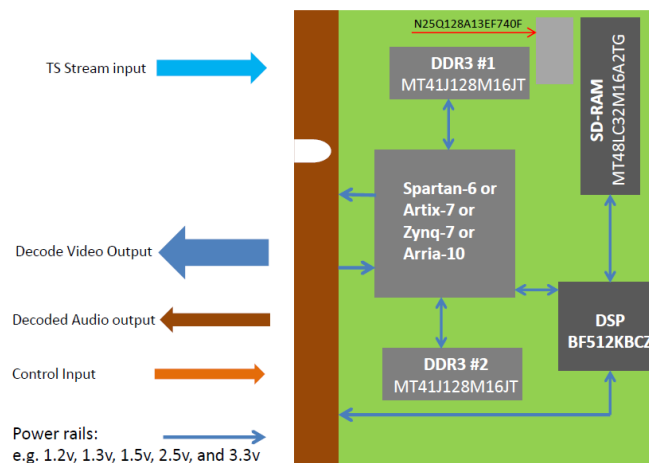


Fig. 8 SOC Standard decoder modules (H.265, H.264, or MPEG-2)

**Appendix-A** provides the details of the Standard Codec Modules, including the product tables which list the product codes along with the specifications. Customers can order the modules according the specifications required by using the corresponding product code.

The pin assignments, pin voltages, and signal formats for standard encoder and decoder modules are detailed respectively in this Datasheet in the following sections:

- Section 4: The H.264 (and MPEG-2) HD Encoder Modules
- Section 5: The H.264 (and MPEG-2) HD Decoder Modules
- Section 6: The H.264 4k Encoder Modules
- Section 7: The H.264 4k Decoder Modules
- Section 8: The H.265 HD Encoder Modules
- Section 9: The H.265 HD Decoder Modules (will be available soon)
- Section 10: The H.265 4k Encoder Modules
- Section 11: The H.265 4k Encoder Modules (will be available soon)

*It should be noted that not all of the modules listed in Appendix-A are discussed in this Datasheet. Pin assignments and electrical properties for the modules that are not provided in the document, will be provided on demand basis.*

SOC also offers customized modules according to customer requirements, such as Transcoder modules, Multi-channel encoder or decoder modules, and modules with non-standard I/Os. For details, contact SOC sales at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com)

One of the popular extended versions of the standard codec modules is the –NET version which integrates the SOC low latency network stack (UDP/IP over Ethernet) into the encoder or decoder module. The pin assignments, pin voltages, and signal formats for the –NET version encoder and decoder modules are detailed in the document:

**Datasheet – Encoder and Decoder Modules – NET Version**

## 4. The H.264 (and MPEG-2) HD Encoder Modules

### 4.1 Pin Assignments and Pin Voltages

The HD encoder modules for H.264 and MPEG-2 have the same pin assignments and electrical properties. The hardware module for HD resolution uses the MCM-1000A (the Artix-7 A200T FPGA), the hardware module MCM-1000Z is used for 4k resolutions (the Zynq-7035 for 4k@30, Zynq-7045 for 4k@60).

This Section provides the pin assignments and electrical properties for HD encoder (H.264, or MPEG-2) module which is based on the MCM-1000A. Table-1 lists the pin assignments and the pin voltages.

The schematics of MCM-1000A edge connector are attached in Appendix-B of this document, which shows the pin numbers for data, clock, control, and power. It should be noted that the encoder module uses only some of the edge pins, and not all of the edge pins are used.

Table-1 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Artix-7 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

**Table 1: HD Encoder Module (based on MCM-1000A) Pin Assignment and Pin Voltages**

| Description           | MCM-1000A Edge Connector Pin # | Direction | FPGA Pin # | Voltage | IO Standard |
|-----------------------|--------------------------------|-----------|------------|---------|-------------|
| External Reset        | 121                            | Input     | W21        | 3.3v    | LVC MOS33   |
| Video Clock           | 105                            | Input     | Y11        | 3.3v    | LVC MOS33   |
| Video Horizontal Sync | 146                            | Input     | W16        | 3.3v    | LVC MOS33   |
| Video Vertical Sync   | 148                            | Input     | V15        | 3.3v    | LVC MOS33   |
| Video Display Enable  | 150                            | Input     | U15        | 3.3v    | LVC MOS33   |
| Video Data Luma[0]    | 50                             | Input     | W14        | 3.3v    | LVC MOS33   |
| Video Data Luma[1]    | 52                             | Input     | Y14        | 3.3v    | LVC MOS33   |
| Video Data Luma[2]    | 58                             | Input     | V10        | 3.3v    | LVC MOS33   |
| Video Data Luma[3]    | 59                             | Input     | Y13        | 3.3v    | LVC MOS33   |
| Video Data Luma[4]    | 60                             | Input     | W10        | 3.3v    | LVC MOS33   |
| Video Data Luma[5]    | 61                             | Input     | AA14       | 3.3v    | LVC MOS33   |
| Video Data Luma[6]    | 80                             | Input     | AB13       | 3.3v    | LVC MOS33   |
| Video Data Luma[7]    | 82                             | Input     | AA13       | 3.3v    | LVC MOS33   |
| Video Data Luma[8]    | 84                             | Input     | AB17       | 3.3v    | LVC MOS33   |
| Video Data Luma[9]    | 86                             | Input     | AB16       | 3.3v    | LVC MOS33   |
| Video Data Chroma[0]  | 92                             | Input     | AA15       | 3.3v    | LVC MOS33   |
| Video Data Chroma[1]  | 94                             | Input     | AB15       | 3.3v    | LVC MOS33   |
| Video Data Chroma[2]  | 96                             | Input     | AB12       | 3.3v    | LVC MOS33   |
| Video Data Chroma[3]  | 98                             | Input     | AB11       | 3.3v    | LVC MOS33   |
| Video Data Chroma[4]  | 107                            | Input     | Y12        | 3.3v    | LVC MOS33   |
| Video Data Chroma[5]  | 108                            | Input     | W12        | 3.3v    | LVC MOS33   |
| Video Data Chroma[6]  | 110                            | Input     | Y17        | 3.3v    | LVC MOS33   |
| Video Data Chroma[7]  | 140                            | Input     | T14        | 3.3v    | LVC MOS33   |
| Video Data Chroma[8]  | 142                            | Input     | T15        | 3.3v    | LVC MOS33   |
| Video Data Chroma[9]  | 144                            | Input     | W15        | 3.3v    | LVC MOS33   |
| SPDIF Audio           | 109                            | Input     | Y21        | 3.3v    | LVC MOS33   |



#### 4.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** (pin # 69) is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

#### 4.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]**; along with the Transport Stream output data clock **Transport Stream Clock** (pin # 113). The frequency of the Transport Stream Data clock is 27MHz.

**Transport Stream Buffer Ready** (pin # 118) and **Transport Stream Data Valid** (pin # 135) are the signals to inform the user side to take over the signals.

#### 4.2.5 Encoder Control Signals (Input and Output)

**Uart\_rx** and **Uart\_tx** are the API pins for controlling the operations of the encoder. **Uart\_rx** receives the command from external control device. **Uart\_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the [Encoder API User Manual](#) for more details.

An external reset pin (pin # 121) is available. This pin allows the user to reset the encoder when necessary. A high signal will trigger a reset. The reset signal should be maintained at low when in normal operation mode.

### 4.3 Power Rails of MCM-1000A

Table-2 lists the power and ground pins. Refer to Appendix-A for the pins of power and ground on the edge connector of the MCM-1000A module.

**Table-2: MCM-1000A Power and Ground Pins**

| MCM-1000S Connector Pin                 | Voltage |
|-----------------------------------------|---------|
| 1,3,5,7,9,11,13,15                      | 3.3V    |
| 10,12,14,16                             | 1.2V    |
| 22,24,26,28,30,32                       | 1.5V    |
| 189,191,193,195,197,199                 | 2.5V    |
| 188,190,192,194                         | 1.3V    |
| 43,45,47,49,51,53,55,57                 | 1.0V    |
| 2,4,6,8,18,20,34,36,42,44,62,72         | Ground  |
| 17,35,37,39,41,71                       | Ground  |
| 73,75,129                               | Ground  |
| 74                                      | Ground  |
| 163,165,167,169,175,177,185,187,203     | Ground  |
| 168,170,172,174,176,184,186,200,202,204 | Ground  |

#### 4.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 2 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-3 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 1080p@60 resolution, which can be used as a reference for PCB design. It should be noted that the measured real power consumption is about 20% lower than the estimated power consumption.

It should be noted that the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-2, as the 1.8v is generated on the module.

**Table-3: Power estimation for the encoder module (1080p@60 resolution)**

| Power Supply  |             |           |             |            |
|---------------|-------------|-----------|-------------|------------|
| Supply Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) |
| Vccint        | 1.000       | 3.792     | 3.723       | 0.069      |
| Vccaux        | 1.800       | 0.454     | 0.421       | 0.034      |
| Vcco33        | 3.300       | 0.013     | 0.008       | 0.005      |
| Vcco25        | 2.500       | 0.000     | 0.000       | 0.000      |
| Vcco18        | 1.800       | 0.000     | 0.000       | 0.000      |
| Vcco15        | 1.500       | 0.499     | 0.494       | 0.005      |
| Vcco135       | 1.350       | 0.000     | 0.000       | 0.000      |
| Vcco12        | 1.200       | 0.000     | 0.000       | 0.000      |
| Vccaux_io     | 1.800       | 0.000     | 0.000       | 0.000      |
| Vccbram       | 1.000       | 0.063     | 0.052       | 0.011      |
| MGTAVcc       | 1.000       | 0.000     | 0.000       | 0.000      |
| MGTAVtt       | 1.200       | 0.000     | 0.000       | 0.000      |
| Vccadc        | 1.800       | 0.022     | 0.002       | 0.020      |

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 12 of this document. The reference designs provide not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing details.

## 5. The H.264 (and MPEG-2) HD Decoder Modules

### 5.1 Pin Assignments and Pin Voltages

The decoders for H.264 and MPEG-2 have the same pin assignment. The module for HD resolution decoding uses the MCM-1000A (with the Artix-7 A200T FPGA which is the same as the one used for the HD Encoder). The module MCM-1000Z is used for 4k decoding (the Zynq-7035 for 4k@30, Zynq-7045 for 4k@60).

This section details the pin assignments and pin voltages for the HD decoder (H.264, and MPEG-2) modules. Table-4 shows the pin assignments and the pin voltages.

The schematics of MCM-1000A edge connector are attached in Appendix-B of this document. Appendix-B shows the pin numbers for data, clock, control, and power, which are connected to the FPGA (Artix-7 XC7A200T). It should be noted that the decoder module uses only some of the available edge pins that are connected to the FPGA (some of the pins are not used).

It should also be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

**Table-4: HD Decoder Module (based on MCM-1000A) Pin Assignment**

| Description             | MCM-1000A Edge Connector Pin # | Direction | FPGA Pin # | Voltage | IO Standard |
|-------------------------|--------------------------------|-----------|------------|---------|-------------|
| External Reset          | 121                            | Input     | W21        | 3.3v    | LVC MOS33   |
| Decoder Clock           | 115                            | Input     | U20        | 3.3v    | LVC MOS33   |
| Video Clock             | 105                            | Output    | Y11        | 3.3v    | LVC MOS33   |
| Video Horizontal Sync   | 146                            | Output    | W16        | 3.3v    | LVC MOS33   |
| Video Vertical Sync     | 148                            | Output    | V15        | 3.3v    | LVC MOS33   |
| Video Display Enable    | 150                            | Output    | U15        | 3.3v    | LVC MOS33   |
| Video Data Luma[0]      | 50                             | Output    | W14        | 3.3v    | LVC MOS33   |
| Video Data Luma[1]      | 52                             | Output    | Y14        | 3.3v    | LVC MOS33   |
| Video Data Luma[2]      | 58                             | Output    | V10        | 3.3v    | LVC MOS33   |
| Video Data Luma[3]      | 59                             | Output    | Y13        | 3.3v    | LVC MOS33   |
| Video Data Luma[4]      | 60                             | Output    | W10        | 3.3v    | LVC MOS33   |
| Video Data Luma[5]      | 61                             | Output    | AA14       | 3.3v    | LVC MOS33   |
| Video Data Luma[6]      | 80                             | Output    | AB13       | 3.3v    | LVC MOS33   |
| Video Data Luma[7]      | 82                             | Output    | AA13       | 3.3v    | LVC MOS33   |
| Video Data Luma[8]      | 84                             | Output    | AB17       | 3.3v    | LVC MOS33   |
| Video Data Luma[9]      | 86                             | Output    | AB16       | 3.3v    | LVC MOS33   |
| Video Data Chroma[0]    | 92                             | Output    | AA15       | 3.3v    | LVC MOS33   |
| Video Data Chroma[1]    | 94                             | Output    | AB15       | 3.3v    | LVC MOS33   |
| Video Data Chroma[2]    | 96                             | Output    | AB12       | 3.3v    | LVC MOS33   |
| Video Data Chroma[3]    | 98                             | Output    | AB11       | 3.3v    | LVC MOS33   |
| Video Data Chroma[4]    | 107                            | Output    | Y12        | 3.3v    | LVC MOS33   |
| Video Data Chroma[5]    | 108                            | Output    | W12        | 3.3v    | LVC MOS33   |
| Video Data Chroma[6]    | 110                            | Output    | Y17        | 3.3v    | LVC MOS33   |
| Video Data Chroma[7]    | 140                            | Output    | T14        | 3.3v    | LVC MOS33   |
| Video Data Chroma[8]    | 142                            | Output    | T15        | 3.3v    | LVC MOS33   |
| Video Data Chroma[9]    | 144                            | Output    | W15        | 3.3v    | LVC MOS33   |
| Video Frame Sync Relock | 56                             | Input     | AB21       | 3.3v    | LVC MOS33   |

|                                         |     |        |      |      |           |
|-----------------------------------------|-----|--------|------|------|-----------|
| SPDIF Audio                             | 109 | Output | Y21  | 3.3v | LVC MOS33 |
| Transport Stream Clock ( <b>27MHz</b> ) | 93  | Output | Y18  | 3.3v | LVC MOS33 |
| Transport Stream Data Valid             | 106 | Output | R17  | 3.3v | LVC MOS33 |
| Transport Stream Data[0]                | 77  | Output | N13  | 3.3v | LVC MOS33 |
| Transport Stream Data[1]                | 79  | Output | N14  | 3.3v | LVC MOS33 |
| Transport Stream Data[2]                | 81  | Output | R18  | 3.3v | LVC MOS33 |
| Transport Stream Data[3]                | 83  | Output | T18  | 3.3v | LVC MOS33 |
| Transport Stream Data[4]                | 85  | Output | U17  | 3.3v | LVC MOS33 |
| Transport Stream Data[5]                | 87  | Output | U18  | 3.3v | LVC MOS33 |
| Transport Stream Data[6]                | 89  | Output | AB18 | 3.3v | LVC MOS33 |
| Transport Stream Data[7]                | 91  | Output | AA18 | 3.3v | LVC MOS33 |
| Uart_tx                                 | 90  | Output | AA16 | 3.3v | LVC MOS33 |
| Uart_rx                                 | 88  | Input  | Y16  | 3.3v | LVC MOS33 |

## 5.2 Signal Formats

### 5.2.1 Clock Signals

The **Decoder Clock** signal (pin # 115) is an input clock for driving the decoder engine. The default frequency is **27MHz**. However, when an SDI port on the carrier board is used to send out the decoded video data, the SDI clock can be connected to the **Decoder Clock**. This will automatically synchronize the decoder outputs with the SDI interface.

The SDI clock frequencies are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

The **Video Clock** signal (pin # 105) is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

4. 27MHz, for SD resolution
5. 74.25MHz, for 720@60 and 1080@30
6. 148.5MHz, for 1080@60.

### 5.2.2 Video Data Signals (Output)

The output of the HD decoder module (H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma and 10 lines. And, **Video Data Chroma[0]**

## 6. The H.264 4k Encoder Modules

### 6.1 Pin Assignments and Pin Voltages

The modules for 4K resolution uses the MCM-1000Z hardware, with the MCM-1000Z35 (Zynq-7035 FPGA) for 4k@30 and MCM-1000Z45 (Zynq-7045 FPGA) for 4k@60. The pin assignment and electrical properties are the same for MCM-1000Z35 and MCM-1000Z45.

Table-6 lists the pin assignments and the pin voltages for the 4K encoder modules based on the MCM-1000Z (MCM-1000Z35 and MCM-1000Z45 are the same).

The schematics of MCM-1000Z edge connector are attached in Appendix-C of this document, which shows the pin numbers for data, clock, control, and power.

Table-6 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

**Table-6: 4K Encoder Module (based on MCM-1000Z) Pin Assignment and Pin Voltages**

| Description           | MCM-1000Z Edge Connector Pin # | Direction | FPGA Pin # | Voltage | IO Standard |
|-----------------------|--------------------------------|-----------|------------|---------|-------------|
| PS Soft Reset B       | 156                            | Input     | B19        | 3.3V    | LVCN0533    |
| Video Clock 0         | 63                             | Input     | AC18       | 1.5v    | LVCN0515    |
| Video Clock 1         | 80                             | Input     | AF15       | 3.3v    | LVCN0533    |
| Video Clock 2         | 144                            | Input     | AE28       | 3.3v    | LVCN0533    |
| Video Clock 3         | 105                            | Input     | AG21       | 3.3v    | LVCN0533    |
| Video Horizontal Sync | 133                            | Input     | W24        | 1.5v    | LVCN0515    |
| Video Vertical Sync   | 113                            | Input     | AF22       | 3.3v    | LVCN0533    |
| Video Display Enable  | 67                             | Input     | AD18       | 1.5v    | LVCN0515    |
| Video Data 0 Luma[0]  | 135                            | Input     | W25        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[1]  | 137                            | Input     | W26        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[2]  | 116                            | Input     | V27        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[3]  | 118                            | Input     | W28        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[4]  | 124                            | Input     | W29        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[5]  | 126                            | Input     | W30        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[6]  | 128                            | Input     | V28        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[7]  | 130                            | Input     | V29        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[8]  | 132                            | Input     | T30        | 1.5v    | LVCN0515    |
| Video Data 0 Luma[9]  | 134                            | Input     | U30        | 1.5v    | LVCN0515    |
| Video Data 1 Luma[0]  | 117                            | Input     | AG22       | 3.3v    | LVCN0533    |
| Video Data 1 Luma[1]  | 119                            | Input     | AH22       | 3.3v    | LVCN0533    |
| Video Data 1 Luma[2]  | 121                            | Input     | AJ21       | 3.3v    | LVCN0533    |
| Video Data 1 Luma[3]  | 123                            | Input     | AK21       | 3.3v    | LVCN0533    |

## 6.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 3 to 6 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-7 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 4k@60 resolution, which can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-7 is higher than the measured real power of the module. However, for PCB design purposes, Table-7 is sufficient. It should also be noted that the power rails 1.8v and 2.0v are generated on the module, by using some of the input power rails. Carrier board PCB designers need not to consider these two rails.

**Table-7: Power estimation for the H.264 4k encoder module (4k@60 resolution)**

| Power Supply  |             |           |             |            |
|---------------|-------------|-----------|-------------|------------|
| Supply Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) |
| Vccint        | 1.000       | 5.462     | 5.351       | 0.111      |
| Vccaux        | 1.800       | 0.558     | 0.500       | 0.058      |
| Vcco33        | 3.300       | 0.006     | 0.005       | 0.001      |
| Vcco25        | 2.500       | 0.000     | 0.000       | 0.000      |
| Vcco18        | 1.800       | 0.001     | 0.000       | 0.001      |
| Vcco15        | 1.500       | 0.429     | 0.428       | 0.001      |
| Vcco135       | 1.350       | 0.000     | 0.000       | 0.000      |
| Vcco12        | 1.200       | 0.000     | 0.000       | 0.000      |
| Vccaux_io     | 2.000       | 0.109     | 0.109       | 0.000      |
| Vccbram       | 1.000       | 0.083     | 0.057       | 0.026      |
| MGTAVcc       | 1.000       | 0.000     | 0.000       | 0.000      |
| MGTAVtt       | 1.200       | 0.000     | 0.000       | 0.000      |
| MGTVccaux     | 1.800       | 0.000     | 0.000       | 0.000      |
| Vccpint       | 1.000       | 0.750     | 0.723       | 0.027      |
| Vccpaux       | 1.800       | 0.061     | 0.051       | 0.010      |
| Vccpll        | 1.800       | 0.019     | 0.016       | 0.003      |
| Vcco_ddr      | 1.500       | 0.459     | 0.457       | 0.002      |
| Vcco_mio0     | 1.800       | 0.007     | 0.006       | 0.001      |
| Vcco_mio1     | 1.800       | 0.001     | 0.000       | 0.001      |
| Vccadc        | 1.800       | 0.022     | 0.002       | 0.020      |

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 12 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for design licensing information.

|                        |     |        |      |      |           |
|------------------------|-----|--------|------|------|-----------|
| Video Data 1 Luma[8]   | 96  | Output | AG24 | 3.3v | LVC MOS33 |
| Video Data 1 Luma[9]   | 98  | Output | AG25 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[0]   | 77  | Output | AJ16 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[1]   | 79  | Output | AK16 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[2]   | 81  | Output | AH17 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[3]   | 83  | Output | AH16 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[4]   | 85  | Output | AH18 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[5]   | 87  | Output | AJ18 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[6]   | 78  | Output | AF13 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[7]   | 82  | Output | AG15 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[8]   | 84  | Output | AG17 | 3.3v | LVC MOS33 |
| Video Data 2 Luma[9]   | 86  | Output | AG16 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[0]   | 107 | Output | AH21 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[1]   | 122 | Output | AH29 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[2]   | 115 | Output | AE22 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[3]   | 146 | Output | AF28 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[4]   | 148 | Output | AF29 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[5]   | 150 | Output | AG29 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[6]   | 100 | Output | AH23 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[7]   | 102 | Output | AH24 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[8]   | 104 | Output | AJ25 | 3.3v | LVC MOS33 |
| Video Data 3 Luma[9]   | 106 | Output | AK25 | 3.3v | LVC MOS33 |
| Video Data 0 Chroma[0] | 143 | Output | T29  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[1] | 145 | Output | U29  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[2] | 147 | Output | R28  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[3] | 149 | Output | T28  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[4] | 151 | Output | P30  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[5] | 153 | Output | R30  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[6] | 155 | Output | N29  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[7] | 157 | Output | P29  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[8] | 159 | Output | N28  | 1.5v | LVC MOS15 |
| Video Data 0 Chroma[9] | 161 | Output | P28  | 1.5v | LVC MOS15 |
| Video Data 1 Chroma[0] | 89  | Output | AK17 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[1] | 91  | Output | AK18 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[2] | 93  | Output | AF19 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[3] | 95  | Output | AG19 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[4] | 97  | Output | AH19 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[5] | 99  | Output | AJ19 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[6] | 101 | Output | AF20 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[7] | 103 | Output | AG20 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[8] | 109 | Output | AJ20 | 3.3v | LVC MOS33 |
| Video Data 1 Chroma[9] | 111 | Output | AK20 | 3.3v | LVC MOS33 |
| Video Data 2 Chroma[0] | 38  | Output | AE12 | 3.3v | LVC MOS33 |

6 of this document, is for 4k resolution. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: [sales@soctechnologies.com](mailto:sales@soctechnologies.com) for further details.

**Table-10: Power estimation for the decoder module (4K@60 resolution)**

| Power Supply  |             |           |             |            |
|---------------|-------------|-----------|-------------|------------|
| Supply Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) |
| Vccint        | 1.000       | 4.786     | 4.682       | 0.104      |
| Vccaux        | 1.800       | 0.692     | 0.634       | 0.058      |
| Vcco33        | 3.300       | 0.007     | 0.006       | 0.001      |
| Vcco25        | 2.500       | 0.000     | 0.000       | 0.000      |
| Vcco18        | 1.800       | 0.001     | 0.000       | 0.001      |
| Vcco15        | 1.500       | 0.429     | 0.428       | 0.001      |
| Vcco135       | 1.350       | 0.000     | 0.000       | 0.000      |
| Vcco12        | 1.200       | 0.000     | 0.000       | 0.000      |
| Vccaux_io     | 2.000       | 0.109     | 0.109       | 0.000      |
| Vccbram       | 1.000       | 0.093     | 0.074       | 0.019      |
| MGTAVcc       | 1.000       | 0.000     | 0.000       | 0.000      |
| MGTAVtt       | 1.200       | 0.000     | 0.000       | 0.000      |
| MGTVccaux     | 1.800       | 0.000     | 0.000       | 0.000      |
| Vccpint       | 1.000       | 0.750     | 0.723       | 0.026      |
| Vccpaux       | 1.800       | 0.061     | 0.051       | 0.010      |
| Vccpll        | 1.800       | 0.019     | 0.016       | 0.003      |
| Vcco_ddr      | 1.500       | 0.459     | 0.457       | 0.002      |
| Vcco_mio0     | 1.800       | 0.007     | 0.006       | 0.001      |
| Vcco_mio1     | 1.800       | 0.001     | 0.000       | 0.001      |
| Vccadc        | 1.800       | 0.022     | 0.002       | 0.020      |



## **8. The H.265 HD Encoder Modules**

To be added

## **9. The H.265 HD Decoder Modules**

To be added

## **10. The H.265 4k Encoder Modules**

To be added

## **11. The H.265 4k Decoder Modules**

To be added

## 12.2 VTR-4000C Evaluation Board

Fig. 12 shows the top view of the VTR-4000C board. Major components and I/O ports are marked in the figure. Refer to the [User Guide of VTR-4000C](#) for further details.

SOC licenses the Schematics of VTR-4000C to the customers that have purchased encoder (or decoder) Modules. Firmware of the VTR-4000C, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, [sales@soctechnologies.com](mailto:sales@soctechnologies.com), for details.

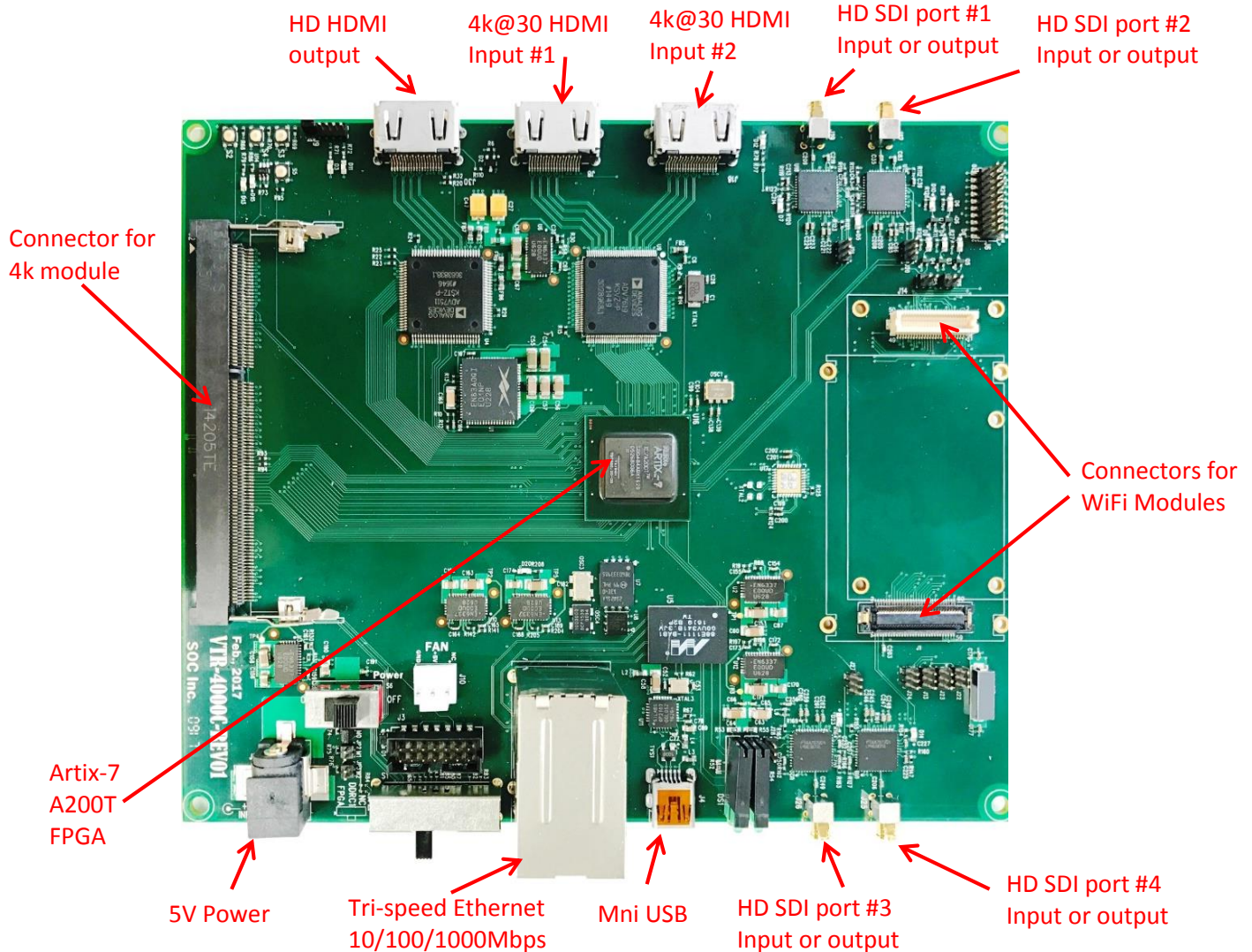


Fig. 12. VTR-4000C evaluation board top view

**Table-A2: H.265 Video&Audio Encoder Modules** (both video and audio):

| Product #                | Specifications |               |               |             |               |             |                      |
|--------------------------|----------------|---------------|---------------|-------------|---------------|-------------|----------------------|
|                          | Standard       | Profile       | Resolution    | Chroma      | Precision     | Frame Rate  | Audio                |
| EC-VA-H265-8b-30-1080-M  | H.265          | Main 4:2:2 12 | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 30fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-10b-30-1080-M | H.265          | Main 4:2:2 12 | up to 1080i/p | 4:2:0/4:2:2 | up to 10 bits | up to 30fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-12b-30-1080-M | H.265          | Main 4:2:2 12 | up to 1080i/p | 4:2:0/4:2:2 | up to 12 bits | up to 30fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-8b-60-1080-M  | H.265          | Main 4:2:2 12 | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 60fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-10b-60-1080-M | H.265          | Main 4:2:2 12 | up to 1080i/p | 4:2:0/4:2:2 | up to 10 bits | up to 60fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-12b-60-1080-M | H.265          | Main 4:2:2 12 | up to 1080i/p | 4:2:0/4:2:2 | up to 12 bits | up to 60fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-8b-30-4k-M    | H.265          | Main 4:2:2 12 | 4k/UHD        | 4:2:0/4:2:2 | 8 bits        | up to 30fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-10b-30-4k-M   | H.265          | Main 4:2:2 12 | 4k/UHD        | 4:2:0/4:2:2 | up to 10 bits | up to 30fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-12b-30-4k-M   | H.265          | Main 4:2:2 12 | 4k/UHD        | 4:2:0/4:2:2 | up to 12 bits | up to 30fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-8b-60-4k-M    | H.265          | Main 4:2:2 12 | 4k/UHD        | 4:2:0/4:2:2 | 8 bits        | up to 60fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-10b-60-4k-M   | H.265          | Main 4:2:2 12 | 4k/UHD        | 4:2:0/4:2:2 | up to 10 bits | up to 60fps | AAC or MPEG2 Layer-2 |
| EC-VA-H265-12b-60-4k-M   | H.265          | Main 4:2:2 12 | 4k/UHD        | 4:2:0/4:2:2 | up to 12bits  | up to 60fps | AAC or MPEG2 Layer-2 |

## A.2 H.264 Encoder Modules

The H.264 encoder modules are based on either the on the MCM-1000A hardware. The SOC H.264 encoder IP cores are used to configure the FPGAs on the hardware modules to produce the codec modules.

Table-A3 lists the product code of the factory standard video encoder modules (video only), along with the specifications for each module. Table-A4 lists the video/audio encoder modules (both video and audio). Customers can order the encoder modules using the product code, according to the specifications required by the application.

**Table-A3: H.264 Video Encoder Modules** (video only without audio):

| Product #                | Specifications |            |               |             |               |             |       | Hardware  |
|--------------------------|----------------|------------|---------------|-------------|---------------|-------------|-------|-----------|
|                          | Standard       | Profile    | Resolution    | Chroma      | Precision     | Frame Rate  | Audio |           |
| EC-V-H264-8b-30-720-MS   | H.264          | up to High | up to 720i/p  | 4:2:0/4:2:2 | 8 bits        | up to 30fps | no    | MCM-1000A |
| EC-V-H264-8b-60-720-MS   | H.264          | up to High | up to 720i/p  | 4:2:0/4:2:2 | 8 bits        | up to 60fps | no    | MCM-1000A |
| EC-V-H264-8b-30-1080-MS  | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 30fps | no    | MCM-1000A |
| EC-V-H264-10b-30-1080-MS | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | up to 10 bits | up to 30fps | no    | MCM-1000A |
| EC-V-H264-8b-60-1080-MA  | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 60fps | no    | MCM-1000A |
| EC-V-H264-10b-60-1080-MA | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | up to 10 bits | up to 60fps | no    | MCM-1000A |
| EC-V-H264-8b-30-4k-MZ    | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | up to 8 bits  | up to 30fps | no    | MCM-1000Z |
| EC-V-H264-10b-30-4k-MZ   | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | up to 10 bits | up to 30fps | no    | MCM-1000Z |
| EC-V-H264-8b-60-4k-MZ    | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | up to 8 bits  | up to 60fps | no    | MCM-1000Z |
| EC-V-H264-10b-60-4k-MZ   | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | up to 10 bits | up to 60fps | no    | MCM-1000Z |

**Table-A4: H.264 Video&Audio Encoder Modules** (both video and audio):

| Product #                 | Specifications |            |               |             |               |             |               | Hardware  |
|---------------------------|----------------|------------|---------------|-------------|---------------|-------------|---------------|-----------|
|                           | Standard       | Profile    | Resolution    | Chroma      | Precision     | Frame Rate  | Audio         |           |
| EC-VA-H264-8b-30-720-MS   | H.264          | up to High | up to 720i/p  | 4:2:0/4:2:2 | 8 bits        | up to 30fps | AAC/MPEG2 L-2 | MCM-1000A |
| EC-VA-H264-8b-60-720-MS   | H.264          | up to High | up to 720i/p  | 4:2:0/4:2:2 | 8 bits        | up to 60fps | AAC/MPEG2 L-2 | MCM-1000A |
| EC-VA-H264-8b-30-1080-MS  | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 30fps | AAC/MPEG2 L-2 | MCM-1000A |
| EC-VA-H264-10b-30-1080-MS | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | up to 10bits  | up to 30fps | AAC/MPEG2 L-2 | MCM-1000A |
| EC-VA-H264-8b-60-1080-MA  | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 60fps | AAC/MPEG2 L-2 | MCM-1000A |
| EC-VA-H264-10b-60-1080-MA | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | up to 10 bits | up to 60fps | AAC/MPEG2 L-2 | MCM-1000A |
| EC-VA-H264-8b-30-4k-MZ    | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 8 bits        | up to 30fps | AAC/MPEG2 L-2 | MCM-1000Z |
| EC-VA-H264-10b-30-4k-MZ   | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 10 bits       | up to 30fps | AAC/MPEG2 L-2 | MCM-1000Z |
| EC-VA-H264-8b-60-4k-MZ    | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 8 bits        | up to 60fps | AAC/MPEG2 L-2 | MCM-1000Z |
| EC-VA-H264-10b-60-4k-MZ   | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 10 bits       | up to 60fps | AAC/MPEG2 L-2 | MCM-1000Z |

### A.3 H.264 Decoder Modules

Hardware platform MCM-1000A is used for the H.264 HD decoders. Table-A5 lists the factory standard H.264 video decoder modules (video only), along with the product code and specifications. Table-A6 lists the factory standard H.264 video and audio decoder modules, product code, specifications.

**Table-A5: H.264 Video Decoder Modules** (video only without audio):

| Product #                | Specifications |            |               |             |               |             |       | Hardware  |
|--------------------------|----------------|------------|---------------|-------------|---------------|-------------|-------|-----------|
|                          | Standard       | Profile    | Resolution    | Chroma      | Precision     | Frame Rate  | Audio |           |
| DC-V-H264-8b-30-720-MA   | H.264          | up to High | up to 720i/p  | 4:2:0/4:2:2 | 8 bits        | up to 30fps | no    | MCM-1000A |
| DC-V-H264-8b-60-720-MA   | H.264          | up to High | up to 720i/p  | 4:2:0/4:2:2 | 8 bits        | up to 60fps | no    | MCM-1000A |
| DC-V-H264-8b-30-1080-MA  | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 30fps | no    | MCM-1000A |
| DC-V-H264-10b-30-1080-MA | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | up to 10 bits | up to 30fps | no    | MCM-1000A |
| DC-V-H264-8b-60-1080-MA  | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | 8 bits        | up to 60fps | no    | MCM-1000A |
| DC-V-H264-10b-60-1080-MA | H.264          | up to High | up to 1080i/p | 4:2:0/4:2:2 | up to 10 bits | up to 60fps | no    | MCM-1000A |
| DC-V-H264-8b-30-4k-MZ    | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 8 bits        | up to 30fps | no    | MCM-1000Z |
| DC-V-H264-10b-30-4k-MZ   | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 10 bits       | up to 30fps | no    | MCM-1000Z |
| DC-V-H264-8b-60-4k-MZ    | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 8 bits        | up to 60fps | no    | MCM-1000Z |
| DC-V-H264-10b-60-4k-MZ   | H.264          | High       | 4kx2k         | 4:2:0/4:2:2 | 10 bits       | up to 60fps | no    | MCM-1000Z |

