System-On-Chip (SOC) Technologies Inc. - DC-VA-H264-8B-60-1080-MXC-ZL Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Artix-7 A200T
Co-Processor	-
Speed	-
Flash Size	32MB
RAM Size	256KB
Connector Type	SO-DIMM-204
Size / Dimension	2.7" x 2.0" (68mm x 51mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/soc-technologies/dc-va-h264-8b-60-1080-mxc-zl

9. The H.265 HD Decoder Modules

10. The H.265 4K Encoder Modules

11. The H.265 4K Decoder Modules

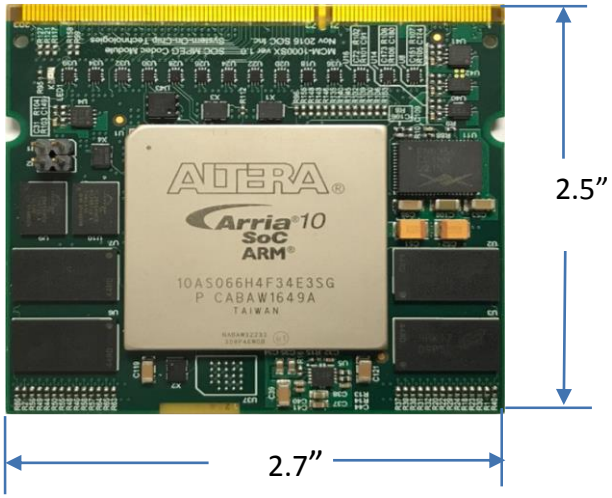

Fig. 5. Dimension of MCM-1000SX

2. Connecting the Module to a User PCB

The MCM-1000S/A/Z/SX modules have identical edge pins that are compatible with standard DDR3 SODIMM connectors. The following off-the-shelf DDR3 SODIMM connectors can be used to connect the SOC codec modules onto a user PCB:

1. MM80-204B1-1
2. MM80-204B1-1E
3. AS0A621-U2SN-7F
4. AS0A621-H2S6-7H

Fig. 6 shows a photo of a standard 204 pin DDR3 SODIMM PCB connector. Refer to the datasheet of the connector used for the physical dimension and PCB design requirements.

Fig. 6 A photo of the standard 204 pin DDR3 SODIMM connector

3. Overview SOC Standard Codec Modules

Each of the above described SOMs: the **MCM-1000S** (based on Spatran-6 FPGA), **MCM-1000A** (based on Artix-7 FPGA), **MCM-1000Z** (based on Zynq-7 FPGAs), and **MCM-1000SX** (based on Altera Arria-10 FPGAs); can be configured into different products by down-loading the desired firmware. At SOC, we produce encoder, decoder, transcoder, and multi-channel encoder or decoder SOMs for video compressions, by down-loading **SOC MPEG Codec IP** cores onto the modules.

The standard encoder modules: H.265, H.264, and MPEG-2, take raw video and audio as input and output TS streams, via the edge pins of the modules, as shown in Fig. 7. The standard decoder modules: H.265, H.264, and MPEG-2, take TS stream as inputs and output decoded video and audio, via the edge pins of the modules, as shown in Fig. 8. There are also control signal pins, to allow the user control of the encoder or decoder.

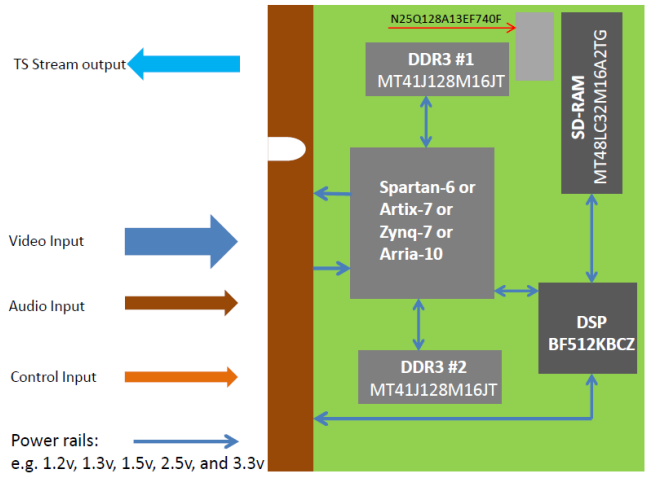

Fig. 7 SOC Standard encoder modules (H.265, H.264, or MPEG-2)

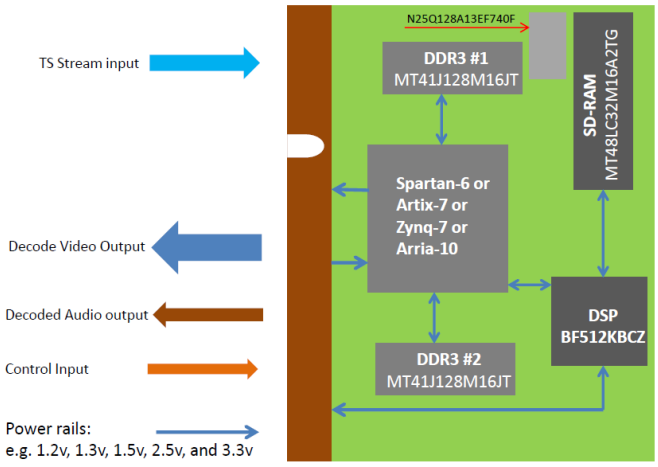

Fig. 8 SOC Standard decoder modules (H.265, H.264, or MPEG-2)

Transport Stream Buffer Ready	112	Input	AA20	3.3v	LVCMOS33
Transport Stream Clock	93	Output	Y18	3.3v	LVCMOS33
Transport Stream Data Valid	106	Output	R17	3.3v	LVCMOS33
Transport Stream Data[0]	77	Output	N13	3.3v	LVCMOS33
Transport Stream Data[1]	79	Output	N14	3.3v	LVCMOS33
Transport Stream Data[2]	81	Output	R18	3.3v	LVCMOS33
Transport Stream Data[3]	83	Output	T18	3.3v	LVCMOS33
Transport Stream Data[4]	85	Output	U17	3.3v	LVCMOS33
Transport Stream Data[5]	87	Output	U18	3.3v	LVCMOS33
Transport Stream Data[6]	89	Output	AB18	3.3v	LVCMOS33
Transport Stream Data[7]	91	Output	AA18	3.3v	LVCMOS33
Transport Stream Start Code	40	Output	V19	3.3v	LVCMOS33
Uart_tx	90	Output	AA16	3.3v	LVCMOS33
Uart_rx	88	Input	Y16	3.3v	LVCMOS33

4.2 Signal Formats

4.2.1 Video Clock Signal (Input)

The **Video Clock** signal (pin # 105) has two functions: (1) It is the clock for the input video data, and (2) it is the clock that drives the encoder engine.

The **Video Clock** signal usually comes from the video input interface chip, such as HDMI or SDI. It is the clock for the input video data. It is also used for driving the encoder engine. The frequency varies according to the resolution of the video input. The following are the clock frequencies for standard video resolutions.

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

4.2.2 Video Data Signals (Input)

The input to the encoder module (H.264 or MPEG-2) is raw video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma. And, 10 input lines: **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization. A **Video Clock** (refer to Section **4.2.1** for the clock frequencies) is required, which provides the timing for the parallel input of luma, chroma, as well as for the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal (pin #150) is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Display Enable signal** at high, when active pixels are being sent out.
The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **4.2.1.**

4.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** (pin # 69) is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

4.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7];** along with the Transport Stream output data clock **Transport Stream Clock** (pin # 113). The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready (pin # 118) and **Transport Stream Data Valid** (pin # 135) are the signals to inform the user side to take over the signals.

4.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset pin (pin # 121) is available. This pin allows the user to reset the encoder when necessary. A high signal will trigger a reset. The reset signal should be maintained at low when in normal operation mode.

4.3 Power Rails of MCM-1000A

Table-2 lists the power and ground pins. Refer to Appendix-A for the pins of power and ground on the edge connector of the MCM-1000A module.

Table-2: MCM-1000A Power and Ground Pins

MCM-1000S Connector Pin	Voltage
1,3,5,7,9,11,13,15	3.3V
10,12,14,16	1.2V
22,24,26,28,30,32	1.5V
189,191,193,195,197,199	2.5V
188,190,192,194	1.3V
43,45,47,49,51,53,55,57	1.0V
2,4,6,8,18,20,34,36,42,44,62,72	**Ground**
17,35,37,39,41,71	**Ground**
73,75,129	**Ground**
74	**Ground**
163,165,167,169,175,177,185,187,203	**Ground**
168,170,172,174,176,184,186,200,202,204	**Ground**

5. The H.264 (and MPEG-2) HD Decoder Modules

5.1 Pin Assignments and Pin Voltages

The decoders for H.264 and MPEG-2 have the same pin assignment. The module for HD resolution decoding uses the MCM-1000A (with the Artix-7 A200T FPGA which is the same as the one used for the HD Encoder). The module MCM-1000Z is used for 4k decoding (the Zynq-7035 for 4k@30, Zynq-7045 for 4k@60).

This section details the pin assignments and pin voltages for the HD decoder (H.264, and MPEG-2) modules. Table-4 shows the pin assignments and the pin voltages.

The schematics of MCM-1000A edge connector are attached in Appendix-B of this document. Appendix-B shows the pin numbers for data, clock, control, and power, which are connected to the FPGA (Artix-7 XC7A200T). It should be noted that the decoder module uses only some of the available edge pins that are connected to the FPGA (some of the pins are not used).

It should also be noted that the HD encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

Table-4: HD Decoder Module (based on MCM-1000A) Pin Assignment

Description	MCM-1000A Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
External Reset	121	Input	W21	3.3v	LVCMOS33
Decoder Clock	115	Input	U20	3.3v	LVCMOS33
Video Clock	105	Output	Y11	3.3v	LVCMOS33
Video Horizontal Sync	146	Output	W16	3.3v	LVCMOS33
Video Vertical Sync	148	Output	V15	3.3v	LVCMOS33
Video Display Enable	150	Output	U15	3.3v	LVCMOS33
Video Data Luma[0]	50	Output	W14	3.3v	LVCMOS33
Video Data Luma[1]	52	Output	Y14	3.3v	LVCMOS33
Video Data Luma[2]	58	Output	V10	3.3v	LVCMOS33
Video Data Luma[3]	59	Output	Y13	3.3v	LVCMOS33
Video Data Luma[4]	60	Output	W10	3.3v	LVCMOS33
Video Data Luma[5]	61	Output	AA14	3.3v	LVCMOS33
Video Data Luma[6]	80	Output	AB13	3.3v	LVCMOS33
Video Data Luma[7]	82	Output	AA13	3.3v	LVCMOS33
Video Data Luma[8]	84	Output	AB17	3.3v	LVCMOS33
Video Data Luma[9]	86	Output	AB16	3.3v	LVCMOS33
Video Data Chroma[0]	92	Output	AA15	3.3v	LVCMOS33
Video Data Chroma[1]	94	Output	AB15	3.3v	LVCMOS33
Video Data Chroma[2]	96	Output	AB12	3.3v	LVCMOS33
Video Data Chroma[3]	98	Output	AB11	3.3v	LVCMOS33
Video Data Chroma[4]	107	Output	Y12	3.3v	LVCMOS33
Video Data Chroma[5]	108	Output	W12	3.3v	LVCMOS33
Video Data Chroma[6]	110	Output	Y17	3.3v	LVCMOS33
Video Data Chroma[7]	140	Output	T14	3.3v	LVCMOS33
Video Data Chroma[8]	142	Output	T15	3.3v	LVCMOS33
Video Data Chroma[9]	144	Output	W15	3.3v	LVCMOS33
Video Frame Sync Relock	56	Input	AB21	3.3v	LVCMOS33

SPDIF Audio	109	Output	Y21	3.3v	LVCMOS33
Transport Stream Clock **(27MHz)**	93	Output	Y18	3.3v	LVCMOS33
Transport Stream Data Valid	106	Output	R17	3.3v	LVCMOS33
Transport Stream Data[0]	77	Output	N13	3.3v	LVCMOS33
Transport Stream Data[1]	79	Output	N14	3.3v	LVCMOS33
Transport Stream Data[2]	81	Output	R18	3.3v	LVCMOS33
Transport Stream Data[3]	83	Output	T18	3.3v	LVCMOS33
Transport Stream Data[4]	85	Output	U17	3.3v	LVCMOS33
Transport Stream Data[5]	87	Output	U18	3.3v	LVCMOS33
Transport Stream Data[6]	89	Output	AB18	3.3v	LVCMOS33
Transport Stream Data[7]	91	Output	AA18	3.3v	LVCMOS33
Uart_tx	90	Output	AA16	3.3v	LVCMOS33
Uart_rx	88	Input	Y16	3.3v	LVCMOS33

5.2 Signal Formats

5.2.1 Clock Signals

The **Decoder Clock** signal (pin # 115) is an input clock for driving the decoder engine. The default frequency is **27MHz**. However, when an SDI port on the carrier board is used to send out the decoded video data, the SDI clock can be connected to the **Decoder Clock.** This will automatically synchronize the decoder outputs with the SDI interface.

The SDI clock frequencies are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

The **Video Clock** signal (pin # 105) is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

4. 27MHz, for SD resolution
5. 74.25MHz, for 720@60 and 1080@30
6. 148.5MHz, for 1080@60.

5.2.2 Video Data Signals (Output)

The output of the HD decoder module (H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma and 10 lines. And, **Video Data Chroma[0]**

6. The H.264 4k Encoder Modules

6.1 Pin Assignments and Pin Voltages

The modules for 4K resolution uses the MCM-1000Z hardware, with the MCM-1000Z35 (Zynq-7035 FPGA) for 4k@30 and MCM-1000Z45 (Zynq-7045 FPGA) for 4k@60. The pin assignment and electrical properties are the same for MCM-1000Z35 and MCM-1000Z45.

Table-6 lists the pin assignments and the pin voltages for the 4K encoder modules based on the MCM-1000Z (MCM-1000Z35 and MCM-1000Z45 are the same).

The schematics of MCM-1000Z edge connector are attached in Appendix-C of this document, which shows the pin numbers for data, clock, control, and power.

Table-6 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

Table-6: 4K Encoder Module (based on MCM-1000Z) Pin Assignment and Pin Voltages

Description	MCM-1000Z Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset B	156	Input	B19	3.3V	LVCMOS33
Video Clock 0	63	Input	AC18	1.5v	LVCMOS15
Video Clock 1	80	Input	AF15	3.3v	LVCMOS33
Video Clock 2	144	Input	AE28	3.3v	LVCMOS33
Video Clock 3	105	Input	AG21	3.3v	LVCMOS33
Video Horizontal Sync	133	Input	W24	1.5v	LVCMOS15
Video Vertical Sync	113	Input	AF22	3.3v	LVCMOS33
Video Display Enable	67	Input	AD18	1.5v	LVCMOS15
Video Data 0 Luma[0]	135	Input	W25	1.5v	LVCMOS15
Video Data 0 Luma[1]	137	Input	W26	1.5v	LVCMOS15
Video Data 0 Luma[2]	116	Input	V27	1.5v	LVCMOS15
Video Data 0 Luma[3]	118	Input	W28	1.5v	LVCMOS15
Video Data 0 Luma[4]	124	Input	W29	1.5v	LVCMOS15
Video Data 0 Luma[5]	126	Input	W30	1.5v	LVCMOS15
Video Data 0 Luma[6]	128	Input	V28	1.5v	LVCMOS15
Video Data 0 Luma[7]	130	Input	V29	1.5v	LVCMOS15
Video Data 0 Luma[8]	132	Input	T30	1.5v	LVCMOS15
Video Data 0 Luma[9]	134	Input	U30	1.5v	LVCMOS15
Video Data 1 Luma[0]	117	Input	AG22	3.3v	LVCMOS33
Video Data 1 Luma[1]	119	Input	AH22	3.3v	LVCMOS33
Video Data 1 Luma[2]	121	Input	AJ21	3.3v	LVCMOS33
Video Data 1 Luma[3]	123	Input	AK21	3.3v	LVCMOS33

Video Data 1 Luma[4]	125	Input	AF23	3.3v	LVCMOS33
Video Data 1 Luma[5]	127	Input	AF24	3.3v	LVCMOS33
Video Data 1 Luma[6]	92	Input	AJ23	3.3v	LVCMOS33
Video Data 1 Luma[7]	94	Input	AJ24	3.3v	LVCMOS33
Video Data 1 Luma[8]	96	Input	AG24	3.3v	LVCMOS33
Video Data 1 Luma[9]	98	Input	AG25	3.3v	LVCMOS33
Video Data 2 Luma[0]	77	Input	AJ16	3.3v	LVCMOS33
Video Data 2 Luma[1]	79	Input	AK16	3.3v	LVCMOS33
Video Data 2 Luma[2]	81	Input	AH17	3.3v	LVCMOS33
Video Data 2 Luma[3]	83	Input	AH16	3.3v	LVCMOS33
Video Data 2 Luma[4]	85	Input	AH18	3.3v	LVCMOS33
Video Data 2 Luma[5]	87	Input	AJ18	3.3v	LVCMOS33
Video Data 2 Luma[6]	78	Input	AF13	3.3v	LVCMOS33
Video Data 2 Luma[7]	82	Input	AG15	3.3v	LVCMOS33
Video Data 2 Luma[8]	84	Input	AG17	3.3v	LVCMOS33
Video Data 2 Luma[9]	86	Input	AG16	3.3v	LVCMOS33
Video Data 3 Luma[0]	107	Input	AH21	3.3v	LVCMOS33
Video Data 3 Luma[1]	122	Input	AH29	3.3v	LVCMOS33
Video Data 3 Luma[2]	115	Input	AE22	3.3v	LVCMOS33
Video Data 3 Luma[3]	146	Input	AF28	3.3v	LVCMOS33
Video Data 3 Luma[4]	148	Input	AF29	3.3v	LVCMOS33
Video Data 3 Luma[5]	150	Input	AG29	3.3v	LVCMOS33
Video Data 3 Luma[6]	100	Input	AH23	3.3v	LVCMOS33
Video Data 3 Luma[7]	102	Input	AH24	3.3v	LVCMOS33
Video Data 3 Luma[8]	104	Input	AJ25	3.3v	LVCMOS33
Video Data 3 Luma[9]	106	Input	AK25	3.3v	LVCMOS33
Video Data 0 Chroma[0]	143	Input	T29	1.5v	LVCMOS15
Video Data 0 Chroma[1]	145	Input	U29	1.5v	LVCMOS15
Video Data 0 Chroma[2]	147	Input	R28	1.5v	LVCMOS15
Video Data 0 Chroma[3]	149	Input	T28	1.5v	LVCMOS15
Video Data 0 Chroma[4]	151	Input	P30	1.5v	LVCMOS15
Video Data 0 Chroma[5]	153	Input	R30	1.5v	LVCMOS15
Video Data 0 Chroma[6]	155	Input	N29	1.5v	LVCMOS15
Video Data 0 Chroma[7]	157	Input	P29	1.5v	LVCMOS15
Video Data 0 Chroma[8]	159	Input	N28	1.5v	LVCMOS15
Video Data 0 Chroma[9]	161	Input	P28	1.5v	LVCMOS15
Video Data 1 Chroma[0]	89	Input	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[1]	91	Input	AK18	3.3v	LVCMOS33
Video Data 1 Chroma[2]	93	Input	AF19	3.3v	LVCMOS33
Video Data 1 Chroma[3]	95	Input	AG19	3.3v	LVCMOS33
Video Data 1 Chroma[4]	97	Input	AH19	3.3v	LVCMOS33
Video Data 1 Chroma[5]	99	Input	AJ19	3.3v	LVCMOS33
Video Data 1 Chroma[6]	101	Input	AF20	3.3v	LVCMOS33
Video Data 1 Chroma[7]	103	Input	AG20	3.3v	LVCMOS33
Video Data 1 Chroma[8]	109	Input	AJ20	3.3v	LVCMOS33
Video Data 1 Chroma[9]	111	Input	AK20	3.3v	LVCMOS33
Video Data 2 Chroma[0]	38	Input	AE12	3.3v	LVCMOS33
Video Data 2 Chroma[1]	40	Input	AF12	3.3v	LVCMOS33

Video Data 2 Chroma[1]	40	Output	AF12	3.3v	LVCMOS33
Video Data 2 Chroma[2]	50	Output	AG12	3.3v	LVCMOS33
Video Data 2 Chroma[3]	52	Output	AH12	3.3v	LVCMOS33
Video Data 2 Chroma[4]	54	Output	AH14	3.3v	LVCMOS33
Video Data 2 Chroma[5]	56	Output	AH13	3.3v	LVCMOS33
Video Data 2 Chroma[6]	58	Output	AJ14	3.3v	LVCMOS33
Video Data 2 Chroma[7]	60	Output	AJ13	3.3v	LVCMOS33
Video Data 2 Chroma[8]	59	Output	AK13	3.3v	LVCMOS33
Video Data 2 Chroma[9]	61	Output	AK12	3.3v	LVCMOS33
Video Data 3 Chroma[0]	108	Output	AJ26	3.3v	LVCMOS33
Video Data 3 Chroma[1]	110	Output	AK26	3.3v	LVCMOS33
Video Data 3 Chroma[2]	112	Output	AH26	3.3v	LVCMOS33
Video Data 3 Chroma[3]	114	Output	AH27	3.3v	LVCMOS33
Video Data 3 Chroma[4]	136	Output	AK27	3.3v	LVCMOS33
Video Data 3 Chroma[5]	138	Output	AK28	3.3v	LVCMOS33
Video Data 3 Chroma[6]	139	Output	AJ28	3.3v	LVCMOS33
Video Data 3 Chroma[7]	141	Output	AJ29	3.3v	LVCMOS33
Video Data 3 Chroma[8]	140	Output	AJ30	3.3v	LVCMOS33
Video Data 3 Chroma[9]	142	Output	AK30	3.3v	LVCMOS33
SPDIF Audio	27	Output	Y20	1.5v	LVCMOS15
Transport Stream Clock	31	Input	AA18	1.5v	LVCMOS15
Transport Stream Data Valid	33	input	AA19	1.5v	LVCMOS15
Transport Stream Data [0]	152	input	AF30	3.3v	LVCMOS33
Transport Stream Data [1]	154	input	AG30	3.3v	LVCMOS33
Transport Stream Data [2]	158	input	AE30	3.3v	LVCMOS33
Transport Stream Data [3]	160	input	AB29	3.3v	LVCMOS33
Transport Stream Data [4]	162	input	AB30	3.3v	LVCMOS33
Transport Stream Data [5]	164	input	AA27	3.3v	LVCMOS33
Transport Stream Data [6]	166	input	AA28	3.3v	LVCMOS33
Transport Stream Data [7]	120	input	AH28	3.3v	LVCMOS33
Uart_tx	90	Output	AK15	3.3v	LVCMOS33
Uart_rx	88	Input	AJ15	3.3v	LVCMOS33
Video Frame Sync Clock	80	Input	AF15	3.3v	LVCMOS33
Video Frame Sync Pause	63	Input	AC18	1.5v	LVCMOS15

7.2 Signal Formats

7.2.1 Video Clock Signal (Output)

The **Video Clock** signal (pin # 105) is the clock signal that provides the timing for the parallel luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The default is 148.5MHz for 4K@60 and 74.25MHz for 4K@30.

12.2 VTR-4000C Evaluation Board

Fig. 12 shows the top view of the VTR-4000C board. Major components and I/O ports are marked in the figure. Refer to the User Guide of VTR-4000C for further details.

SOC licenses the Schematics of VTR-4000C to the customers that have purchased encoder (or decoder) Modules. Firmware of the VTR-4000C, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, sales@soctechnologies.com, for details.

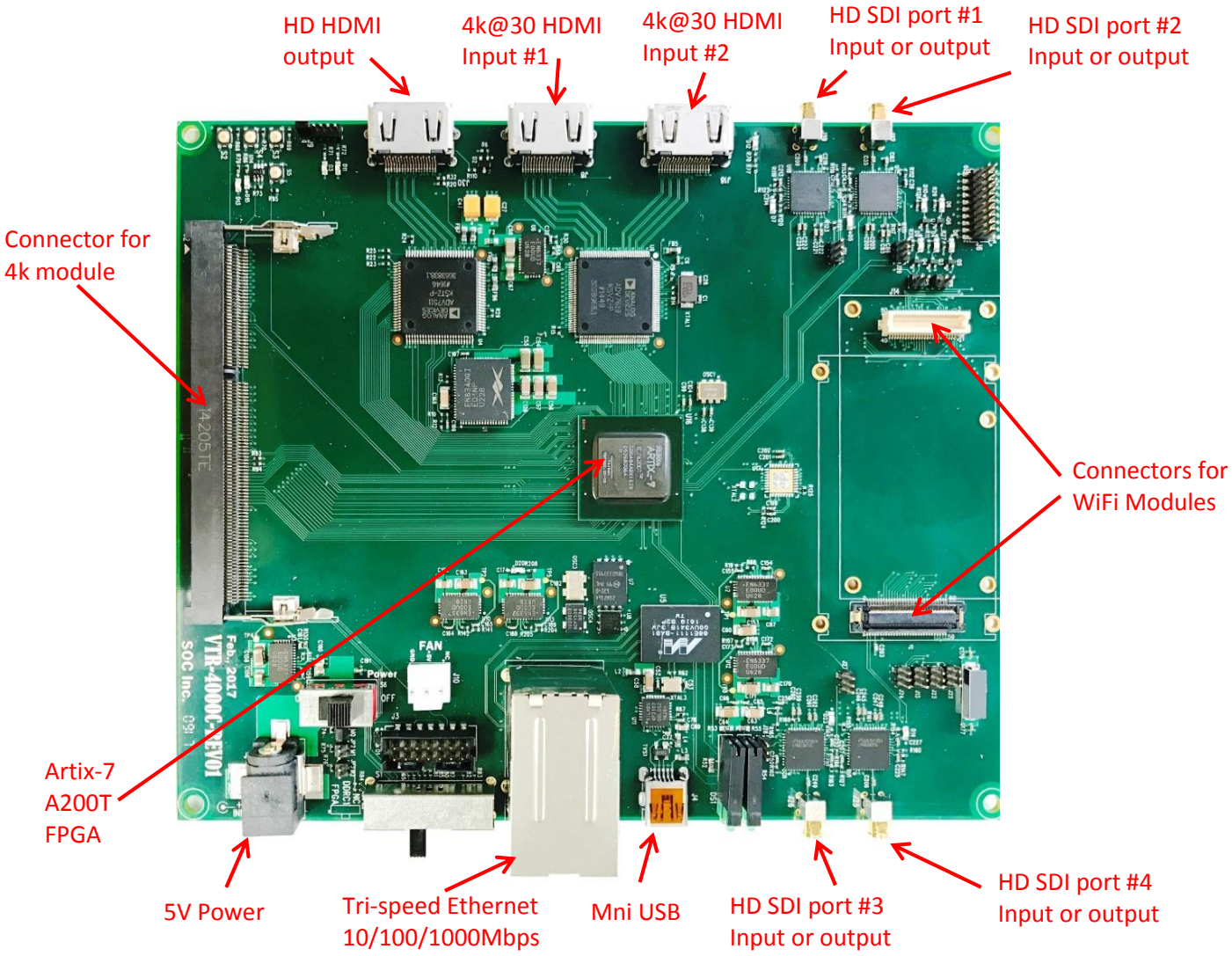

Fig. 12. VTR-4000C evaluation board top view

13. Ordering Information

Fig. 13 shows the product code naming convention for the SOC MPEG codec modules and IP cores. Non-standard codec modules can be ordered following the same naming format (minimum order quantity is required for non-standard modules).

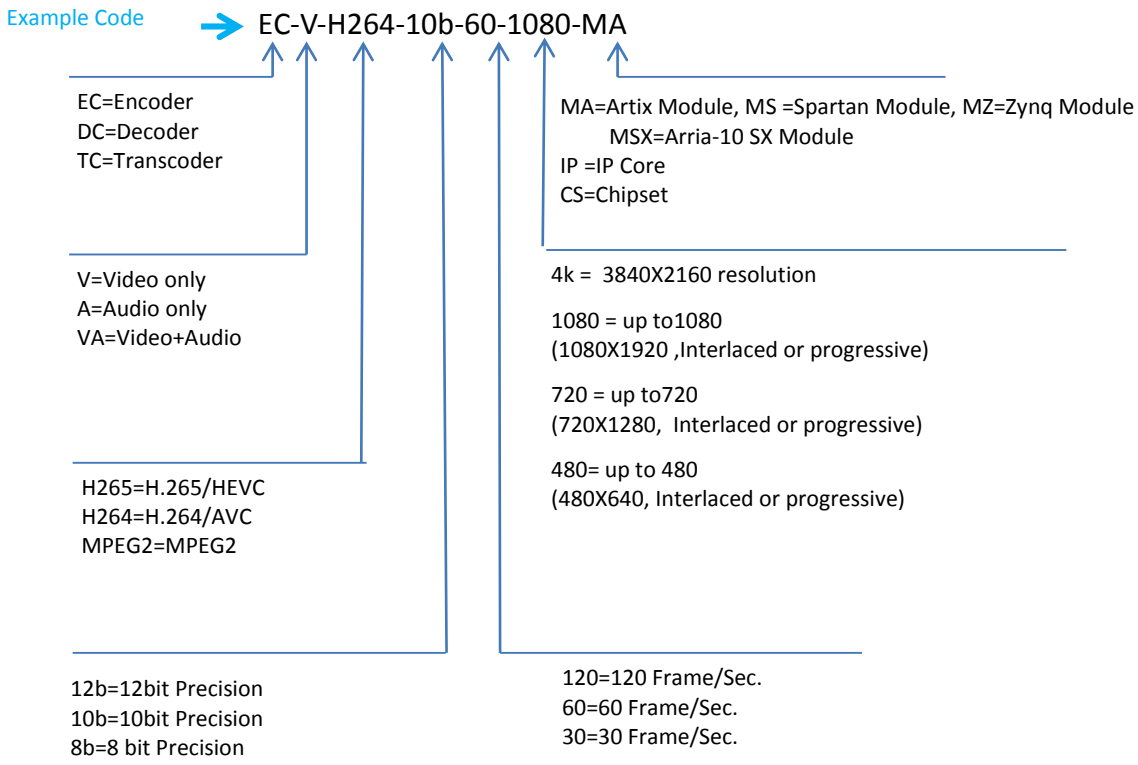

Fig. 13 SOC MPEG codec (IP cores and modules) product code naming convention

14. Contact Information

Please contact SOC head office or distributor for product details and to place an order.

Head Office

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15. Document Revisions

Version #	Revision Date	Notes
V.1.0	10/05/2017	First release
V.1.1	19/05/2017	Minor revision
V.2.0	20/05/2017	Major revision (adding 4k)
V.2.1	05/06/2017	Minor revision

Appendix-A Factory Standard Codec Modules

A.1 H.265 Encoder Modules

The H.265 encoder modules are based on either the MCM-1000SX or MCM-1000Z hardware. The SOC H.265 encoder IP cores of different configurations are used to configure the FPGAs on the hardware modules to produce the codec modules.

Table-A1 lists the product codes of the factory standard H.265 video encoder (video only) modules, along with the specifications for each module. Table-A2 lists the video/audio encoder modules. The hardware platform, MCM-1000SX or MCM-1000Z, is used for the H.265 video encoder. Customers can order the H.265 encoder modules using the product code, according to the specifications required by the application.

Table-A1: H.265 Video Encoder Modules (video only without audio):

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-V-H265-8b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H265-10b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H265-10b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 30fps	no
EC-V-H265-8b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H265-10b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
EC-V-H265-10b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 60fps	no
EC-V-H265-8b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H265-10b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H265-10b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12 bits	up to 30fps	no
EC-V-H265-8b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H265-10b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
EC-V-H265-10b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12bits	up to 60fps	no

Table-A6: H.264 Video&Audio Decoder Modules (both video and audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H264-8b-30-720-MA	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-60-720-MA	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-30-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-10b-30-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-10b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-10b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	10 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-8b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-10b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	10 bits	up to 60fps	AAC/MPEG2 L-2 L	MCM-1000Z

A.4 MPEG-2 Encoder Modules

Table-A7 lists the standard MPEG-2 video encoder modules. Table-A8 lists the MPEG-2 video/audio encoder modules. The 8 -bit precision and 60 frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A7: MPEG-2 Video Encoder Module (video only without audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-MPEG2-8b-30-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-MPEG2-8b-30-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A

Table-A8: MPEG-2 Video&Audio Encoder Modules (both video and audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-MPEG2-8b-30-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-30-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A

A.8 MPEG2-to-H.264 Transcoder Modules

Table-A15 lists the standard MPEG2-to-H.264 video transcoder modules, and Table-A16 lists the MPEG2-to-H.264 video/audio transcoder modules. The 60frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A15: MPEG2-to-H.264 Video Transcoder Modules (video only without audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-MPEG2-to-H.264-8b-30-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-60-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-30-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000A
TC-V-MPEG2-to-H.264-8b-60-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000A

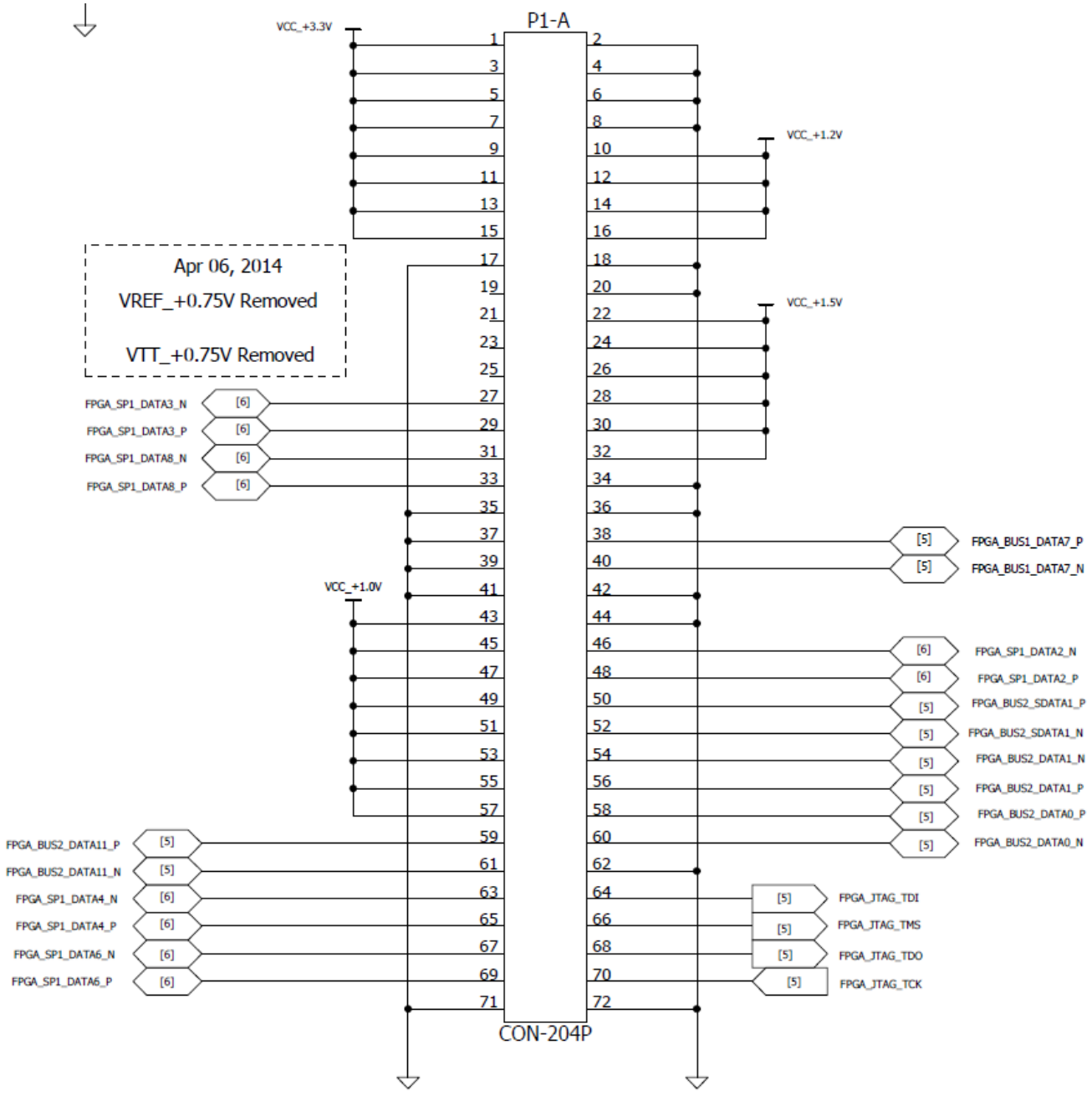
Table-A16: MPEG2-to-H.264 Video&Audio Transcoder Modules (both video and audio)**:**

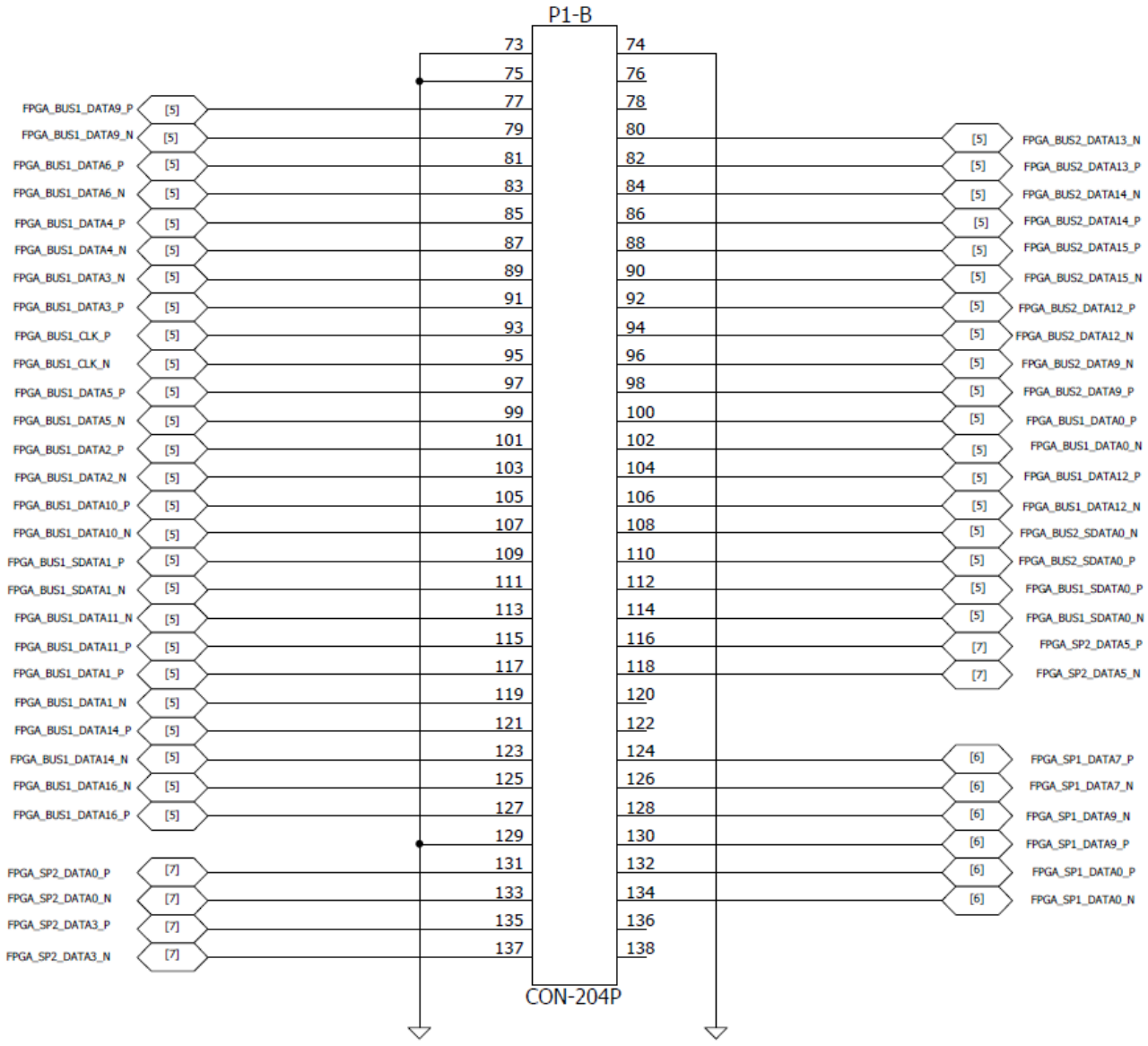
Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-VA-MPEG2-to-H.264-8b-30-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-60-720-MA	MPEG2	High	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-30-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	MPEG2-L2/AAC	MCM-1000A
TC-VA-MPEG2-to-H.264-8b-60-1080-MA	MPEG2	High	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	MPEG2-L2/AAC	MCM-1000A

A.9 Non-Standard Codec Modules

The previous section provides the information on SOC's factory standard MPEG codec modules. Customers can order modules based on customer specific requirements (non-standard modules). There is a Minimum Order Quantity (MOQ) required for customized configurations. Contact SOC sales sale@soctechnologies.com for information.

Appendix - B MCM-1000A Edge Connector Schematics

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FPGA_BUS1_DATA3_N
FPGA_BUS1_DATA3_P
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FPGA_BUS1_DATA1_N
FPGA_BUS1_DATA14_P
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FPGA_BUS1_DATA16_N
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FPGA_BUS2_DATA14_P
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FPGA_BUS2_DATA12_N
FPGA_BUS2_DATA9_N
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FPGA_BUS1_DATA12_P
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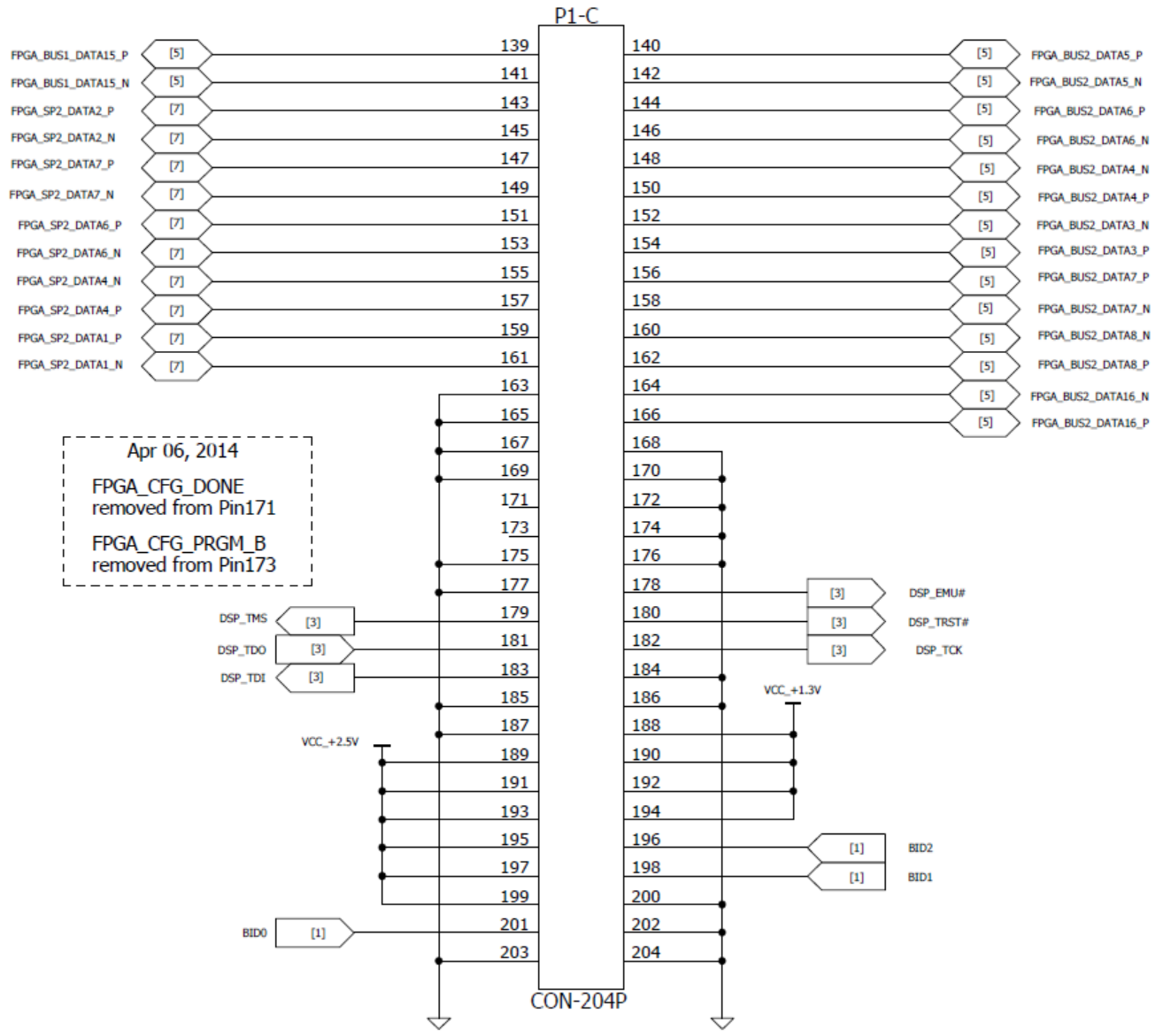
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Apr 06, 2014
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VCC_+1.3V
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