System On Chip (SOC) Technologies Inc. - EC-V-H264-8B-60-1080-MXC-ZL Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Artix-7 A200T
Co-Processor	-
Speed	-
Flash Size	32MB
RAM Size	256KB
Connector Type	SO-DIMM-204
Size / Dimension	2.7" x 2.0" (68mm x 51mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/soc-technologies/ec-v-h264-8b-60-1080-mxc-zl

6. The H.264 4K Encoder Modules

7. The H.264 4K Decoder Modules

8. The H.265 HD Encoder Modules

1. Overview of SOC SOM Modules

The SOC SOMs are small circuit boards with FPGA, DDRs, Flash, and clocks in one module to support FPGA-based systems. A module can be configured into a SOM by using the applicable firmware. The module is connected to a user PCB through a standard DDR3 SODIMM connector. Customers can order the blank SOMs from SOC and use their own firmware to make SOM products.

SOC configures the modules into MPEG codec SOMs for video/audio compression, decompression, and transcoding functions. Currently available modules are:

	Hardware Product Code	FPGA Chip on the Module	SOC Codec module Resolution Capacity
1	MCM-1000S	Spartan-6 XC6SLX150	H.264 or MPEG-2 HD up to 1080@30
2	MCM-1000A	Artix-7 XC7A200T	H.264 or MPEG-2 HD up to 1080@60
3	MCM-1000Z	Zynq-7 XC7Z035/045	H.264 4k@30/60, or H.265 HD up to 1080@60
4	MCM-1000SX	Arria-10 SX220/270/320/480/570/660	H.264 HD 1080@30/60, or H.264 4k@30/60, or H.265 HD up to 1080@60), or H.265 4k@30/60

Fig. 1 shows a photo of the modules. Fig. 2-5 shows the dimensions of MCM-1000S, MCM-1000A, MCM-1000Z, and MCM-1000SX respectively.

Fig. 1 SOC codec modules

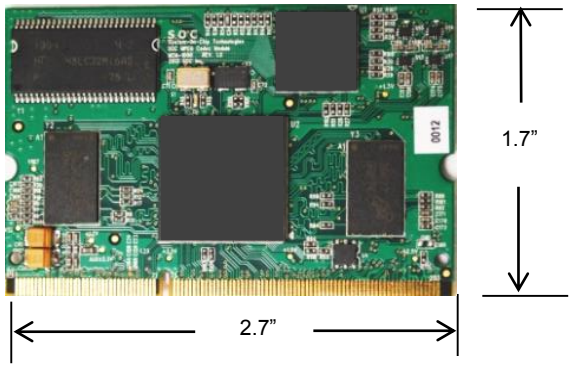

Fig. 2. Dimension of MCM-1000S

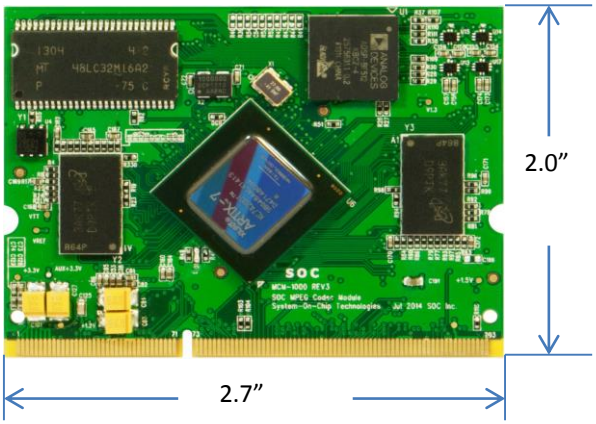

Fig. 3. Dimension of MCM-1000A

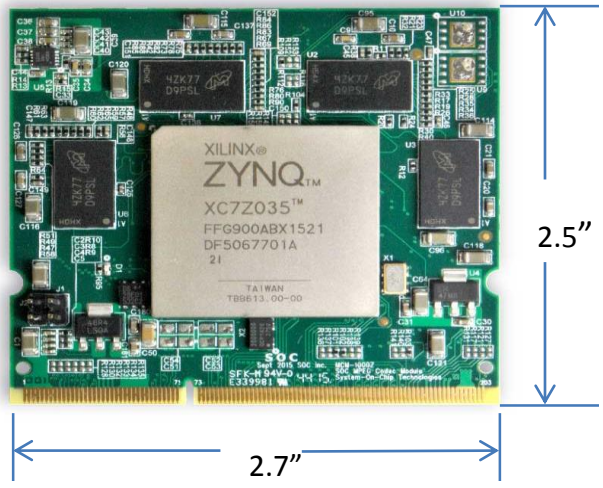

Fig. 4. Dimension of MCM-1000Z

3. Overview SOC Standard Codec Modules

Each of the above described SOMs: the **MCM-1000S** (based on Spatran-6 FPGA), **MCM-1000A** (based on Artix-7 FPGA), **MCM-1000Z** (based on Zynq-7 FPGAs), and **MCM-1000SX** (based on Altera Arria-10 FPGAs); can be configured into different products by down-loading the desired firmware. At SOC, we produce encoder, decoder, transcoder, and multi-channel encoder or decoder SOMs for video compressions, by down-loading **SOC MPEG Codec IP** cores onto the modules.

The standard encoder modules: H.265, H.264, and MPEG-2, take raw video and audio as input and output TS streams, via the edge pins of the modules, as shown in Fig. 7. The standard decoder modules: H.265, H.264, and MPEG-2, take TS stream as inputs and output decoded video and audio, via the edge pins of the modules, as shown in Fig. 8. There are also control signal pins, to allow the user control of the encoder or decoder.

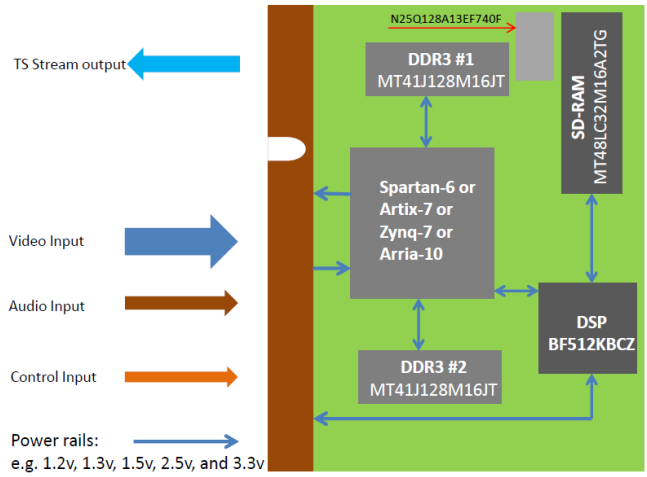

Fig. 7 SOC Standard encoder modules (H.265, H.264, or MPEG-2)

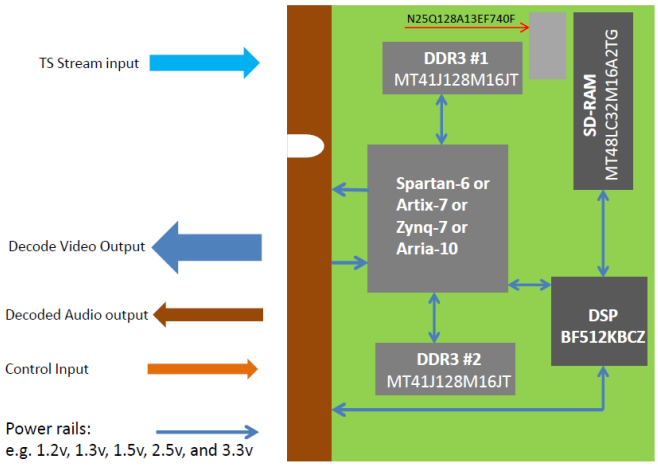

Fig. 8 SOC Standard decoder modules (H.265, H.264, or MPEG-2)

Appendix-A provides the details of the Standard Codec Modules, including the product tables which list the product codes along with the specifications. Customers can order the modules according the specifications required by using the corresponding product code.

The pin assignments, pin voltages, and signal formats for standard encoder and decoder modules are detailed respectively in this Datasheet in the following sections:

- Section 4: The H.264 (and MPEG-2) HD Encoder Modules
- Section 5: The H.264 (and MPEG-2) HD Decoder Modules
- Section 6: The H.264 4k Encoder Modules
- Section 7: The H.264 4k Decoder Modules
- Section 8: The H.265 HD Encoder Modules
- Section 9: The H.265 HD Decoder Modules (will be available soon)
- Section 10: The H.265 4k Encoder Modules
- Section 11: The H.265 4k Encoder Modules (will be available soon)

It should be noted that not all of the modules listed in Appendix-A are discussed in this Datasheet. Pin assignments and electrical properties for the modules that are not provided in the document, will be provided on demand basis.

SOC also offers customized modules according to customer requirements, such as Transcoder modules, Multi-channel encoder or decoder modules, and modules with non-standard I/Os. For details, contact SOC sales at: sales@soctechnologies.com

One of the popular extended versions of the standard codec modules is the –NET version which integrates the SOC low latency network stack (UDP/IP over Ethernet) into the encoder or decoder module. The pin assignments, pin voltages, and signal formats for the –NET version encoder and decoder modules are detailed in the document:

Datasheet – Encoder and Decoder Modules – NET Version

4.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** (pin # 69) is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

4.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7];** along with the Transport Stream output data clock **Transport Stream Clock** (pin # 113). The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready (pin # 118) and **Transport Stream Data Valid** (pin # 135) are the signals to inform the user side to take over the signals.

4.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset pin (pin # 121) is available. This pin allows the user to reset the encoder when necessary. A high signal will trigger a reset. The reset signal should be maintained at low when in normal operation mode.

4.3 Power Rails of MCM-1000A

Table-2 lists the power and ground pins. Refer to Appendix-A for the pins of power and ground on the edge connector of the MCM-1000A module.

Table-2: MCM-1000A Power and Ground Pins

MCM-1000S Connector Pin	Voltage
1,3,5,7,9,11,13,15	3.3V
10,12,14,16	1.2V
22,24,26,28,30,32	1.5V
189,191,193,195,197,199	2.5V
188,190,192,194	1.3V
43,45,47,49,51,53,55,57	1.0V
2,4,6,8,18,20,34,36,42,44,62,72	**Ground**
17,35,37,39,41,71	**Ground**
73,75,129	**Ground**
74	**Ground**
163,165,167,169,175,177,185,187,203	**Ground**
168,170,172,174,176,184,186,200,202,204	**Ground**

SPDIF Audio	109	Output	Y21	3.3v	LVCMOS33
Transport Stream Clock **(27MHz)**	93	Output	Y18	3.3v	LVCMOS33
Transport Stream Data Valid	106	Output	R17	3.3v	LVCMOS33
Transport Stream Data[0]	77	Output	N13	3.3v	LVCMOS33
Transport Stream Data[1]	79	Output	N14	3.3v	LVCMOS33
Transport Stream Data[2]	81	Output	R18	3.3v	LVCMOS33
Transport Stream Data[3]	83	Output	T18	3.3v	LVCMOS33
Transport Stream Data[4]	85	Output	U17	3.3v	LVCMOS33
Transport Stream Data[5]	87	Output	U18	3.3v	LVCMOS33
Transport Stream Data[6]	89	Output	AB18	3.3v	LVCMOS33
Transport Stream Data[7]	91	Output	AA18	3.3v	LVCMOS33
Uart_tx	90	Output	AA16	3.3v	LVCMOS33
Uart_rx	88	Input	Y16	3.3v	LVCMOS33

5.2 Signal Formats

5.2.1 Clock Signals

The **Decoder Clock** signal (pin # 115) is an input clock for driving the decoder engine. The default frequency is **27MHz**. However, when an SDI port on the carrier board is used to send out the decoded video data, the SDI clock can be connected to the **Decoder Clock.** This will automatically synchronize the decoder outputs with the SDI interface.

The SDI clock frequencies are:

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

The **Video Clock** signal (pin # 105) is the clock for the video data output by the decoder. The frequency of the **Video clock** is determined by the video resolution, which are:

4. 27MHz, for SD resolution
5. 74.25MHz, for 720@60 and 1080@30
6. 148.5MHz, for 1080@60.

5.2.2 Video Data Signals (Output)

The output of the HD decoder module (H.264 or MPEG-2) is the decoded video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma and 10 lines. And, **Video Data Chroma[0]**

to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. A **Video Clock** (refer to Section **5.2.1** for the clock frequencies) is sent out, which provides the timing for the parallel inputs of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal (pin #150) is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

Output data are sampled at the rising edge of the clock. (The clock rates will correspond to the resolution and frame rate, as discussed in Section **5.2.1.)**

5.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

5.2.4 TS Stream Signals (Input)

The input of the decoder module is an MPEG transport stream, which is sent into the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7]. Transport Stream Clock** (27MHz) is the clock for the **Transport Stream Data** lines. The **Transport Stream Data Valid** signal informs the decoder that the input is valid.

5.2.5 Decoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

5.3 Power Rails of MCM-1000A

The power rails for the HD (H.264 or MPEG-2) decoder module is the same as the ones for the HD encoder module. Refer to Table-2 for the power and ground pins. Also, refer to Appendix-A for the power and ground pins on the edge connector of the MCM-1000A module.

5.4 Power Requirement and Supply Amperage

The total power at operation required by a given decoder ranges from 2 to 4 Watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail delivers only a portion of the total lower. However, the power is not evenly distributed among the rails. Table-5 lists the power

estimation by Xilinx Vivado FPGA software for each rail, at 1080p@60 resolution, and can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-5 is higher than the measured real power.

Again, the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-5.

Table-5: Power estimation for the decoder module (1080p@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	2.421	2.362	0.058
Vccaux	1.800	0.497	0.464	0.033
Vcco33	3.300	0.053	0.048	0.005
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.500	0.495	0.005
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.037	0.028	0.009
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.022	0.002	0.020

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 6 of this document. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for further details.

6. The H.264 4k Encoder Modules

6.1 Pin Assignments and Pin Voltages

The modules for 4K resolution uses the MCM-1000Z hardware, with the MCM-1000Z35 (Zynq-7035 FPGA) for 4k@30 and MCM-1000Z45 (Zynq-7045 FPGA) for 4k@60. The pin assignment and electrical properties are the same for MCM-1000Z35 and MCM-1000Z45.

Table-6 lists the pin assignments and the pin voltages for the 4K encoder modules based on the MCM-1000Z (MCM-1000Z35 and MCM-1000Z45 are the same).

The schematics of MCM-1000Z edge connector are attached in Appendix-C of this document, which shows the pin numbers for data, clock, control, and power.

Table-6 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Zynq-7000 datasheet provides further information regarding the properties of these pins, and can be used as a reference.

Table-6: 4K Encoder Module (based on MCM-1000Z) Pin Assignment and Pin Voltages

Description	MCM-1000Z Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset B	156	Input	B19	3.3V	LVCMOS33
Video Clock 0	63	Input	AC18	1.5v	LVCMOS15
Video Clock 1	80	Input	AF15	3.3v	LVCMOS33
Video Clock 2	144	Input	AE28	3.3v	LVCMOS33
Video Clock 3	105	Input	AG21	3.3v	LVCMOS33
Video Horizontal Sync	133	Input	W24	1.5v	LVCMOS15
Video Vertical Sync	113	Input	AF22	3.3v	LVCMOS33
Video Display Enable	67	Input	AD18	1.5v	LVCMOS15
Video Data 0 Luma[0]	135	Input	W25	1.5v	LVCMOS15
Video Data 0 Luma[1]	137	Input	W26	1.5v	LVCMOS15
Video Data 0 Luma[2]	116	Input	V27	1.5v	LVCMOS15
Video Data 0 Luma[3]	118	Input	W28	1.5v	LVCMOS15
Video Data 0 Luma[4]	124	Input	W29	1.5v	LVCMOS15
Video Data 0 Luma[5]	126	Input	W30	1.5v	LVCMOS15
Video Data 0 Luma[6]	128	Input	V28	1.5v	LVCMOS15
Video Data 0 Luma[7]	130	Input	V29	1.5v	LVCMOS15
Video Data 0 Luma[8]	132	Input	T30	1.5v	LVCMOS15
Video Data 0 Luma[9]	134	Input	U30	1.5v	LVCMOS15
Video Data 1 Luma[0]	117	Input	AG22	3.3v	LVCMOS33
Video Data 1 Luma[1]	119	Input	AH22	3.3v	LVCMOS33
Video Data 1 Luma[2]	121	Input	AJ21	3.3v	LVCMOS33
Video Data 1 Luma[3]	123	Input	AK21	3.3v	LVCMOS33

Video Data 1 Luma[4]	125	Input	AF23	3.3v	LVCMOS33
Video Data 1 Luma[5]	127	Input	AF24	3.3v	LVCMOS33
Video Data 1 Luma[6]	92	Input	AJ23	3.3v	LVCMOS33
Video Data 1 Luma[7]	94	Input	AJ24	3.3v	LVCMOS33
Video Data 1 Luma[8]	96	Input	AG24	3.3v	LVCMOS33
Video Data 1 Luma[9]	98	Input	AG25	3.3v	LVCMOS33
Video Data 2 Luma[0]	77	Input	AJ16	3.3v	LVCMOS33
Video Data 2 Luma[1]	79	Input	AK16	3.3v	LVCMOS33
Video Data 2 Luma[2]	81	Input	AH17	3.3v	LVCMOS33
Video Data 2 Luma[3]	83	Input	AH16	3.3v	LVCMOS33
Video Data 2 Luma[4]	85	Input	AH18	3.3v	LVCMOS33
Video Data 2 Luma[5]	87	Input	AJ18	3.3v	LVCMOS33
Video Data 2 Luma[6]	78	Input	AF13	3.3v	LVCMOS33
Video Data 2 Luma[7]	82	Input	AG15	3.3v	LVCMOS33
Video Data 2 Luma[8]	84	Input	AG17	3.3v	LVCMOS33
Video Data 2 Luma[9]	86	Input	AG16	3.3v	LVCMOS33
Video Data 3 Luma[0]	107	Input	AH21	3.3v	LVCMOS33
Video Data 3 Luma[1]	122	Input	AH29	3.3v	LVCMOS33
Video Data 3 Luma[2]	115	Input	AE22	3.3v	LVCMOS33
Video Data 3 Luma[3]	146	Input	AF28	3.3v	LVCMOS33
Video Data 3 Luma[4]	148	Input	AF29	3.3v	LVCMOS33
Video Data 3 Luma[5]	150	Input	AG29	3.3v	LVCMOS33
Video Data 3 Luma[6]	100	Input	AH23	3.3v	LVCMOS33
Video Data 3 Luma[7]	102	Input	AH24	3.3v	LVCMOS33
Video Data 3 Luma[8]	104	Input	AJ25	3.3v	LVCMOS33
Video Data 3 Luma[9]	106	Input	AK25	3.3v	LVCMOS33
Video Data 0 Chroma[0]	143	Input	T29	1.5v	LVCMOS15
Video Data 0 Chroma[1]	145	Input	U29	1.5v	LVCMOS15
Video Data 0 Chroma[2]	147	Input	R28	1.5v	LVCMOS15
Video Data 0 Chroma[3]	149	Input	T28	1.5v	LVCMOS15
Video Data 0 Chroma[4]	151	Input	P30	1.5v	LVCMOS15
Video Data 0 Chroma[5]	153	Input	R30	1.5v	LVCMOS15
Video Data 0 Chroma[6]	155	Input	N29	1.5v	LVCMOS15
Video Data 0 Chroma[7]	157	Input	P29	1.5v	LVCMOS15
Video Data 0 Chroma[8]	159	Input	N28	1.5v	LVCMOS15
Video Data 0 Chroma[9]	161	Input	P28	1.5v	LVCMOS15
Video Data 1 Chroma[0]	89	Input	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[1]	91	Input	AK18	3.3v	LVCMOS33
Video Data 1 Chroma[2]	93	Input	AF19	3.3v	LVCMOS33
Video Data 1 Chroma[3]	95	Input	AG19	3.3v	LVCMOS33
Video Data 1 Chroma[4]	97	Input	AH19	3.3v	LVCMOS33
Video Data 1 Chroma[5]	99	Input	AJ19	3.3v	LVCMOS33
Video Data 1 Chroma[6]	101	Input	AF20	3.3v	LVCMOS33
Video Data 1 Chroma[7]	103	Input	AG20	3.3v	LVCMOS33
Video Data 1 Chroma[8]	109	Input	AJ20	3.3v	LVCMOS33
Video Data 1 Chroma[9]	111	Input	AK20	3.3v	LVCMOS33
Video Data 2 Chroma[0]	38	Input	AE12	3.3v	LVCMOS33
Video Data 2 Chroma[1]	40	Input	AF12	3.3v	LVCMOS33

Chroma[9], for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization if embedded SAV/EAV are not used. The video clocks (refer to Section **6.2.1**) provide the timing for the parallel input of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Video Display Enable** signal at high, when active pixels are being sent out.

The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **6.2.1.**

6.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

6.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7],** along with the Transport Stream output data clock **Transport Stream Clock** (pin # 31). The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready (pin # 28) and **Transport Stream Data Valid** (pin # 33) are the signals to inform the user side to take over the signals.

6.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset **PS Soft Reset_B** (pin # 156) is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

6.3 Power Rails of MCM-1000Z

Refer to Appendix-B for the pins of power and ground on the edge connector of the MCM-1000Z module. The power rails are: 1.0V, 1.2V, 1.3V, 1.5V, 2.5V, and 3.3V.

7. The H.264 4K Decoder Modules

7.1 Pin Assignments and Pin Voltages

The modules for H.264 4K resolution use the MCM-1000Z, Zynq-7035 (for 4k@30) or Zynq-7045 (4k@60). This section details the pin assignment and pin voltages for H.264 4K decoder modules based on the MCM-1000Z hardware.

Table-8 shows the pin assignments and the pin voltages for H.264 4k decoder modules based on the MCM-1000Z.

The schematics of MCM-1000Z edge connector are attached in Appendix-C of this document. Appendix-C shows the pin numbers for data, clock, control, and power, which are connected to the FPGA (Zynq-7035 or 7045, which are pin-compatible).

It should be noted that the 4K encoder and decoder pin assignments are symmetrical, i.e. the video input pins on the encoder module become the video output pins on the decoder module.

Table-8: 4K Decoder Module (based on MCM-1000Z) Pin Assignment

Description	MCM-1000Z Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
PS Soft Reset_B	156	Input	B19	3.3V	LVCMOS33
Video Clock	105	Output	AG21	3.3v	LVCMOS33
Video Horizontal Sync	133	Output	W24	1.5v	LVCMOS15
Video Vertical Sync	113	Output	AF22	3.3v	LVCMOS33
Video Display Enable	67	Output	AD18	1.5v	LVCMOS15
Video Data 0 Luma[0]	135	Output	W25	1.5v	LVCMOS15
Video Data 0 Luma[1]	137	Output	W26	1.5v	LVCMOS15
Video Data 0 Luma[2]	116	Output	V27	1.5v	LVCMOS15
Video Data 0 Luma[3]	118	Output	W28	1.5v	LVCMOS15
Video Data 0 Luma[4]	124	Output	W29	1.5v	LVCMOS15
Video Data 0 Luma[5]	126	Output	W30	1.5v	LVCMOS15
Video Data 0 Luma[6]	128	Output	V28	1.5v	LVCMOS15
Video Data 0 Luma[7]	130	Output	V29	1.5v	LVCMOS15
Video Data 0 Luma[8]	132	Output	T30	1.5v	LVCMOS15
Video Data 0 Luma[9]	134	Output	U30	1.5v	LVCMOS15
Video Data 1 Luma[0]	117	Output	AG22	3.3v	LVCMOS33
Video Data 1 Luma[1]	119	Output	AH22	3.3v	LVCMOS33
Video Data 1 Luma[2]	121	Output	AJ21	3.3v	LVCMOS33
Video Data 1 Luma[3]	123	Output	AK21	3.3v	LVCMOS33
Video Data 1 Luma[4]	125	Output	AF23	3.3v	LVCMOS33
Video Data 1 Luma[5]	127	Output	AF24	3.3v	LVCMOS33
Video Data 1 Luma[6]	92	Output	AJ23	3.3v	LVCMOS33
Video Data 1 Luma[7]	94	Output	AJ24	3.3v	LVCMOS33

Video Data 1 Luma[8]	96	Output	AG24	3.3v	LVCMOS33
Video Data 1 Luma[9]	98	Output	AG25	3.3v	LVCMOS33
Video Data 2 Luma[0]	77	Output	AJ16	3.3v	LVCMOS33
Video Data 2 Luma[1]	79	Output	AK16	3.3v	LVCMOS33
Video Data 2 Luma[2]	81	Output	AH17	3.3v	LVCMOS33
Video Data 2 Luma[3]	83	Output	AH16	3.3v	LVCMOS33
Video Data 2 Luma[4]	85	Output	AH18	3.3v	LVCMOS33
Video Data 2 Luma[5]	87	Output	AJ18	3.3v	LVCMOS33
Video Data 2 Luma[6]	78	Output	AF13	3.3v	LVCMOS33
Video Data 2 Luma[7]	82	Output	AG15	3.3v	LVCMOS33
Video Data 2 Luma[8]	84	Output	AG17	3.3v	LVCMOS33
Video Data 2 Luma[9]	86	Output	AG16	3.3v	LVCMOS33
Video Data 3 Luma[0]	107	Output	AH21	3.3v	LVCMOS33
Video Data 3 Luma[1]	122	Output	AH29	3.3v	LVCMOS33
Video Data 3 Luma[2]	115	Output	AE22	3.3v	LVCMOS33
Video Data 3 Luma[3]	146	Output	AF28	3.3v	LVCMOS33
Video Data 3 Luma[4]	148	Output	AF29	3.3v	LVCMOS33
Video Data 3 Luma[5]	150	Output	AG29	3.3v	LVCMOS33
Video Data 3 Luma[6]	100	Output	AH23	3.3v	LVCMOS33
Video Data 3 Luma[7]	102	Output	AH24	3.3v	LVCMOS33
Video Data 3 Luma[8]	104	Output	AJ25	3.3v	LVCMOS33
Video Data 3 Luma[9]	106	Output	AK25	3.3v	LVCMOS33
Video Data 0 Chroma[0]	143	Output	T29	1.5v	LVCMOS15
Video Data 0 Chroma[1]	145	Output	U29	1.5v	LVCMOS15
Video Data 0 Chroma[2]	147	Output	R28	1.5v	LVCMOS15
Video Data 0 Chroma[3]	149	Output	T28	1.5v	LVCMOS15
Video Data 0 Chroma[4]	151	Output	P30	1.5v	LVCMOS15
Video Data 0 Chroma[5]	153	Output	R30	1.5v	LVCMOS15
Video Data 0 Chroma[6]	155	Output	N29	1.5v	LVCMOS15
Video Data 0 Chroma[7]	157	Output	P29	1.5v	LVCMOS15
Video Data 0 Chroma[8]	159	Output	N28	1.5v	LVCMOS15
Video Data 0 Chroma[9]	161	Output	P28	1.5v	LVCMOS15
Video Data 1 Chroma[0]	89	Output	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[1]	91	Output	AK18	3.3v	LVCMOS33
Video Data 1 Chroma[2]	93	Output	AF19	3.3v	LVCMOS33
Video Data 1 Chroma[3]	95	Output	AG19	3.3v	LVCMOS33
Video Data 1 Chroma[4]	97	Output	AH19	3.3v	LVCMOS33
Video Data 1 Chroma[5]	99	Output	AJ19	3.3v	LVCMOS33
Video Data 1 Chroma[6]	101	Output	AF20	3.3v	LVCMOS33
Video Data 1 Chroma[7]	103	Output	AG20	3.3v	LVCMOS33
Video Data 1 Chroma[8]	109	Output	AJ20	3.3v	LVCMOS33
Video Data 1 Chroma[9]	111	Output	AK20	3.3v	LVCMOS33
Video Data 2 Chroma[0]	38	Output	AE12	3.3v	LVCMOS33

7.2.2 Video Data Signals (Output)

The output of the H.264 4k decoder module is the decoded video data in YUV format (4:2:2 or 4:2:0), with 40 output lines: **Video Data 0 Luma[0]** to **Video Data 3 Luma[9]**, for Luma. And, 40 lines: **Video Data 0 Chroma[0]** to **Video Data 3 Chroma[9]**, for the Chroma. The precision can be either 8-bit precision or 10-bit precision. For 8-bit precision, the Most Significant Bits of luma and chroma output lines (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are provided for frame synchronization. The Video **Display Enable signal** is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels.

7.2.3 Audio Data Signals (Output)

Line **SPDIF Audio** is for PCM audio output, in **SPDIF** frames. An **SPDIF** transmitter is included in the module to send the PCM data out via the decoder edge pins. Refer to the **SPDIF** protocol documents for details.

7.2.4 Decoder Control Signals (Input and output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the decoder. **Uart_rx** receives the command from external control device. **Uart_tx** send the decoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Decoder API User Manual for details.

7.3 Power Rails of MCM-1000Z

The power rails for H.264 4K decoder for 4k@30 or 4k@60 are the same and are also the same as the H.264 4k encoder. Refer to Appendix-C for the pins of power and ground on the edge connector of the MCM-1000Z module.

7.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 3 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-10 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 4k@60 resolution, and can be used for PCB design. It should be noted that the power rails 1.8v and 2.0v are generated on the module using the input power rails. PCB designers for the carrier boards need not to consider these two rails.

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards. The VTR-4000C, discussed in Section

12. Carrier Board PCB Reference Designs

SOC has several evaluation boards for evaluating the standard encoder and decoder modules (and for evaluating the IP cores as well). These evaluation boards provide not only the DDR3 SODIMM connectors for connecting the encoder (and/or decoder) modules, but also the commonly used digital video/audio ports, such as SDI and HDMI. Ethernet port of tri-speed, 10/100/1000Mbps, as a network connection, is used in all of the SOC evaluation boards.

12.1 VTR-S1000 Evaluation Board

Fig. 11 shows a photo of the VTR-S1000 board. Major components and I/O ports are marked in the figure. Refer to the User Guide of VTR -S1000 for further details.

SOC licenses the Schematics of VTR-S1000 to the customers that have purchased the eval kit VTR-S1000 and encoder (or decoder) Modules. Firmware of the VTR-S1000, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, sales@soctechnologies.com, for details.

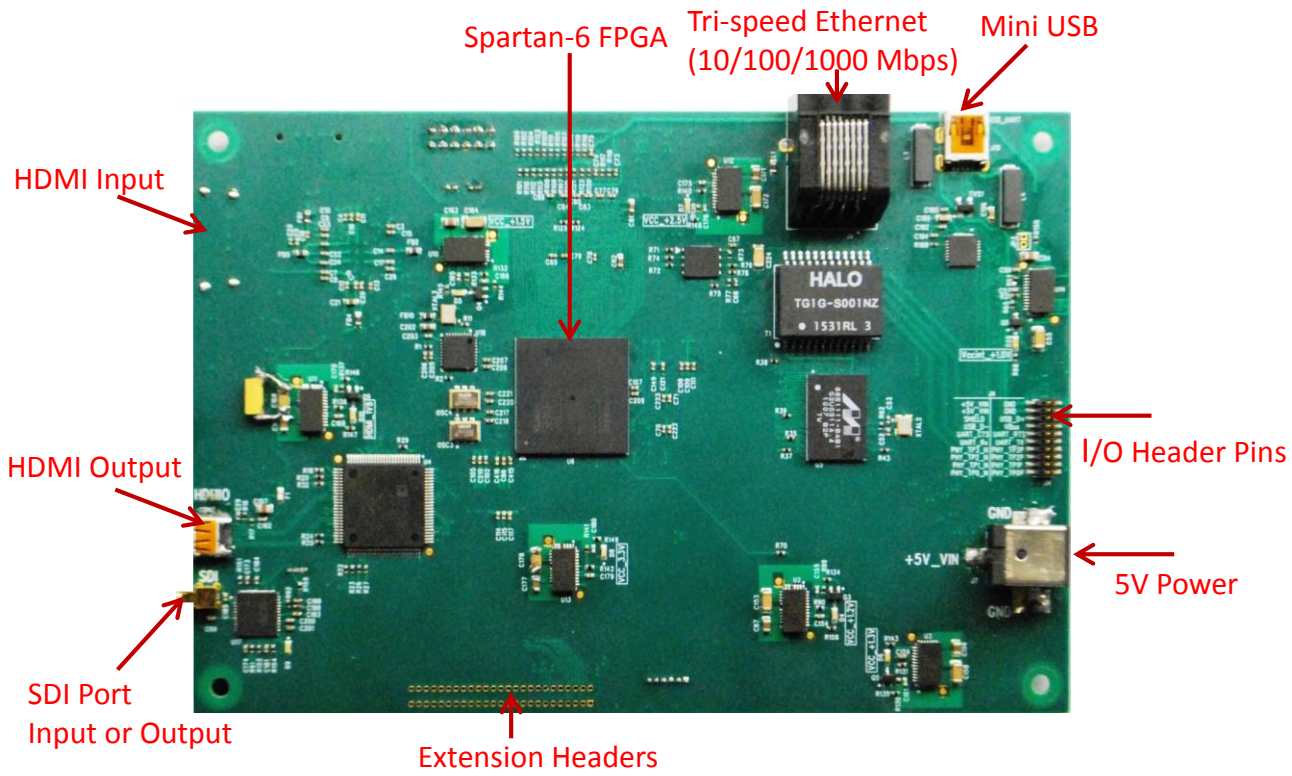

Fig. 11. FMC-MCM-1000 evaluation board

13. Ordering Information

Fig. 13 shows the product code naming convention for the SOC MPEG codec modules and IP cores. Non-standard codec modules can be ordered following the same naming format (minimum order quantity is required for non-standard modules).

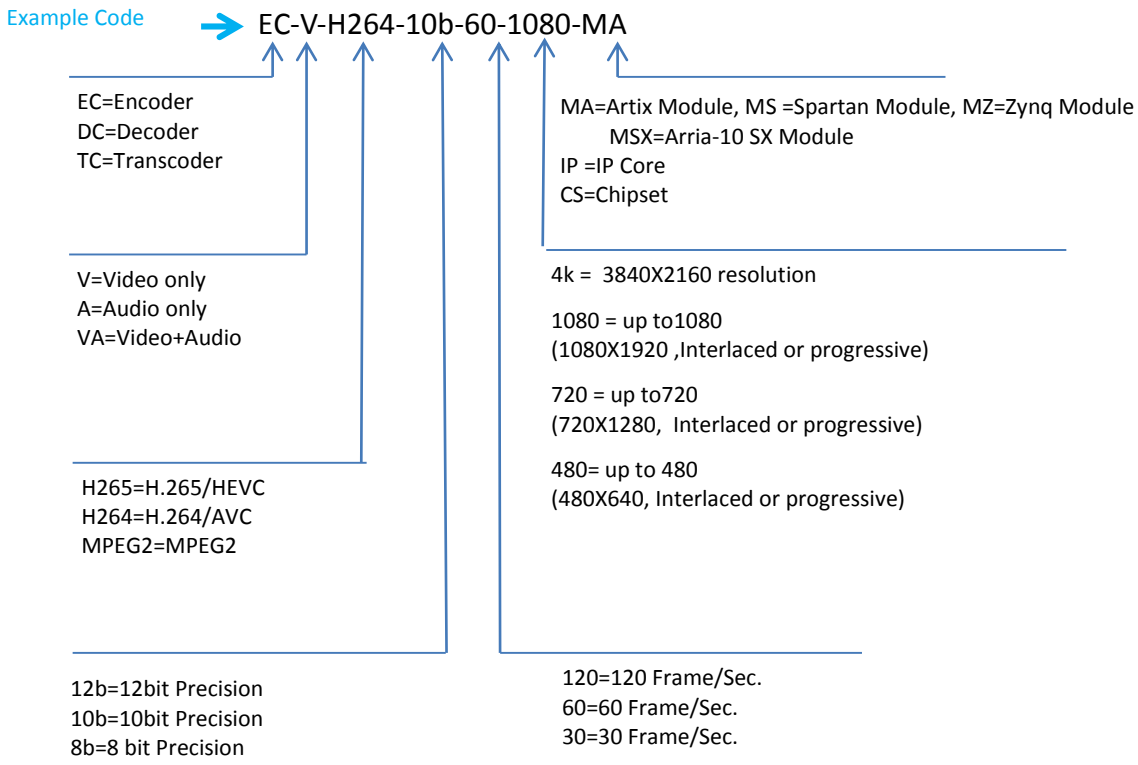

Fig. 13 SOC MPEG codec (IP cores and modules) product code naming convention

14. Contact Information

Please contact SOC head office or distributor for product details and to place an order.

Head Office

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E-mail: sales@soctechnologies.com

A.5 MPEG-2 Decoder Modules

Table-A9 lists the standard MPEG-2 video decoder modules. Table-A10 lists the MPEG-2 video/audio decoder modules. The 10-bit precision and 60 frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A9: MPEG-2 Video Decoder Modules (video only without audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-MPEG2-8b-30-720-MS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000S
DC-V-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
DC-V-MPEG2-8b-30-1080-MS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000S
DC-V-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A

Table-A10: MPEG-2 Video&Audio Decoder Modules (both video and audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-V-MPEG2-8b-30-720-MS	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000S
DC-V-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-V-MPEG2-8b-30-1080-MS	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000S
DC-V-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A

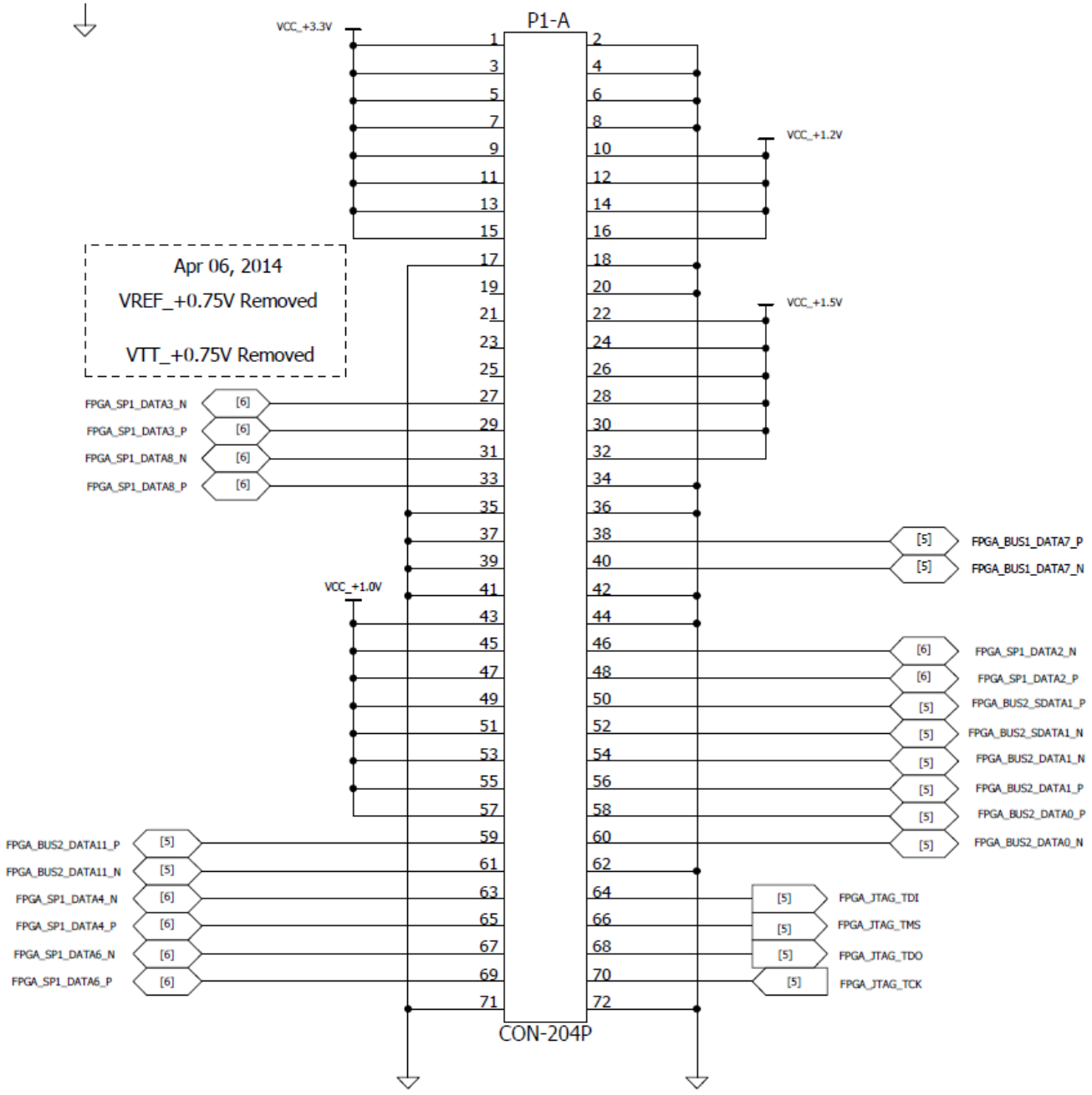
A.6 H.264-to-H.265 Transcoder Modules

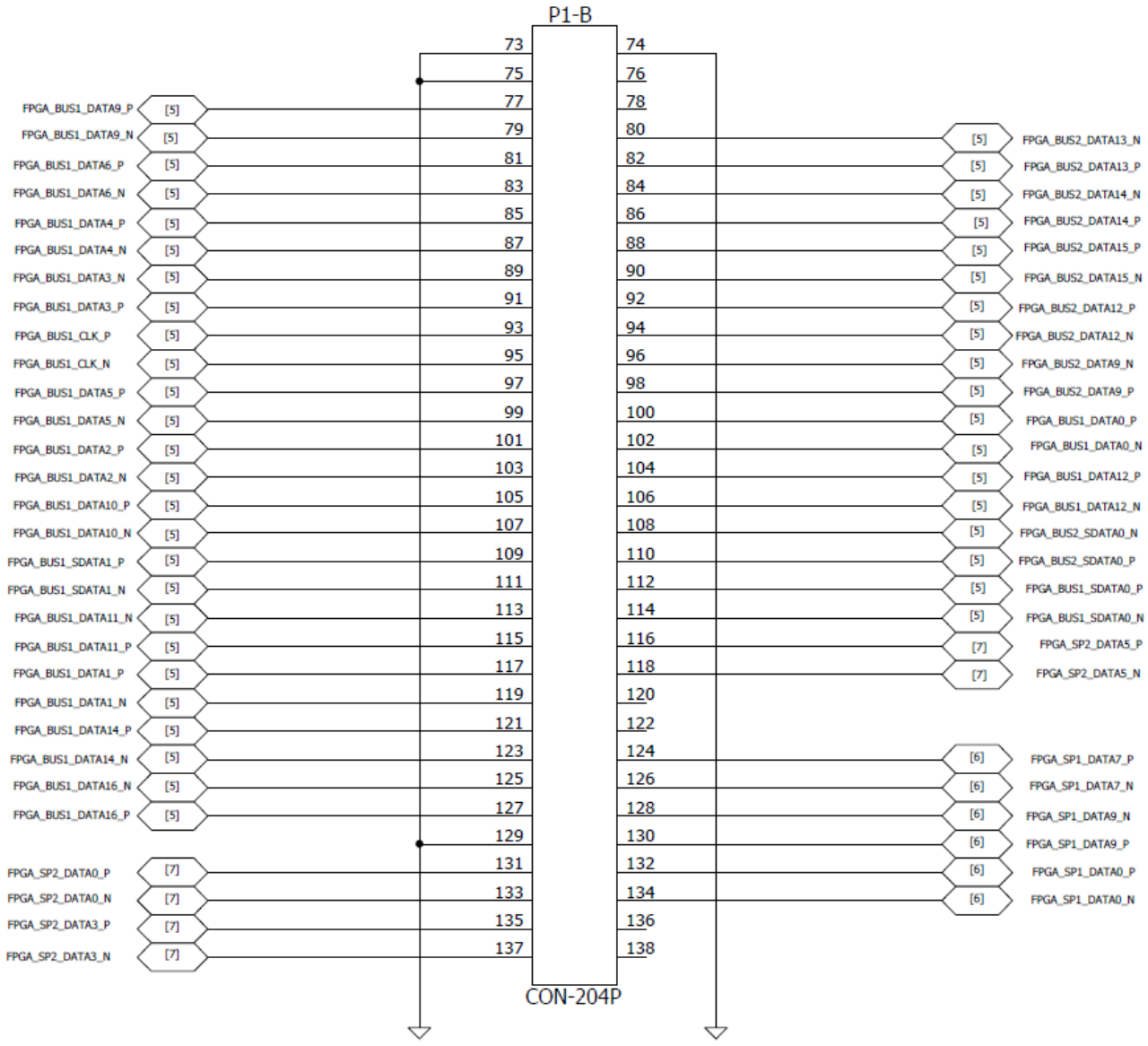
Table-A11 lists the standard H.264-to-H.265 video transcoder modules. Table-A12 lists the H.264-to-H.265 video/audio transcoder modules.

Table-A11: H.264-to-H.265 Video Transcoder Modules (video only without audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
TC-V-H.264-to-H.265-8b-30-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000Z
TC-V-H.264-to-H.265-10b-30-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 30fps	no	MCM-1000Z
TC-V- H.264-to-H.265-8b-60-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000Z
TC-V- H.264-to-H.265-10b-60-720-MZ	H.265	Main 4:2:2	up to 720i/p	up to 4:2:2	10 bits	up to 60fps	no	MCM-1000Z
TC-V- H.264-to-H.265-8b-30-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 30fps	no	MCM-1000Z
TC-V- H.264-to-H.265-10b-30-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 30fps	no	MCM-1000Z
TC-V- H.264-to-H.265-8b-60-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	8 bits	up to 60fps	no	MCM-1000Z
TC-V- H.264-to-H.265-10b-60-1080-MZ	H.265	Main 4:2:2	up to 1080i/p	up to 4:2:2	10 bits	up to 60fps	no	MCM-1000Z

Appendix - B MCM-1000A Edge Connector Schematics




P1-B
CON-204P
FPGA_BUS1_DATA9_P
FPGA_BUS1_DATA9_N
FPGA_BUS1_DATA6_P
FPGA_BUS1_DATA6_N
FPGA_BUS1_DATA4_P
FPGA_BUS1_DATA4_N
FPGA_BUS1_DATA3_N
FPGA_BUS1_DATA3_P
FPGA_BUS1_CLK_P
FPGA_BUS1_CLK_N
FPGA_BUS1_DATA5_P
FPGA_BUS1_DATA5_N
FPGA_BUS1_DATA2_P
FPGA_BUS1_DATA2_N
FPGA_BUS1_DATA10_P
FPGA_BUS1_DATA10_N
FPGA_BUS1_SDATA1_P
FPGA_BUS1_SDATA1_N
FPGA_BUS1_DATA11_N
FPGA_BUS1_DATA11_P
FPGA_BUS1_DATA1_P
FPGA_BUS1_DATA1_N
FPGA_BUS1_DATA14_P
FPGA_BUS1_DATA14_N
FPGA_BUS1_DATA16_N
FPGA_BUS1_DATA16_P
FPGA_SP2_DATA0_P
FPGA_SP2_DATA0_N
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FPGA_BUS2_DATA13_P
FPGA_BUS2_DATA14_N
FPGA_BUS2_DATA14_P
FPGA_BUS2_DATA15_P
FPGA_BUS2_DATA15_N
FPGA_BUS2_DATA12_P
FPGA_BUS2_DATA12_N
FPGA_BUS2_DATA9_N
FPGA_BUS2_DATA9_P
FPGA_BUS1_DATA0_P
FPGA_BUS1_DATA0_N
FPGA_BUS1_DATA12_P
FPGA_BUS1_DATA12_N
FPGA_BUS2_SDATA0_N
FPGA_BUS2_SDATA0_P
FPGA_BUS1_SDATA0_P
FPGA_BUS1_SDATA0_N
FPGA_SP2_DATA5_P
FPGA_SP2_DATA5_N
FPGA_SP1_DATA7_P
FPGA_SP1_DATA7_N
FPGA_SP1_DATA9_N
FPGA_SP1_DATA9_P
FPGA_SP1_DATA0_P
FPGA_SP1_DATA0_N