System-On-Chip (SOC) Technologies Inc. - EC-VA-H264-10B-60-1080-MXC-SL Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	FPGA Core
Core Processor	Artix-7 A200T
Co-Processor	-
Speed	-
Flash Size	32MB
RAM Size	256KB
Connector Type	SO-DIMM-204
Size / Dimension	2.7" x 2.0" (68mm x 51mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/soc-technologies/ec-va-h264-10b-60-1080-mxc-sl

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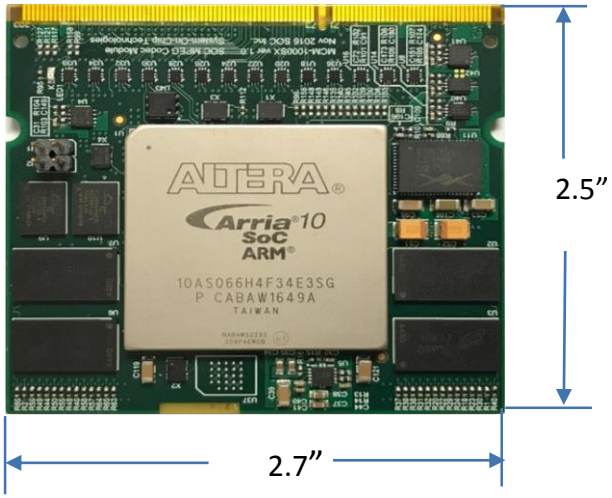

Fig. 5. Dimension of MCM-1000SX

2. Connecting the Module to a User PCB

The MCM-1000S/A/Z/SX modules have identical edge pins that are compatible with standard DDR3 SODIMM connectors. The following off-the-shelf DDR3 SODIMM connectors can be used to connect the SOC codec modules onto a user PCB:

1. MM80-204B1-1
2. MM80-204B1-1E
3. AS0A621-U2SN-7F
4. AS0A621-H2S6-7H

Fig. 6 shows a photo of a standard 204 pin DDR3 SODIMM PCB connector. Refer to the datasheet of the connector used for the physical dimension and PCB design requirements.

Fig. 6 A photo of the standard 204 pin DDR3 SODIMM connector

3. Overview SOC Standard Codec Modules

Each of the above described SOMs: the **MCM-1000S** (based on Spatran-6 FPGA), **MCM-1000A** (based on Artix-7 FPGA), **MCM-1000Z** (based on Zynq-7 FPGAs), and **MCM-1000SX** (based on Altera Arria-10 FPGAs); can be configured into different products by down-loading the desired firmware. At SOC, we produce encoder, decoder, transcoder, and multi-channel encoder or decoder SOMs for video compressions, by down-loading **SOC MPEG Codec IP** cores onto the modules.

The standard encoder modules: H.265, H.264, and MPEG-2, take raw video and audio as input and output TS streams, via the edge pins of the modules, as shown in Fig. 7. The standard decoder modules: H.265, H.264, and MPEG-2, take TS stream as inputs and output decoded video and audio, via the edge pins of the modules, as shown in Fig. 8. There are also control signal pins, to allow the user control of the encoder or decoder.

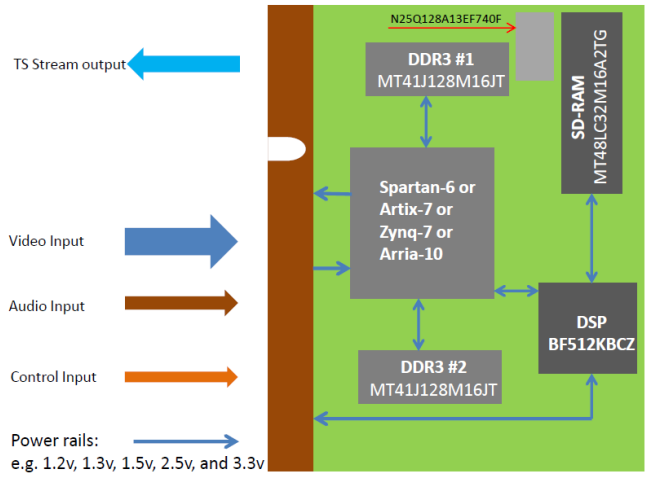

Fig. 7 SOC Standard encoder modules (H.265, H.264, or MPEG-2)

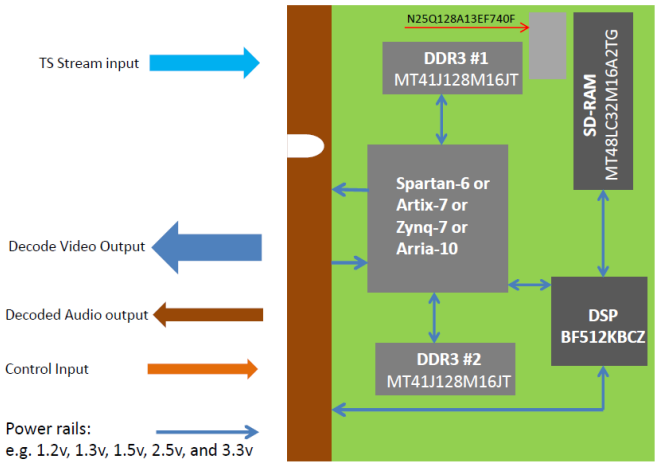

Fig. 8 SOC Standard decoder modules (H.265, H.264, or MPEG-2)

4. The H.264 (and MPEG-2) HD Encoder Modules

4.1 Pin Assignments and Pin Voltages

The HD encoder modules for H.264 and MPEG-2 have the same pin assignments and electrical properties. The hardware module for HD resolution uses the MCM-1000A (the Artix-7 A200T FPGA), the hardware module MCM-1000Z is used for 4k resolutions (the Zynq-7035 for 4k@30, Zynq-7045 for 4k@60).

This Section provides the pin assignments and electrical properties for HD encoder (H.264, or MPEG-2) module which is based on the MCM-1000A. Table-1 lists the pin assignments and the pin voltages.

The schematics of MCM-1000A edge connector are attached in Appendix-B of this document, which shows the pin numbers for data, clock, control, and power. It should be noted that the encoder module uses only some of the edge pins, and not all of the edge pins are used.

Table-1 also lists the FPGA pin numbers that are connected to the edge pins assigned to the encoder. The Artix-7 datasheet provides further information regarding the properties of these pins, and can be used as a r reference.

Table 1: HD Encoder Module (based on MCM-1000A) Pin Assignment and Pin Voltages

Description	MCM-1000A Edge Connector Pin #	Direction	FPGA Pin #	Voltage	IO Standard
External Reset	121	Input	W21	3.3v	LVCMOS33
Video Clock	105	Input	Y11	3.3v	LVCMOS33
Video Horizontal Sync	146	Input	W16	3.3v	LVCMOS33
Video Vertical Sync	148	Input	V15	3.3v	LVCMOS33
Video Display Enable	150	Input	U15	3.3v	LVCMOS33
Video Data Luma[0]	50	Input	W14	3.3v	LVCMOS33
Video Data Luma[1]	52	Input	Y14	3.3v	LVCMOS33
Video Data Luma[2]	58	Input	V10	3.3v	LVCMOS33
Video Data Luma[3]	59	Input	Y13	3.3v	LVCMOS33
Video Data Luma[4]	60	Input	W10	3.3v	LVCMOS33
Video Data Luma[5]	61	Input	AA14	3.3v	LVCMOS33
Video Data Luma[6]	80	Input	AB13	3.3v	LVCMOS33
Video Data Luma[7]	82	Input	AA13	3.3v	LVCMOS33
Video Data Luma[8]	84	Input	AB17	3.3v	LVCMOS33
Video Data Luma[9]	86	Input	AB16	3.3v	LVCMOS33
Video Data Chroma[0]	92	Input	AA15	3.3v	LVCMOS33
Video Data Chroma[1]	94	Input	AB15	3.3v	LVCMOS33
Video Data Chroma[2]	96	Input	AB12	3.3v	LVCMOS33
Video Data Chroma[3]	98	Input	AB11	3.3v	LVCMOS33
Video Data Chroma[4]	107	Input	Y12	3.3v	LVCMOS33
Video Data Chroma[5]	108	Input	W12	3.3v	LVCMOS33
Video Data Chroma[6]	110	Input	Y17	3.3v	LVCMOS33
Video Data Chroma[7]	140	Input	T14	3.3v	LVCMOS33
Video Data Chroma[8]	142	Input	T15	3.3v	LVCMOS33
Video Data Chroma[9]	144	Input	W15	3.3v	LVCMOS33
SPDIF Audio	109	Input	Y21	3.3v	LVCMOS33

Transport Stream Buffer Ready	112	Input	AA20	3.3v	LVCMOS33
Transport Stream Clock	93	Output	Y18	3.3v	LVCMOS33
Transport Stream Data Valid	106	Output	R17	3.3v	LVCMOS33
Transport Stream Data[0]	77	Output	N13	3.3v	LVCMOS33
Transport Stream Data[1]	79	Output	N14	3.3v	LVCMOS33
Transport Stream Data[2]	81	Output	R18	3.3v	LVCMOS33
Transport Stream Data[3]	83	Output	T18	3.3v	LVCMOS33
Transport Stream Data[4]	85	Output	U17	3.3v	LVCMOS33
Transport Stream Data[5]	87	Output	U18	3.3v	LVCMOS33
Transport Stream Data[6]	89	Output	AB18	3.3v	LVCMOS33
Transport Stream Data[7]	91	Output	AA18	3.3v	LVCMOS33
Transport Stream Start Code	40	Output	V19	3.3v	LVCMOS33
Uart_tx	90	Output	AA16	3.3v	LVCMOS33
Uart_rx	88	Input	Y16	3.3v	LVCMOS33

4.2 Signal Formats

4.2.1 Video Clock Signal (Input)

The **Video Clock** signal (pin # 105) has two functions: (1) It is the clock for the input video data, and (2) it is the clock that drives the encoder engine.

The **Video Clock** signal usually comes from the video input interface chip, such as HDMI or SDI. It is the clock for the input video data. It is also used for driving the encoder engine. The frequency varies according to the resolution of the video input. The following are the clock frequencies for standard video resolutions.

1. 27MHz, for SD resolution
2. 74.25MHz, for 720@60 and 1080@30
3. 148.5MHz, for 1080@60

4.2.2 Video Data Signals (Input)

The input to the encoder module (H.264 or MPEG-2) is raw video data in YUV format (4:2:2 or 4:2:0), with 10 input lines: **Video Data Luma[0]** to **Video Data Luma[9]**, for Luma. And, 10 input lines: **Video Data Chroma[0]** to **Video Data Chroma[9]**, for the Chroma. The precision can be either 8-bit or 10-bit. When 8-bit precision is used, **Video Data Luma[0]** , **Video Data Luma[1]**, **Video Data Chroma[0]**, and **Video Data Chroma[1]** are zeros.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization. A **Video Clock** (refer to Section **4.2.1** for the clock frequencies) is required, which provides the timing for the parallel input of luma, chroma, as well as for the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal (pin #150) is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Display Enable signal** at high, when active pixels are being sent out.
The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **4.2.1.**

4.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 2 to 5 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails, each individual power rail deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-3 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 1080p@60 resolution, which can be used as a reference for PCB design. It should be noted that the measured real power consumption is about 20% lower than the estimated power consumption.

It should be noted that the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-2, as the 1.8v is generated on the module.

Table-3: Power estimation for the encoder module (1080p@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	3.792	3.723	0.069
Vccaux	1.800	0.454	0.421	0.034
Vcco33	3.300	0.013	0.008	0.005
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.499	0.494	0.005
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.063	0.052	0.011
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.022	0.002	0.020

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 12 of this document. The reference designs provide not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for design licensing details.

estimation by Xilinx Vivado FPGA software for each rail, at 1080p@60 resolution, and can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-5 is higher than the measured real power.

Again, the power rails of 1.8v is generated on the module, using the 2.5v power input from the edge pin. PCB designers need only to design the 6 power rails listed in Table-5.

Table-5: Power estimation for the decoder module (1080p@60 resolution)

Power Supply				
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	2.421	2.362	0.058
Vccaux	1.800	0.497	0.464	0.033
Vcco33	3.300	0.053	0.048	0.005
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.500	0.495	0.005
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.037	0.028	0.009
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.022	0.002	0.020

Since the decoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both. SOC licenses the schematics of carrier boards, such as the VTR-S1000 and VTR-4000C discussed in Section 6 of this document. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for further details.

Chroma[9], for the Chroma. The precision is either 8 bits or 10 bits. For 8-bit precision, the Most Significant Luma and Chroma pins (Luma[2] to Luma[9], Chroma[2] to Chroma[9]) are used.

In addition to the video Luma and Chroma data signals, the **Video Horizontal Sync** and **Video Vertical Sync** signals are required for frame synchronization if embedded SAV/EAV are not used. The video clocks (refer to Section **6.2.1**) provide the timing for the parallel input of luma, chroma, as well as the **Video Horizontal Sync** and **Video Vertical Sync signals**. The **Video Display Enable** signal is a part of the **Video Horizontal Sync** and **Video Vertical Sync** system, where high signal indicates active video pixels. For example, an HDMI input interface chip will output the **Video Display Enable** signal at high, when active pixels are being sent out.

The video data are sampled at the rising edge of the clock. The clock rates will correspond to the resolution and frame rate, as discussed in Section **6.2.1.**

6.2.3 Audio Data Signals (Input)

Input line **SPDIF Audio** is for PCM audio input, in **SPDIF** frames. An **SPDIF** transmitter is required to send the PCM data to the encoder module. Refer to the **SPDIF** protocol documents for details.

6.2.4 TS stream Signals (Output)

The output of the encoder module is MPEG Transport Stream (TS), which is sent out from the module by 8 parallel lines: **Transport Stream Data[0]** to **Transport Stream Data[7],** along with the Transport Stream output data clock **Transport Stream Clock** (pin # 31). The frequency of the Transport Stream Data clock is 27MHz.

Transport Stream Buffer Ready (pin # 28) and **Transport Stream Data Valid** (pin # 33) are the signals to inform the user side to take over the signals.

6.2.5 Encoder Control Signals (Input and Output)

Uart_rx and **Uart_tx** are the API pins for controlling the operations of the encoder. **Uart_rx** receives the command from external control device. **Uart_tx** sends the encoder information to the control device. Refer to the **Uart** standard for details of **Uart** operations. The SOC API User Manual provides the register map for the API control. Refer to the Encoder API User Manual for more details.

An external reset **PS Soft Reset_B** (pin # 156) is available. This pin allows the user to reset the encoder when necessary. A low signal will trigger a reset. The reset signal should be maintained at high or left unconnected when in normal operation mode.

6.3 Power Rails of MCM-1000Z

Refer to Appendix-B for the pins of power and ground on the edge connector of the MCM-1000Z module. The power rails are: 1.0V, 1.2V, 1.3V, 1.5V, 2.5V, and 3.3V.

6.4 Power Requirement and Supply Amperage

The total power, at operation, required by a given encoder module ranges from 3 to 6 watts, depending on the resolution and frame rate. Since the total power is delivered over 6 power rails (1.0v, 1.2v, 1.3v, 1.5v, 2.5v, and 3.3v), each individual power rails deliveries only a portion of the total power. However, the power is not evenly distributed among the rails. Table-7 lists the power estimation by Xilinx Vivado FPGA software for each rail, at 4k@60 resolution, which can be used as a reference for PCB design. It should be noted that the estimated total power showing in Table-7 is higher than the measured real power of the module. However, for PCB design purposes, Table-7 is sufficient. It should also be noted that the power rails 1.8v and 2.0v are generated on the module, by using some of the input power rails. Carrier board PCB designers need not to consider these two rails.

Table-7: Power estimation for the H.264 4k encoder module (4k@60 resolution)

Power Supply

Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	5.462	5.351	0.111
Vccaux	1.800	0.558	0.500	0.058
Vcco33	3.300	0.006	0.005	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.001	0.000	0.001
Vcco15	1.500	0.429	0.428	0.001
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	2.000	0.109	0.109	0.000
Vccbram	1.000	0.083	0.057	0.026
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
MGTVccaux	1.800	0.000	0.000	0.000
Vccpint	1.000	0.750	0.723	0.027
Vccpaux	1.800	0.061	0.051	0.010
Vccpll	1.800	0.019	0.016	0.003
Vcco_ddr	1.500	0.459	0.457	0.002
Vcco_mio0	1.800	0.007	0.006	0.001
Vcco_mio1	1.800	0.001	0.000	0.001
Vccadc	1.800	0.022	0.002	0.020

Since the encoder module normally shares the power supplies with the carrier board (user PCB). The power design should be considered for both the module and the carrier board. SOC licenses the schematics of carrier boards. The VTR-4000C discussed in Section 12 of this document is for 4k resolution. The reference design provides not only the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Contact SOC sale at: sales@soctechnologies.com for design licensing information.

Video Data 1 Luma[8]	96	Output	AG24	3.3v	LVCMOS33
Video Data 1 Luma[9]	98	Output	AG25	3.3v	LVCMOS33
Video Data 2 Luma[0]	77	Output	AJ16	3.3v	LVCMOS33
Video Data 2 Luma[1]	79	Output	AK16	3.3v	LVCMOS33
Video Data 2 Luma[2]	81	Output	AH17	3.3v	LVCMOS33
Video Data 2 Luma[3]	83	Output	AH16	3.3v	LVCMOS33
Video Data 2 Luma[4]	85	Output	AH18	3.3v	LVCMOS33
Video Data 2 Luma[5]	87	Output	AJ18	3.3v	LVCMOS33
Video Data 2 Luma[6]	78	Output	AF13	3.3v	LVCMOS33
Video Data 2 Luma[7]	82	Output	AG15	3.3v	LVCMOS33
Video Data 2 Luma[8]	84	Output	AG17	3.3v	LVCMOS33
Video Data 2 Luma[9]	86	Output	AG16	3.3v	LVCMOS33
Video Data 3 Luma[0]	107	Output	AH21	3.3v	LVCMOS33
Video Data 3 Luma[1]	122	Output	AH29	3.3v	LVCMOS33
Video Data 3 Luma[2]	115	Output	AE22	3.3v	LVCMOS33
Video Data 3 Luma[3]	146	Output	AF28	3.3v	LVCMOS33
Video Data 3 Luma[4]	148	Output	AF29	3.3v	LVCMOS33
Video Data 3 Luma[5]	150	Output	AG29	3.3v	LVCMOS33
Video Data 3 Luma[6]	100	Output	AH23	3.3v	LVCMOS33
Video Data 3 Luma[7]	102	Output	AH24	3.3v	LVCMOS33
Video Data 3 Luma[8]	104	Output	AJ25	3.3v	LVCMOS33
Video Data 3 Luma[9]	106	Output	AK25	3.3v	LVCMOS33
Video Data 0 Chroma[0]	143	Output	T29	1.5v	LVCMOS15
Video Data 0 Chroma[1]	145	Output	U29	1.5v	LVCMOS15
Video Data 0 Chroma[2]	147	Output	R28	1.5v	LVCMOS15
Video Data 0 Chroma[3]	149	Output	T28	1.5v	LVCMOS15
Video Data 0 Chroma[4]	151	Output	P30	1.5v	LVCMOS15
Video Data 0 Chroma[5]	153	Output	R30	1.5v	LVCMOS15
Video Data 0 Chroma[6]	155	Output	N29	1.5v	LVCMOS15
Video Data 0 Chroma[7]	157	Output	P29	1.5v	LVCMOS15
Video Data 0 Chroma[8]	159	Output	N28	1.5v	LVCMOS15
Video Data 0 Chroma[9]	161	Output	P28	1.5v	LVCMOS15
Video Data 1 Chroma[0]	89	Output	AK17	3.3v	LVCMOS33
Video Data 1 Chroma[1]	91	Output	AK18	3.3v	LVCMOS33
Video Data 1 Chroma[2]	93	Output	AF19	3.3v	LVCMOS33
Video Data 1 Chroma[3]	95	Output	AG19	3.3v	LVCMOS33
Video Data 1 Chroma[4]	97	Output	AH19	3.3v	LVCMOS33
Video Data 1 Chroma[5]	99	Output	AJ19	3.3v	LVCMOS33
Video Data 1 Chroma[6]	101	Output	AF20	3.3v	LVCMOS33
Video Data 1 Chroma[7]	103	Output	AG20	3.3v	LVCMOS33
Video Data 1 Chroma[8]	109	Output	AJ20	3.3v	LVCMOS33
Video Data 1 Chroma[9]	111	Output	AK20	3.3v	LVCMOS33
Video Data 2 Chroma[0]	38	Output	AE12	3.3v	LVCMOS33

6 of this document, is for 4k resolution. The reference designs not only provide the power system design, but also the I/O port designs, such as SDI, HDMI, Mini-USB, etc. Please contact SOC sale at: sales@soctechnologies.com for further details.

Table-10: Power estimation for the decoder module (4K@60 resolution)

Power Supply

Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	4.786	4.682	0.104
Vccaux	1.800	0.692	0.634	0.058
Vcco33	3.300	0.007	0.006	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.001	0.000	0.001
Vcco15	1.500	0.429	0.428	0.001
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	2.000	0.109	0.109	0.000
Vccbram	1.000	0.093	0.074	0.019
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
MGTVccaux	1.800	0.000	0.000	0.000
Vccpint	1.000	0.750	0.723	0.026
Vccpaux	1.800	0.061	0.051	0.010
Vccpll	1.800	0.019	0.016	0.003
Vcco_ddr	1.500	0.459	0.457	0.002
Vcco_mio0	1.800	0.007	0.006	0.001
Vcco_mio1	1.800	0.001	0.000	0.001
Vccadc	1.800	0.022	0.002	0.020

8. The H.265 HD Encoder Modules

To be added

9. The H.265 HD Decoder Modules

To be added

10. The H.265 4k Encoder Modules

To be added

11. The H.265 4k Decoder Modules

To be added

12. Carrier Board PCB Reference Designs

SOC has several evaluation boards for evaluating the standard encoder and decoder modules (and for evaluating the IP cores as well). These evaluation boards provide not only the DDR3 SODIMM connectors for connecting the encoder (and/or decoder) modules, but also the commonly used digital video/audio ports, such as SDI and HDMI. Ethernet port of tri-speed, 10/100/1000Mbps, as a network connection, is used in all of the SOC evaluation boards.

12.1 VTR-S1000 Evaluation Board

Fig. 11 shows a photo of the VTR-S1000 board. Major components and I/O ports are marked in the figure. Refer to the User Guide of VTR -S1000 for further details.

SOC licenses the Schematics of VTR-S1000 to the customers that have purchased the eval kit VTR-S1000 and encoder (or decoder) Modules. Firmware of the VTR-S1000, including I/O drivers and network IP core, is also available for licensing. Please contact SOC sales, sales@soctechnologies.com, for details.

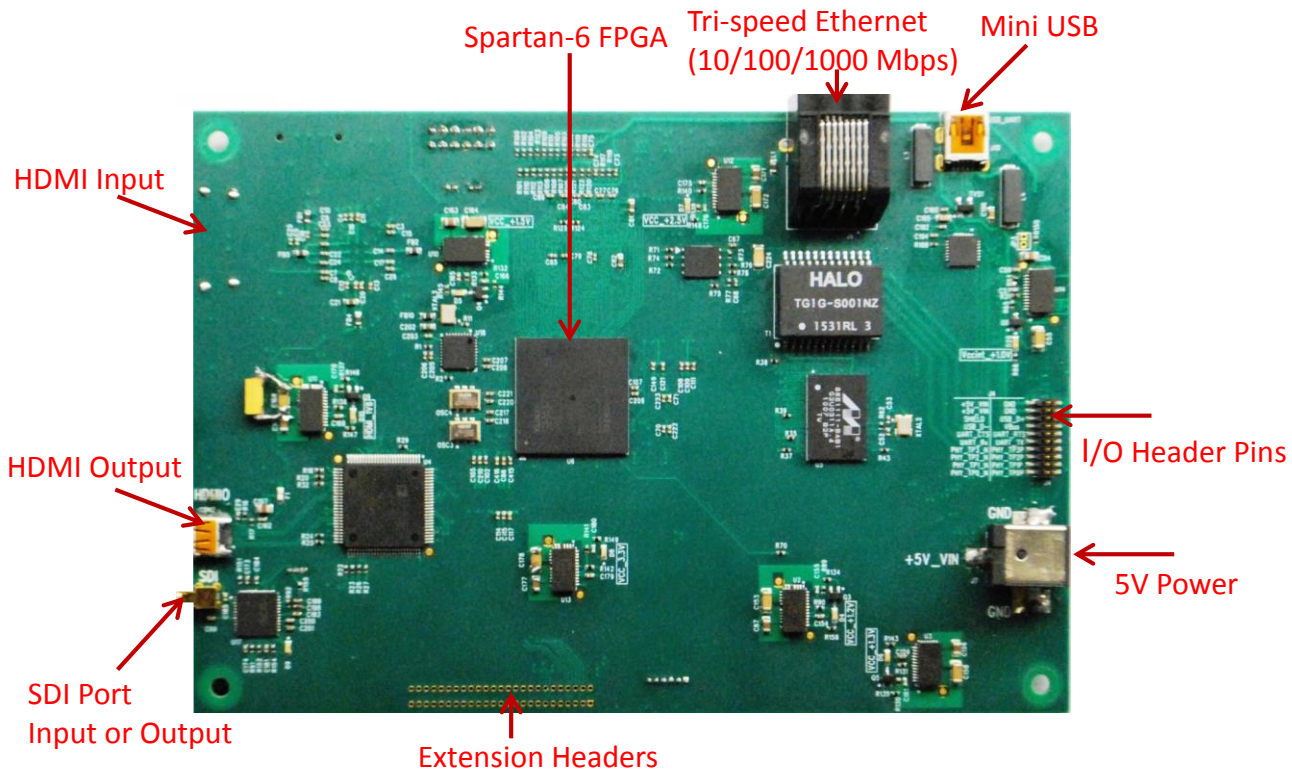

Fig. 11. FMC-MCM-1000 evaluation board

13. Ordering Information

Fig. 13 shows the product code naming convention for the SOC MPEG codec modules and IP cores. Non-standard codec modules can be ordered following the same naming format (minimum order quantity is required for non-standard modules).

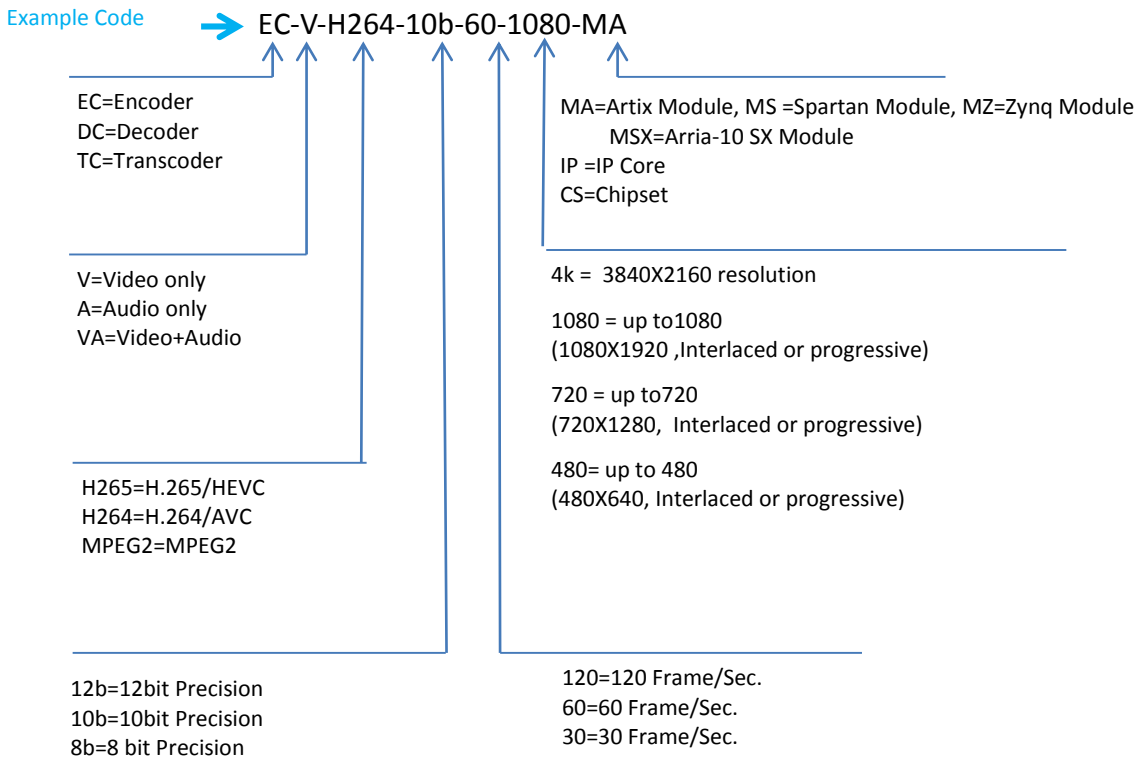

Fig. 13 SOC MPEG codec (IP cores and modules) product code naming convention

14. Contact Information

Please contact SOC head office or distributor for product details and to place an order.

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15. Document Revisions

Version #	Revision Date	Notes
V.1.0	10/05/2017	First release
V.1.1	19/05/2017	Minor revision
V.2.0	20/05/2017	Major revision (adding 4k)
V.2.1	05/06/2017	Minor revision

Appendix-A Factory Standard Codec Modules

A.1 H.265 Encoder Modules

The H.265 encoder modules are based on either the MCM-1000SX or MCM-1000Z hardware. The SOC H.265 encoder IP cores of different configurations are used to configure the FPGAs on the hardware modules to produce the codec modules.

Table-A1 lists the product codes of the factory standard H.265 video encoder (video only) modules, along with the specifications for each module. Table-A2 lists the video/audio encoder modules. The hardware platform, MCM-1000SX or MCM-1000Z, is used for the H.265 video encoder. Customers can order the H.265 encoder modules using the product code, according to the specifications required by the application.

Table-A1: H.265 Video Encoder Modules (video only without audio):

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-V-H265-8b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H265-10b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H265-10b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 30fps	no
EC-V-H265-8b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H265-10b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
EC-V-H265-10b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 60fps	no
EC-V-H265-8b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	no
EC-V-H265-10b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	no
EC-V-H265-10b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12 bits	up to 30fps	no
EC-V-H265-8b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	no
EC-V-H265-10b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 60fps	no
EC-V-H265-10b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12bits	up to 60fps	no

Table-A2: H.265 Video&Audio Encoder Modules (both video and audio)**:**

Product #	Specifications						
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio
EC-VA-H265-8b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-1080-M	H.265	Main 4:2:2 12	up to 1080i/p	4:2:0/4:2:2	up to 12 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-30-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12 bits	up to 30fps	AAC or MPEG2 Layer-2
EC-VA-H265-8b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	8 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-10b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC or MPEG2 Layer-2
EC-VA-H265-12b-60-4k-M	H.265	Main 4:2:2 12	4k/UHD	4:2:0/4:2:2	up to 12bits	up to 60fps	AAC or MPEG2 Layer-2

A.2 H.264 Encoder Modules

The H.264 encoder modules are based on either the on the MCM-1000A hardware. The SOC H.264 encoder IP cores are used to configure the FPGAs on the hardware modules to produce the codec modules.

Table-A3 lists the product code of the factory standard video encoder modules (video only), along with the specifications for each module. Table-A4 lists the video/audio encoder modules (both video and audio). Customers can order the encoder modules using the product code, according to the specifications required by the application.

Table-A3: H.264 Video Encoder Modules (video only without audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-H264-8b-30-720-MS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-H264-8b-60-720-MS	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-H264-8b-30-1080-MS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-H264-10b-30-1080-MS	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	MCM-1000A
EC-V-H264-8b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-H264-10b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	MCM-1000A
EC-V-H264-8b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 8 bits	up to 30fps	no	MCM-1000Z
EC-V-H264-10b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 10 bits	up to 30fps	no	MCM-1000Z
EC-V-H264-8b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 8 bits	up to 60fps	no	MCM-1000Z
EC-V-H264-10b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	up to 10 bits	up to 60fps	no	MCM-1000Z

Table-A6: H.264 Video&Audio Decoder Modules (both video and audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
DC-VA-H264-8b-30-720-MA	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-60-720-MA	H.264	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-30-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-10b-30-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-10b-60-1080-MA	H.264	up to High	up to 1080i/p	4:2:0/4:2:2	up to 10 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
DC-VA-H264-8b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-10b-30-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	10 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-8b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000Z
DC-VA-H264-10b-60-4k-MZ	H.264	High	4kx2k	4:2:0/4:2:2	10 bits	up to 60fps	AAC/MPEG2 L-2 L	MCM-1000Z

A.4 MPEG-2 Encoder Modules

Table-A7 lists the standard MPEG-2 video encoder modules. Table-A8 lists the MPEG-2 video/audio encoder modules. The 8 -bit precision and 60 frames/second modules are offered as extensions of the MPEG-2 standard.

Table-A7: MPEG-2 Video Encoder Module (video only without audio):

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-V-MPEG2-8b-30-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A
EC-V-MPEG2-8b-30-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	no	MCM-1000A
EC-V-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	no	MCM-1000A

Table-A8: MPEG-2 Video&Audio Encoder Modules (both video and audio)**:**

Product #	Specifications							Hardware
	Standard	Profile	Resolution	Chroma	Precision	Frame Rate	Audio	
EC-VA-MPEG2-8b-30-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-60-720-MA	MPEG-2	up to High	up to 720i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-30-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 30fps	AAC/MPEG2 L-2	MCM-1000A
EC-VA-MPEG2-8b-60-1080-MA	MPEG-2	up to High	up to 1080i/p	4:2:0/4:2:2	8 bits	up to 60fps	AAC/MPEG2 L-2	MCM-1000A

Appendix - B MCM-1000A Edge Connector Schematics