Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12hy32j0clh

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12HY/HA-Family devices

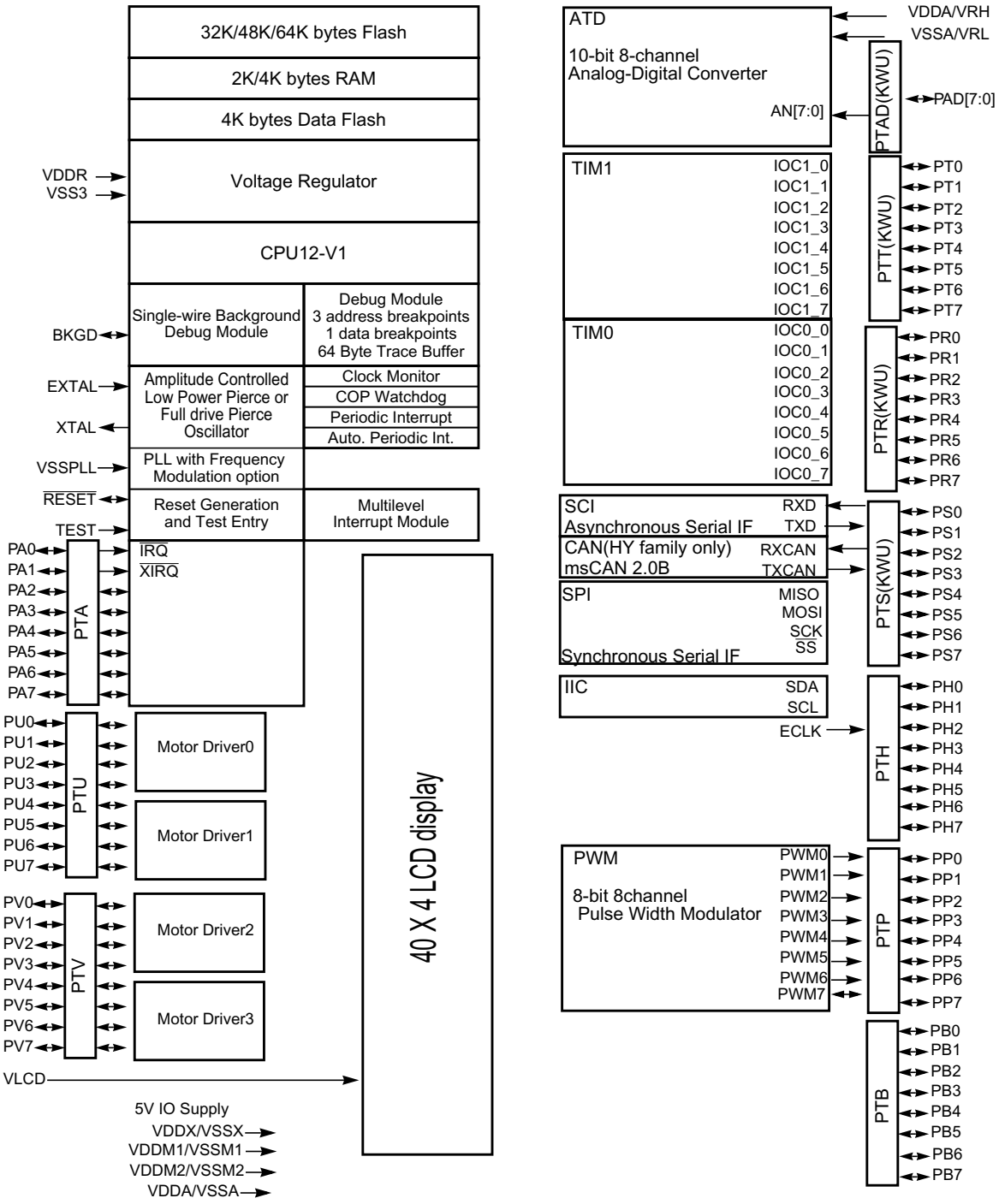

Figure 1-1. MC9S12HY/HA-Family 100 LQFP Block Diagram

Consult the ATD section for information about the analog-to-digital converter module. References to freeze mode are equivalent to active BDM mode.

1.14 S12CPMU Configuration

The bandgap reference voltage V_{BG} and the output voltage of the temperature sensor V_{HT} can be connected to the ATD channel SPECIAL17 (see Table 8-15) using the VSEL (Voltage Access Select Bit) in CPMUHTCTL register (see Table 7-13)

1.15 Documentation Note

The terms S12P, S12X and S12S which appear in some of the following chapters refer to the original architecture which those modules were designed to work with. Please do not confuse them with the S12HY/S12HA product families.

S12HY/S12HA will support only 10-bit ATD resolution, although in ATD12B8C block it still has the 12-bit descriptions.

If the interrupt source is unknown (for example, in the case where an interrupt request becomes inactive after the interrupt has been recognized, but prior to the CPU vector request), the vector address supplied to the CPU will default to that of the spurious interrupt vector.

NOTE

Care must be taken to ensure that all interrupt requests remain active until the system begins execution of the applicable service routine; otherwise, the exception request may not get processed at all or the result may be a spurious interrupt request (vector at address (vector base + 0x0080)).

4.4.3 Reset Exception Requests

The INT module supports three system reset exception request types (please refer to the Clock and Reset generator module for details):

1. Pin reset, power-on reset or illegal address reset, low voltage reset (if applicable)
2. Clock monitor reset request
3. COP watchdog reset request

4.4.4 Exception Priority

The priority (from highest to lowest) and address of all exception vectors issued by the INT module upon request by the CPU is shown in Table 4-4.

Table 4-4. Exception Vector Map and Priority

Vector Address[1]	Source
0xFFFE	Pin reset, power-on reset, illegal address reset, low voltage reset (if applicable)
0xFFFC	Clock monitor reset
0xFFFA	COP watchdog reset
(Vector base + 0x00F8)	Unimplemented opcode trap
(Vector base + 0x00F6)	Software interrupt instruction (SWI) or BDM vector request
(Vector base + 0x00F4)	X bit maskable interrupt request (XIRQ or D2D error interrupt)[2]
(Vector base + 0x00F2)	IRQ or D2D interrupt request[3]
(Vector base + 0x00F0–0x0082)	Device specific I bit maskable interrupt sources (priority determined by the low byte of the vector address, in descending order)
(Vector base + 0x0080)	Spurious interrupt

1 16 bits vector address based

2 D2D error interrupt on MCUs featuring a D2D initiator module, otherwise $\overline{\text{XIRQ}}$ pin interrupt

3 D2D interrupt on MCUs featuring a D2D initiator module, otherwise $\overline{\text{IRQ}}$ pin interrupt

6.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-10. Debug State Control Register 2 (DBGSCR2)

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 6-1 and described in 6.3.2.8.1, "Debug Comparator Control Register (DBGXCTL)". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-17. DBGSCR2 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 6-18. State2 —Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1..... Match2 to State3.
0001	Match1 to State3
0010	Match2 to State3
0011	Match1 to State3..... Match0 Final State
0100	Match1 to State1..... Match2 to State3.
0101	Match2 to Final State
0110	Match2 to State1..... Match0 to Final State
0111	Either Match0 or Match1 to Final State
1000	Reserved
1001	Reserved
1010	Reserved
1011	Reserved
1100	Either Match0 or Match1 to Final State.....Match2 to State3
1101	Reserved
1110	Reserved
1111	Either Match0 or Match1 to Final State.....Match2 to State1

The priorities described in Table 6-36 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2).

Chapter 8
Analog-to-Digital Converter (ADC12B8CV1) Block Description

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	25 July 2007	25 July 2007		Initial version
V01.01	14 Sept 2007	14 Sept 2007		Added reserved registers at the end the memory map.
V01.02	1 Oct 2007	1 Oct 2007		Added following mention where applies: ***(n conversion number, NOT channel number!)***
V01.03	9 Oct 2007	9 Oct 2007		Modified table “Analog Input Channel Select Coding” due to new customer feature (SPECIAL17).
V01.04	30 Apr 2008	30 Apr 2008		Updated document for 8 channels.

8.1 Introduction

The ADC12B8C is a 8-channel, 12-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

8.1.1 Features

- 8-, 10-, or 12-bit resolution.
- Conversion in Stop Mode using internally generated clock
- Automatic return to low power after conversion sequence
- Automatic compare with interrupt for higher than or less/equal than programmable value
- Programmable sample time.
- Left/right justified result data.
- External trigger control.
- Sequence complete interrupt.
- Analog input multiplexer for 8 analog input channels.
- Special conversions for V_{RH}, V_{RL}, $(V_{RL}+V_{RH})/2$.
- 1-to-8 conversion sequence lengths.

Write: Anytime (any value written causes PWM counter to be reset to $00).

11.3.2.13 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

See Section 11.4.2.3, “PWM Period and Duty” for more information.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)
- PWMx Period = Channel Clock Period * PWMPERx Center Aligned Output (CAEx = 1)

  PWMx Period = Channel Clock Period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 11.4.2.8, “PWM Boundary Cases”.

Module Base + 0x0014 = PWMPER0, 0x0015 = PWMPER1, 0x0016 = PWMPER2, 0x0017 = PWMPER3
Module Base + 0x0018 = PWMPER4, 0x0019 = PWMPER5, 0x001A = PWMPER6, 0x001B = PWMPER7

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 11-15. PWM Channel Period Registers (PWMPERx)

Read: Anytime

Write: Anytime

12.3.2.1 SCI Baud Rate Registers (SCIBDH, SCIBDL)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
Reset	0	0	0	0	0	0	0	0

Figure 12-3. SCI Baud Rate Register (SCIBDH)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
Reset	0	0	0	0	0	1	0	0

Figure 12-4. SCI Baud Rate Register (SCIBDL)

Read: Anytime, if AMAP = 0. If only SCIBDH is written to, a read will not return the correct data until SCIBDL is written to as well, following a write to SCIBDH.

Write: Anytime, if AMAP = 0.

NOTE

Those two registers are only visible in the memory map if AMAP = 0 (reset condition).

The SCI baud rate register is used by to determine the baud rate of the SCI, and to control the infrared modulation/demodulation submodule.

Table 12-2. SCIBDH and SCIBDL Field Descriptions

Field	Description
7 IREN	**Infrared Enable Bit** — This bit enables/disables the infrared modulation/demodulation submodule. 0 IR disabled 1 IR enabled
6:5 TNP[1:0]	**Transmitter Narrow Pulse Bits** — These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse. See Table 12-3.
4:0 7:0 SBR[12:0]	**SCI Baud Rate Bits** — The baud rate for the SCI is determined by the bits in this register. The baud rate is calculated two different ways depending on the state of the IREN bit. The formulas for calculating the baud rate are: When IREN = 0 then, SCI baud rate = SCI bus clock / (16 x SBR[12:0]) When IREN = 1 then, SCI baud rate = SCI bus clock / (32 x SBR[12:1]) **Note:** The baud rate generator is disabled after reset and not started until the TE bit or the RE bit is set for the first time. The baud rate generator is disabled when (SBR[12:0] = 0 and IREN = 0) or (SBR[12:1] = 0 and IREN = 1). **Note:** Writing to SCIBDH has no effect without writing to SCIBDL, because writing to SCIBDH puts the data in a temporary location until SCIBDL is written to.

Offset Module Base + 0x000E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-20. Flash Reserved3 Register (FRSV3)

All bits in the FRSV3 register read 0 and are not writable.

15.3.2.15 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Offset Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-21. Flash Reserved4 Register (FRSV4)

All bits in the FRSV4 register read 0 and are not writable.

15.3.2.16 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Offset Module Base + 0x0010

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 15-22. Flash Option Register (FOPT)

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 15-3) as indicated by reset condition F in Figure 15-22. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 15-50. Unsecure Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 15-27)
	FPVIOL	Set if any area of the P-Flash or D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[1]

1 As found in the memory map for FTMRC64K1.

15.4.5.11 Verify Backdoor Access Key Command

The Verify Backdoor Access Key command will only execute if it is enabled by the KEYEN bits in the FSEC register (see Table 15-9). The Verify Backdoor Access Key command releases security if user-supplied keys match those stored in the Flash security bytes of the Flash configuration field (see Table 15-3). The Verify Backdoor Access Key command must not be executed from the Flash block containing the backdoor comparison key to avoid code runaway.

Table 15-51. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

16.1.2.2 D-Flash Features

- 4 Kbytes of D-Flash memory composed of one 4 Kbyte Flash block divided into 16 sectors of 256 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of D-Flash memory
- Ability to program up to four words in a burst sequence

16.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

16.1.3 Block Diagram

The block diagram of the Flash module is shown in Figure 16-1.

Table 16-4. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2	Version ID[1]
0x0_40B8 – 0x0_40BF	8	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 16.4.5.6, “Program Once Command”

1 Used to track firmware patch versions, see Section 16.4.2

Table 16-5. D-Flash and Memory Controller Resource Fields

Global Address	Size (Bytes)	Description
0x0_4000 – 0x0_43FF	1,024	Reserved
0x0_4400 – 0x0_53FF	4,096	D-Flash Memory
0x0_5400 – 0x0_57FF	1,024	Reserved
0x0_5800 – 0x0_5AFF	768	Memory Controller Scratch RAM (RAMON[1] = 1)
0x0_5B00 – 0x0_5FFF	1,280	Reserved
0x0_6000 – 0x0_67FF	2,048	Reserved
0x0_6800 – 0x0_7FFF	6,144	Reserved

1 MMCCTL1 register bit

Table 16-14. FSTAT Field Descriptions (continued)

Field	Description
3 MGBUSY	**Memory Controller Busy Flag** — The MGBUSY flag reflects the active state of the Memory Controller. 0 Memory Controller is idle 1 Memory Controller is busy executing a Flash command (CCIF = 0)
2 RSVD	**Reserved Bit** — This bit is reserved and always reads 0.
1–0 MGSTAT[1:0]	**Memory Controller Command Completion Status Flag** — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. See Section 16.4.5, “Flash Command Description,” and Section 16.6, “Initialization” for details.

16.3.2.8 Flash Error Status Register (FERSTAT)

The FERSTAT register reflects the error status of internal Flash operations.

Offset Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIF	SFDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-12. Flash Error Status Register (FERSTAT)

All flags in the FERSTAT register are readable and only writable to clear the flag.

Table 16-15. FERSTAT Field Descriptions

Field	Description
1 DFDIF	**Double Bit Fault Detect Interrupt Flag** — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation.[1] The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF. 0 No double bit fault detected 1 Double bit fault detected or an invalid Flash array read operation attempted
0 SFDIF	**Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation.[1] The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or an invalid Flash array read operation attempted

[1] The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault but never both). A simultaneous access collision (read attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

16.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Figure 19-2. MC10B8C Memory Map (continued)

Offset	Register	Access
0x0016	Motor Controller Channel Control Register 6 (MCCC6)	RW
0x0017	Motor Controller Channel Control Register 7 (MCCC7)	RW
0x0018	Reserved	—
0x0019	Reserved	—
0x001A	Reserved	—
0x001B	Reserved	—
0x001C	Reserved	—
0x001D	Reserved	—
0x001E	Reserved	—
0x001F	Reserved	—
0x0020	Motor Controller Duty Cycle Register 0 (MCDC0) — High Byte	RW
0x0021	Motor Controller Duty Cycle Register 0 (MCDC0) — Low Byte	RW
0x0022	Motor Controller Duty Cycle Register 1 (MCDC1) — High Byte	RW
0x0023	Motor Controller Duty Cycle Register 1 (MCDC1) — Low Byte	RW
0x0024	Motor Controller Duty Cycle Register 2 (MCDC2) — High Byte	RW
0x0025	Motor Controller Duty Cycle Register 2 (MCDC2) — Low Byte	RW
0x0026	Motor Controller Duty Cycle Register 3 (MCDC3) — High Byte	RW
0x0027	Motor Controller Duty Cycle Register 3 (MCDC3) — Low Byte	RW
0x0028	Motor Controller Duty Cycle Register 4 (MCDC4) — High Byte	RW
0x0029	Motor Controller Duty Cycle Register 4 (MCDC4) — Low Byte	RW
0x002A	Motor Controller Duty Cycle Register 5 (MCDC5) — High Byte	RW
0x002B	Motor Controller Duty Cycle Register 5 (MCDC5) — Low Byte	RW
0x002C	Motor Controller Duty Cycle Register 6 (MCDC6) — High Byte	RW
0x002D	Motor Controller Duty Cycle Register 6 (MCDC6) — Low Byte	RW
0x002E	Motor Controller Duty Cycle Register 7 (MCDC7) — High Byte	RW
0x002F	Motor Controller Duty Cycle Register 7 (MCDC7) — Low Byte	RW
0x0030	Reserved	—
0x0031	Reserved	—
0x0032	Reserved	—
0x0033	Reserved	—
0x0034	Reserved	—
0x0035	Reserved	—
0x0036	Reserved	—
0x0037	Reserved	—
0x0038	Reserved	—
0x0039	Reserved	—
0x003A	Reserved	—
0x003B	Reserved	—
0x003C	Reserved	—
0x003D	Reserved	—

VDDR supplies the internal voltage regulator.

All VDDM pins are internally connected by metal.

All VSSM pins are internally connected by metal.

VDDA, VDDX, VDDM and VSSA, VSSX, VSSM are connected by diodes for ESD protection.

NOTE

In the following context V_{DD35} is used for either VDDA, VDDR, VDDM and VDDX; V_{SS35} is used for either VSSA, VSSM and VSSX unless otherwise noted.

I_{DD35} denotes the sum of the currents flowing into the VDDAand VDDR pins. The run mode current in VDDM and VDDX is external load dependent

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 I/O Pins

The I/O pins have a level in the range of 4.5V to 5.5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the $\overline{\text{RESET}}$ pins. Some functionality may be disabled.

A.1.3.2 Analog Reference

This group is made up by the VDDA and VSSA pins.

A.1.3.3 Oscillator

The pins EXTAL, XTAL dedicated to the oscillator have a nominal 1.8V level.

A.1.3.4 TEST

This pin is used for production testing only. The TEST pin must be tied to ground in all applications.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD35} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD35}$) is greater than I_{DD35}, the injection current may flow out of V_{DD35} and could result in external power supply going out of regulation. Ensure external V_{DD35} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g., if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

Table A-6. 5-V I/O Characteristics

18	D	Port T, S, R, AD interrupt input pulse passed ($\overline{STOP}$)	t_{PULSE}	4	—	—	tcyc
19	D	$\overline{IRQ}$ pulse width, edge-sensitive mode ($\overline{STOP}$)	PW_{IRQ}	1	—	—	tcyc

1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12°C in the temperature range from 50°C to 125°C.
2. Refer to Section A.1.4, “Current Injection” for more details
3. Parameter only applies in stop or pseudo stop mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

IDD value is measured on VDDR pin. It does not include the current to drive external loads. Unless otherwise noted the currents are measured in special single chip mode and the CPU code is executed from RAM. For Run and Wait current measurements PLL is on and the reference clock is the IRC trimmed to 1 MHz. The bus frequency is 32 MHz and the CPU frequency is 64 MHz. Table A-7, Table A-8 and Table A-9 show the configuration of the CPMU module and the peripherals for Run, Wait and Stop current measurement.

Table A-7. CPMU Configuration for Pseudo Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUCLKS	PLLSEL=0, PSTP=1, PRE=PCE=RTIOSCSEL=COPOSCSEL=1
CPMUOSC	OSCE=1, External Square wave on EXTAL f_{EXTAL}=16MHz, V_{IH}= 1.8V, V_{IL}=0V
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111;
CPMUCOP	WCOP=1, CR[2:0]=111

Table A-8. CPUM Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]=01,SYNDIV[5:0] = 32
CPMUPOSTDIV	POSTDIV[4:0]=0,
CPMUCLKS	PLLSEL=1
CPMUOSC	OSCE=0, Reference clock for PLL is f_{ref}=f_{irc1m} trimmed to 1MHz

A.2 ATD Characteristics

This section describes the characteristics of the analog-to-digital converter.

A.2.1 ATD Operating Characteristics

The Table A-12 and Table A-13 show conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

V_{SSA} (V_{RL})≤ V_{IN} ≤ V_{DDA}(V_{RH}).

This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-12. ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted, supply voltage 3.13 V < V_{DDA} < 5.5 V							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Voltage difference V_{DDX}/$V_{DDM}$to V_{DDA}	Δ_{VDDX}	–0.1	0	0.1	V
2	D	Voltage difference V_{SSX}/V_{SSM} to V_{SSA}	Δ_{VSSX}	–0.1	0	0.1	V
3	C	Differential reference voltage[1]	V_{RH}-V_{RL}	3.13	5.0	5.5	V
4	C	ATD Clock Frequency (derived from bus clock via the prescaler bus)	f_{ATDCLk}	0.25		8.0	MHz
5	P	ATD Clock Frequency in Stop mode (internal generated temperature and voltage dependent clock, ICLK)		0.6	1	1.7	MHz
6	D	ADC conversion in stop, recovery time[2]	$t_{ATDSTPRCV}$	—	—	1.5	us
7	D	ATD Conversion Period[3] 10 bit resolution: 8 bit resolution:	N_{CONV10} N_{CONV8}	19 17		41 39	ATD clock Cycles

1. Full accuracy is not guaranteed when differential voltage is less than 4.50 V
2. When converting in Stop Mode (ICLKSTP=1) an ATD Stop Recovery time tATDSTPRCV is required to switch back to bus clock based ATDCLK when leaving Stop Mode. Do not access ATD registers during this time.
3. The minimum time assumes a sample time of 4 ATD clock cycles. The maximum time assumes a sample time of 24 ATD clock cycles and the discharge feature (SMP_DIS) enabled, which adds 2 ATD clock cycles.

A.2.2 Factors Influencing Accuracy

Source resistance, source capacitance and current injection have an influence on the accuracy of the ATD. A further factor is that PortAD pins that are configured as output drivers switching.

A.2.2.1 Port AD Output Drivers Switching

PortAD output drivers switching can adversely affect the ATD accuracy whilst converting the analog voltage on other PortAD pins because the output drivers are supplied from the VDDA/VSSA ATD supply pins. Although internal design measures are implemented to minimize the affect of output driver noise, it

A.3.1.8 Erase P-Flash Block (FCMD=0x09)

The time required to erase the P-Flash block is given by:

for 64 KB P-Flash

$$t_{pmass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 35000 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.9 Erase P-Flash Sector (FCMD=0x0A)

The typical time to erase a 512-byte P-Flash sector is given by:

$$t_{pera} \approx 20020 \cdot \frac{1}{f_{NVMOP}} + 700 \cdot \frac{1}{f_{NVMBUS}}$$

The maximum time to erase a 512-byte P-Flash sector is given by:

$$t_{pera} \approx 20020 \cdot \frac{1}{f_{NVMOP}} + 1400 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.10 Unsecure Flash (FCMD=0x0B)

The maximum time required to erase and unsecure the Flash is given by:

for 64 KB P-Flash and 4 KB D-Flash

$$t_{uns} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 38000 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.11 Verify Backdoor Access Key (FCMD=0x0C)

The maximum verify backdoor access key time is given by:

$$t = 400 \cdot \frac{1}{f_{NVMBUS}}$$

A.3.1.12 Set User Margin Level (FCMD=0x0D)

The maximum set user margin level time is given by:

$$t = 350 \cdot \frac{1}{f_{NVMBUS}}$$

A.4 Reset, Oscillator,IRC,IVREG,IPLL

A.5 Phase Locked Loop

A.5.1 Jitter Definitions

With each transition of the feedback clock, the deviation from the reference clock is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the VCOCLK frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in Figure A-2.

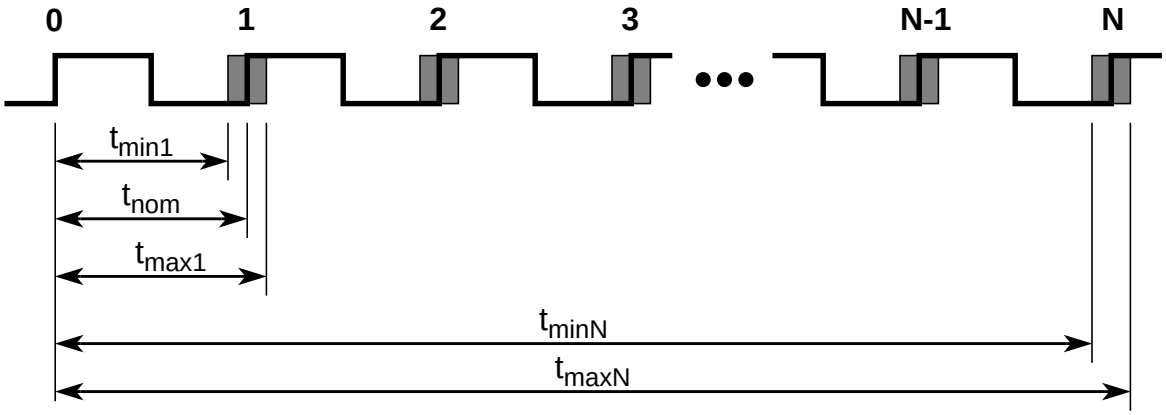

Figure A-2. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}}$$

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x010A	FCCOBHI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x010B	FCCOBLO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x010C-0x010F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0110	FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
		W								
0x0111-0x0113	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0114–0x011F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0114-0x011F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0120 Interrupt Module(INT) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0120	IVBR	R	IVB_ADDR[7:0]							
		W								

0x0121-0x013F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0121-0x013F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x140-0x017F MSCAN(CAN) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0140	CANCTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x0141	CANCTL1	R	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		W								
0x0142	CANBTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x0143	CANBTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x0144	CANRFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								