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Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SCI, SPI
Peripherals	LCD, Motor control PWM, POR, PWM, WDT
Number of I/O	80
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12hy64j0cll

1.7.3.41 PU[0] / IOC0_0 / M0C0M— Port U I/O Pin [0]

PU[0] is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor drive. The pin interfaces to the coils of motor 0. It can aslo be configured as timer(TIM0) channel 0

1.7.3.42 PV[7] / M3C1P— Port V I/O Pin [7]

PV[7] is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor drive. The pin interfaces to the coils of motor 3.

1.7.3.43 PV[6] / IOC1_3 / M3C1M— Port V I/O Pin [6]

PV[6] is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor drive. The pin interfaces to the coils of motor 3. It can aslo be configured as timer (TIM1) channel 3

1.7.3.44 PV[5] / M3C0P— Port V I/O Pin [5]

PV[5] is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor drive. The pin interfaces to the coils of motor 3.

1.7.3.45 PV[4] / IOC1_2 / M3C0M— Port V I/O Pin [4]

PV[4] is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor drive. The pin interfaces to the coils of motor 3. It can aslo be configured as timer (TIM1) channel 2

1.7.3.46 PV3 / $\overline{SS}$ / PWM7 / SDA / M2C1P — Port V I/O Pin 3

PV3 is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor driver. It interface to the coil of motor 2. It can be configured as the slave selection pin $\overline{SS}$ for the serial peripheral interface (SPI). It can be configured as the serial data pin SDA as IIC module. It can be configured as PWM channel 7.

1.7.3.47 PV2 / PWM6 / SCK / IOC1_1 / M2C1M— Port V I/O Pin 2

PV2 is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor driver. It interface to the coil of motor 2. It can be configured as timer(TIM1) channel 1. It can be configured as the serial clock SCK of the serial peripheral interface (SPI). It can be configured as PWM channel 6.

1.7.3.48 PV1 / PWM5 / MOSI / M2C0P — Port V I/O Pin 1

PV1 is a general-purpose input or output pin. It can be configured as high current PWM output pin which can be used for motor driver. It interface to the coil of motor 2. It can be configured as the master output

Table 2-2. Block Memory Map (continued)

Port	Offset or Address	Register	Access	Reset Value	Section/Page
S	0x0248	PTS—Port S Data Register	R/W	0x00	2.3.22/2-84
	0x0249	PTIS—Port S Input Register	R	[3]	2.3.23/2-86
	0x024A	DDRS—Port S Data Direction Register	R/W	0x00	2.3.24/2-87
	0x024B	RDRS—Port S Reduced Drive Register	R/W	0x00	2.3.25/2-88
	0x024C	PERS—Port S Pull Device Enable Register	R/W	0xFF	2.3.26/2-89
	0x024D	PPSS—Port S Polarity Select Register	R/W	0x00	2.3.27/2-89
	0x024E	WOMS—Port S Wired-Or Mode Register	R/W	0x00	2.3.28/2-90
	0x024F	PTSRR Port S Routing Register	R/W	0x00	2.3.29/2-90
	0x0250 : 0x0257	PIM Reserved	R	0x00	2.3.30/2-91
P	0x0258	PTP—Port P Data Register	R/W	0x00	2.3.31/2-91
	0x0259	PTIP—Port P Input Register	R	[3]	2.3.32/2-92
	0x025A	DDRP—Port P Data Direction Register	R/W	0x00	2.3.33/2-92
	0x025B	RDRP—Port P Reduced Drive Register	R/W	0x00	2.3.34/2-93
	0x025C	PERP—Port P Pull Device Enable Register	R/W	0xFF	2.3.35/2-94
	0x025D	PPSP—Port P Polarity Select Register	R/W	0xFF	2.3.36/2-94
	0x025E	PTPRRH Port P Routing Register High	R/W	0x00	2.3.37/2-95
	0x025F	PTPRRL Port P Routing Register Low	R/W	0x00	2.3.38/2-95
H	0x0260	PTH—Port H Data Register	R/W	0x00	2.3.39/2-96
	0x0261	PTIH—Port H Input Register	R	[3]	2.3.40/2-98
	0x0262	DDRH—Port H Data Direction Register	R/W	0x00	2.3.41/2-98
	0x0263	RDRH—Port H Reduced Drive Register	R/W	0x00	2.3.42/2-100
	0x0264	PERH—Port H Pull Device Enable Register	R/W	0xFF	2.3.43/2-100
	0x0265	PPSH—Port H Polarity Select Register	R/W	0xFF	2.3.44/2-101
	0x0266	WOMH—Port H Wired-Or Mode Register	R/W	0x00	2.3.45/2-101
	0x0267	PIM Reserved	R	0x00	2.3.46/2-102
	0x0268 : 0x026F	PIM Reserved	R	0x00	2.3.47/2-102

Table 2-22. RDRS Register Field Descriptions

Field	Description
7-0 RDRS	**Port S reduced drive**—Select reduced drive for outputs This register configures the drive strength of output pins 7 through 0 as either full or reduced. If a pin is used as input this bit has no effect. 1 Reduced drive selected (1/6 of the full drive strength). 0 Full drive strength enabled.

2.3.26 Port S Pull Device Enable Register (PERS)

Address 0x024C Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
Reset	1	1	1	1	1	1	1	1

Figure 2-24. Port S Pull Device Enable Register (PERS)

1 Read: Anytime.
Write: Anytime.

Table 2-23. PERS Register Field Descriptions

Field	Description
7-0 PERS	**Port S pull device enable**—Enable pull devices on input pins These bits configure whether a pull device is activated, if the associated pin is used as an input. This bit has no effect if the pin is used as an output. Out of reset all pull devices are enabled. 1 Pull device enabled. 0 Pull device disabled.

2.3.27 Port S Polarity Select Register (PPSS)

Address 0x024D Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
Reset	0	0	0	0	0	0	0	0

Figure 2-25. Port S Polarity Select Register (PPSS)

1 Read: Anytime.
Write: Anytime.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x002E	DBGADHM	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x002F	DBGADLM	R W	Bit 7	6	5	4	3	2	1	Bit 0

1 This bit is visible at DBGCNT[7] and DBGSR[7]

2 This represents the contents if the Comparator A control register is blended into this address.

3 This represents the contents if the Comparator B control register is blended into this address

4 This represents the contents if the Comparator C control register is blended into this address

Figure 6-2. Quick Reference to DBG Registers

6.3.2 Register Descriptions

This section consists of the DBG control and trace buffer register descriptions in address order. Each comparator has a bank of registers that are visible through an 8-byte window between 0x0028 and 0x002F in the DBG module register address map. When ARM is set in DBGC1, the only bits in the DBG module registers that can be written are ARM, TRIG, and COMRV[1:0].

6.3.2.1 Debug Control Register 1 (DBGC1)

Address: 0x0020

	7	6	5	4	3	2	1	0
R	ARM	0	0	BDM	DBGBRK	0	COMRV	
W		TRIG						
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-3. Debug Control Register (DBGC1)

Read: Anytime

Write: Bits 7, 1, 0 anytime
Bit 6 can be written anytime but always reads back as 0.
Bits 4:3 anytime DBG is not armed.

NOTE

When disarming the DBG by clearing ARM with software, the contents of bits[4:3] are not affected by the write, since up until the write operation, ARM = 1 preventing these bits from being written. These bits must be cleared using a second write if required.

7.3.2.18 Reserved Register CPMUTEST3

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU's functionality.

0x02F6

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-23. Reserved Register (CPMUTEST3)

Read: Anytime

Write: Only in Special Mode

The RTI can be used to generate hardware interrupts at a fixed periodic rate. If enabled (by setting RTIE=1), this interrupt will occur at the rate selected by the CPMURTI register. At the end of the RTI time-out period the RTIF flag is set to one and a new RTI time-out period starts immediately.

A write to the CPMURTI register restarts the RTI time-out period.

7.6.1.2 PLL Lock Interrupt

The S12CPMU generates a PLL Lock interrupt when the lock condition (LOCK status bit) of the PLL changes, either from a locked state to an unlocked state or vice versa. Lock interrupts are locally disabled by setting the LOCKIE bit to zero. The PLL Lock interrupt flag (LOCKIF) is set to 1 when the lock condition has changed, and is cleared to 0 by writing a 1 to the LOCKIF bit.

7.6.1.3 Oscillator Status Interrupt

The Adaptive Oscillator Filter contains two different features:

1. Filter spikes of the external oscillator clock.

2. Qualify the external oscillator clock (detect and flag severe noise disturbances on the external oscillator clock which can not be filtered).

When the OSCE bit is 0, then UPOSC stays 0. When OSCE = 1 and OSCFILT = 0, then the filter is transparent and no spikes are filtered. The UPOSC bit is then set after the LOCK bit is set.

Upon detection of a status change (UPOSC), that is an unqualified oscillation becomes qualified or vice versa, the OSCIF flag is set. Going into Full Stop Mode or disabling the oscillator can also cause a status change of UPOSC.

Also, since the Adaptive Oscillator Filter is based on the PLLCLK, any change in PLL configuration or any other event which causes the PLL lock status to be cleared leads to a loss of the oscillator status information as well (UPOSC=0).

Oscillator status change interrupts are locally enabled with the OSCIE bit.

NOTE

Loosing the oscillator status (UPOSC=0) affects the clock configuration of the system[1]. This needs to be dealt with in application software.

7.6.1.4 Low-Voltage Interrupt (LVI)

In FPM the input voltage VDDA is monitored. Whenever VDDA drops below level $V_{LVIA,}$ the status bit LVDS is set to 1. When VDDA rises above level V_{LVID} the status bit LVDS is cleared to 0. An interrupt, indicated by flag LVIF = 1, is triggered by any change of the status bit LVDS if interrupt enable bit LVIE = 1.

1. For details please refer to “7.4.6 System Clock Configurations”

be edge or level sensitive with polarity control. Table 8-22 gives a brief description of the different combinations of control bits and their effect on the external trigger function.

Table 8-22. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Falling edge triggered. Performs one conversion sequence per trigger.
0	1	1	X	Rising edge triggered. Performs one conversion sequence per trigger.
1	0	1	X	Trigger active low. Performs continuous conversions while trigger is active.
1	1	1	X	Trigger active high. Performs continuous conversions while trigger is active.

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

In either level or edge triggered modes, the first conversion begins when the trigger is received.

Once ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger is left asserted in level mode while a sequence is completing, another sequence will be triggered immediately.

8.4.2.2 General-Purpose Digital Port Operation

The input channel pins can be multiplexed between analog and digital data. As analog inputs, they are multiplexed and sampled as analog channels to the A/D converter. The analog/digital multiplex operation is performed in the input pads. The input pad is always connected to the analog input channels of the ADC12B8C. The input pad signal is buffered to the digital port registers. This buffer can be turned on or off with the ATDDIEN register. This is important so that the buffer does not draw excess current when analog potentials are presented at its input.

8.5 Resets

At reset the ADC12B8C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see Section 8.3.2, “Register Descriptions”) which details the registers and their bit-field.

- The transmission buffer with the lowest local priority field wins the prioritization.

In cases of more than one buffer having the same lowest priority, the message buffer with the lower index number wins.

Module Base + 0x00XD — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R W	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
Reset:	0	0	0	0	0	0	0	0

Figure 9-36. Transmit Buffer Priority Register (TBPR)

1. Read: Anytime when TXEx flag is set (see Section 9.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 9.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)")
   Write: Anytime when TXEx flag is set (see Section 9.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 9.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)")

9.3.3.5 Time Stamp Register (TSRH–TSRL)

If the TIME bit is enabled, the MSCAN will write a time stamp to the respective registers in the active transmit or receive buffer right after the EOF of a valid message on the CAN bus (see Section 9.3.2.1, "MSCAN Control Register 0 (CANCTL0)"). In case of a transmission, the CPU can only read the time stamp after the respective transmit buffer has been flagged empty.

The timer value, which is used for stamping, is taken from a free running internal CAN bit clock. A timer overrun is not indicated by the MSCAN. The timer is reset (all bits set to 0) during initialization mode. The CPU can only read the time stamp registers.

Module Base + 0x00XE — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
W								
Reset:	x	x	x	x	x	x	x	x

Figure 9-37. Time Stamp Register — High Byte (TSRH)

1. Read: Anytime when TXEx flag is set (see Section 9.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 9.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)")
   Write: Unimplemented

9.4.3.1 Protocol Violation Protection

The MSCAN protects the user from accidentally violating the CAN protocol through programming errors. The protection logic implements the following features:

- The receive and transmit error counters cannot be written or otherwise manipulated.
- All registers which control the configuration of the MSCAN cannot be modified while the MSCAN is on-line. The MSCAN has to be in Initialization Mode. The corresponding INITRQ/INITAK handshake bits in the CANCTL0/CANCTL1 registers (see Section 9.3.2.1, "MSCAN Control Register 0 (CANCTL0)") serve as a lock to protect the following registers:
  - MSCAN control 1 register (CANCTL1)
  - MSCAN bus timing registers 0 and 1 (CANBTR0, CANBTR1)
  - MSCAN identifier acceptance control register (CANIDAC)
  - MSCAN identifier acceptance registers (CANIDAR0–CANIDAR7)
  - MSCAN identifier mask registers (CANIDMR0–CANIDMR7)
- The TXCAN is immediately forced to a recessive state when the MSCAN goes into the power down mode or initialization mode (see Section 9.4.5.6, "MSCAN Power Down Mode," and Section 9.4.4.5, "MSCAN Initialization Mode").
- The MSCAN enable bit (CANE) is writable only once in normal system operation modes, which provides further protection against inadvertently disabling the MSCAN.

9.4.3.2 Clock System

Figure 9-43 shows the structure of the MSCAN clock generation circuitry.

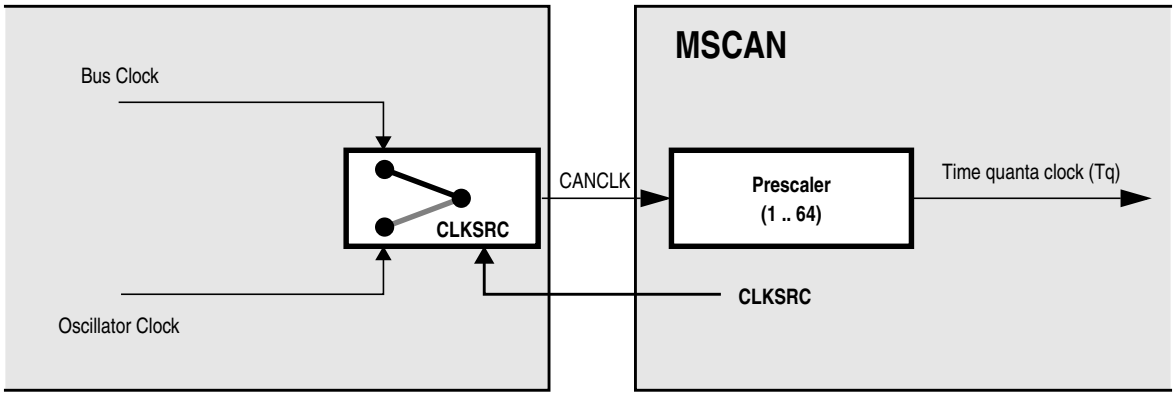

Figure 9-43. MSCAN Clocking Scheme

The clock source bit (CLKSRC) in the CANCTL1 register (9.3.2.2/9-319) defines whether the internal CANCLK is connected to the output of a crystal oscillator (oscillator clock) or to the bus clock.

The clock source has to be chosen such that the tight oscillator tolerance requirements (up to 0.4%) of the CAN protocol are met. Additionally, for high CAN bus rates (1 Mbps), a 45% to 55% duty cycle of the clock is required.

If the bus clock is generated from a PLL, it is recommended to select the oscillator clock rather than the bus clock due to jitter considerations, especially at the faster CAN bus rates.

For microcontrollers without a clock and reset generator (CRG), CANCLK is driven from the crystal oscillator (oscillator clock).

A programmable prescaler generates the time quanta (Tq) clock from CANCLK. A time quantum is the atomic unit of time handled by the MSCAN.

Eqn. 9-2

$$Tq = \frac{f_{CANCLK}}{(Prescaler\ value)}$$

A bit time is subdivided into three segments as described in the Bosch CAN specification. (see Figure 9-44):

- SYNC_SEG: This segment has a fixed length of one time quantum. Signal edges are expected to happen within this section.
- Time Segment 1: This segment includes the PROP_SEG and the PHASE_SEG1 of the CAN standard. It can be programmed by setting the parameter TSEG1 to consist of 4 to 16 time quanta.
- Time Segment 2: This segment represents the PHASE_SEG2 of the CAN standard. It can be programmed by setting the TSEG2 parameter to be 2 to 8 time quanta long.

Eqn. 9-3

$$Bit\ Rate = \frac{f_{Tq}}{(number\ of\ Time\ Quanta)}$$

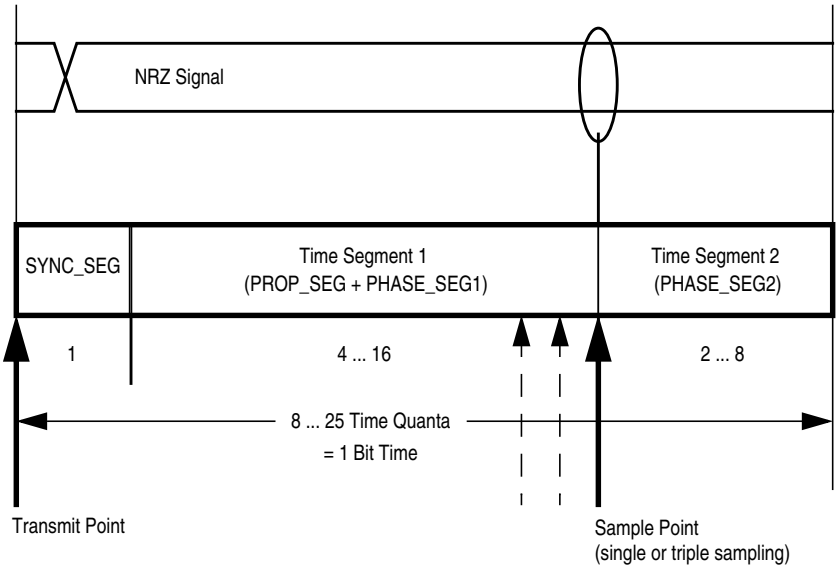

Figure 9-44. Segments within the Bit Time

IIC Interrupt	—	—	—	IBAL, TCF, IAAS bits in IBSR register	When either of IBAL, TCF or IAAS bits is set may cause an interrupt based on arbitration lost, transfer complete or address detect conditions

Internally there are three types of interrupts in IIC. The interrupt service routine can determine the interrupt type by reading the status register.

IIC Interrupt can be generated on

1. Arbitration lost condition (IBAL bit set)
2. Byte transfer condition (TCF bit set)
3. Address detect condition (IAAS bit set)

The IIC interrupt is enabled by the IBIE bit in the IIC control register. It must be cleared by writing 0 to the IBF bit in the interrupt service routine.

10.7 Application Information

10.7.1 IIC Programming Examples

10.7.1.1 Initialization Sequence

Reset will put the IIC bus control register to its default status. Before the interface can be used to transfer serial data, an initialization procedure must be carried out, as follows:

1. Update the frequency divider register (IBFD) and select the required division ratio to obtain SCL frequency from system clock.
2. Update the ADTYPE of IBCR2 to define the address length, 7 bits or 10 bits.
3. Update the IIC bus address register (IBAD) to define its slave address. If 10-bit address is applied IBCR2 should be updated to define the rest bits of address.
4. Set the IBEN bit of the IIC bus control register (IBCR) to enable the IIC interface system.
5. Modify the bits of the IIC bus control register (IBCR) to select master/slave mode, transmit/receive mode and interrupt enable or not.
6. If supported general call, the GCEN in IBCR2 should be asserted.

10.7.1.2 Generation of START

After completion of the initialization procedure, serial data can be transmitted by selecting the 'master transmitter' mode. If the device is connected to a multi-master bus system, the state of the IIC bus busy bit (IBB) must be tested to check whether the serial bus is free.

If the bus is free (IBB=0), the start condition and the first byte (the slave address) can be sent. The data written to the data register comprises the slave calling address and the LSB set to indicate the direction of transfer required from the slave.

The bus free time (i.e., the time between a STOP condition and the following START condition) is built into the hardware that generates the START cycle. Depending on the relative frequencies of the system

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the TXD pin to the receiver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).The TXDIR bit (SCISR2[1]) determines whether the TXD pin is going to be used as an input (TXDIR = 0) or an output (TXDIR = 1) in this mode of operation.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

12.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

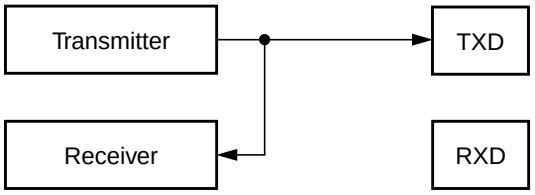

Figure 12-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

12.5 Initialization/Application Information

12.5.1 Reset Initialization

See Section 12.3.2, “Register Descriptions”.

12.5.2 Modes of Operation

12.5.2.1 Run Mode

Normal mode of operation.

To initialize a SCI transmission, see Section 12.4.5.2, “Character Transmission”.

Table 14-17. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 or PAEN bit of PACTL is set to one (See also TCRE control bit explanation.)

14.3.2.14 Timer Input Capture/Output Compare Registers High and Low 0–7 (TCxH and TCxL)

Module Base + 0x0010 = TC0H, 0x0012 = TC1H, 0x0014 = TC2H, 0x0016 = TC3H, 0x0018 = TC4H, 0x001A = TC5H, 0x001C = TC6H, 0x001E = TC7H

	15	14	13	12	11	10	9	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 14-22. Timer Input Capture/Output Compare Register x High (TCxH)

Module Base + 0x0011 = TC0L, 0x0013 = TC1L, 0x0015 = TC2L, 0x0017 = TC3L, 0x0019 = TC4L, 0x001B = TC5L, 0x001D = TC6L, 0x001F = TC7L

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 14-23. Timer Input Capture/Output Compare Register x Low (TCxL)

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should takes place before low byte otherwise it will give a different result.

15.4.3.3 Valid Flash Module Commands

Table 15-27. Flash Commands by Mode

FCMD	Command	Unsecured		Secured	
		NS[1]	SS[2]	NS[3]	SS[4]
0x01	Erase Verify All Blocks	*	*	*	*
0x02	Erase Verify Block	*	*	*	*
0x03	Erase Verify P-Flash Section	*	*	*	
0x04	Read Once	*	*	*	
0x06	Program P-Flash	*	*	*	
0x07	Program Once	*	*	*	
0x08	Erase All Blocks		*		*
0x09	Erase Flash Block	*	*	*	
0x0A	Erase P-Flash Sector	*	*	*	
0x0B	Unsecure Flash		*		*
0x0C	Verify Backdoor Access Key	*		*	
0x0D	Set User Margin Level	*	*	*	
0x0E	Set Field Margin Level		*		
0x10	Erase Verify D-Flash Section	*	*	*	
0x11	Program D-Flash	*	*	*	
0x12	Erase D-Flash Sector	*	*	*	

1 Unsecured Normal Single Chip mode.
2 Unsecured Special Single Chip mode.
3 Secured Normal Single Chip mode.
4 Secured Special Single Chip mode.

15.4.3.4 P-Flash Commands

Table 15-28 summarizes the valid P-Flash commands along with the effects of the commands on the P-Flash block and other resources within the Flash module.

Table 15-28. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x01	Erase Verify All Blocks	Verify that all P-Flash (and D-Flash) blocks are erased.
0x02	Erase Verify Block	Verify that a P-Flash block is erased.
0x03	Erase Verify P-Flash Section	Verify that a given number of words starting at the address provided are erased.

(CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

Table 15-44. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 15-27)
	FPVIOL	Set if any area of the P-Flash or D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[1]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[1]

1 As found in the memory map for FTMRC64K1.

15.4.5.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or D-Flash block.

Table 15-45. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [17:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 15-46. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 15-27)
		Set if an invalid global address [17:16] is supplied[1]
		Set if the supplied P-Flash address is not phrase-aligned or if the D-Flash address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation[2]
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation[2]

1 As defined by the memory map for FTMRC64K1.

2 As found in the memory map for FTMRC64K1.

P-Flash phrase containing the D-Flash protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the D-Flash memory fully protected.

Trying to alter data in any protected area in the D-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the D-Flash memory is not possible if any of the D-Flash sectors are protected.

Table 16-21. DFPROT Field Descriptions

Field	Description
7 DPOPEN	**D-Flash Protection Control** 0 Enables D-Flash memory protection from program and erase with protected address range defined by DPS bits 1 Disables D-Flash memory protection from program and erase
3–0 DPS[3:0]	**D-Flash Protection Size** — The DPS[3:0] bits determine the size of the protected area in the D-Flash memory as shown in Table 16-22.

16.3.2.11 Flash Common Command Object Register (FCCOB)

Table 16-22. D-Flash Protection Address Range

DPS[3:0]	Global Address Range	Protected Size
0000	0x0_4400 – 0x0_44FF	256 bytes
0001	0x0_4400 – 0x0_45FF	512 bytes
0010	0x0_4400 – 0x0_46FF	768 bytes
0011	0x0_4400 – 0x0_47FF	1024 bytes
0100	0x0_4400 – 0x0_48FF	1280 bytes
0101	0x0_4400 – 0x0_49FF	1536 bytes
0110	0x0_4400 – 0x0_4AFF	1792 bytes
0111	0x0_4400 – 0x0_4BFF	2048 bytes
1000	0x0_4400 – 0x0_4CFF	2304 bytes
1001	0x0_4400 – 0x0_4DFF	2560 bytes
1010	0x0_4400 – 0x0_4EFF	2816 bytes
1011	0x0_4400 – 0x0_4FFF	3072 bytes
1100	0x0_4400 – 0x0_50FF	3328 bytes
1101	0x0_4400 – 0x0_51FF	3584 bytes
1110	0x0_4400 – 0x0_52FF	3840 bytes
1111	0x0_4400 – 0x0_53FF	4096 bytes

The FCCOB is an array of six words addressed via the CCOBIX index found in the FCCOBIX register. Byte wide reads and writes are allowed to the FCCOB register.

Table 17-15. FERSTAT Field Descriptions

Field	Description
1 DFDIF	**Double Bit Fault Detect Interrupt Flag** — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation.[1] The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF. 0 No double bit fault detected 1 Double bit fault detected or an invalid Flash array read operation attempted
0 SFDIF	**Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation.[1] The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or an invalid Flash array read operation attempted

[1] The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault but never both). A simultaneous access collision (read attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

17.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Offset Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	FPOPEN	RNV6	FPHDIS	FPHS[1:0]		FPLDIS	FPLS[1:0]	
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 17-13. Flash Protection Register (FPROT)

The (unreserved) bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased (see Section 17.3.2.9.1, “P-Flash Protection Restrictions,” and Table 17-20).

During the reset sequence, the FPROT register is loaded with the contents of the P-Flash protection byte in the Flash configuration field at global address 0x3_FF0C located in P-Flash memory (see Table 17-3) as indicated by reset condition ‘F’ in Figure 17-13. To change the P-Flash protection that will be loaded during the reset sequence, the upper sector of the P-Flash memory must be unprotected, then the P-Flash protection byte must be reprogrammed. If a double bit fault is detected while reading the P-Flash phrase containing the P-Flash protection byte during the reset sequence, the FPOPEN bit will be cleared and remaining bits in the FPROT register will be set to leave the P-Flash memory fully protected.

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table A-9. Peripheral Configurations for Run & Wait Current Measurement

Peripheral	Configuration
MSCAN	configured to loop-back mode using a bit rate of 1 Mbit/s
SPI	configured to master mode, continously transmit data (0x55 or 0xAA) at 1 Mbit/s
SCI	configured into loop mode, continously transmit data (0x55) at speed of 57600 baud
PWM	configured to toggle its pins at the rate of 40 kHz
IIC	operate in master mode and continuously transimit data(0x55 or 0xAA) at 100Kbits/s
LCD	configured to 244Hz frame frequency, 1/4 Duty, 1/3 Bias with all FP/BP enabled and all segment on
MC	configured to full H-bridge mode MCPER=0x3FF, 1/2fbus motor controller timer counter clock, MCDC=0x20
ATD	the peripheral is configured to operate at its maximum specified frequency and to continuously convert voltages on all input channels in sequence.
DBG	the module is enabled and the comparators are configured to trigger in outside range.The range covers all the code executed by the core.
TIM0, TIM1	the peripheral shall be configured to output compare mode, pulse accumulator and modulus counter enabled.
COP & RTI	enabled

Table A-10. Run and Wait Current Characteristics

Conditions are shown in Table A-8 and Table A-9 unless otherwise noted, V_{DD35}=5.5v, 150°C							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	IDD Run Current	I_{DDR}		17	20	mA
2	P	IDD Wait Current	I_{DDW}		9.5	12	mA

Figure C-5. 64-pin LQFP (case no. 840F) - page 2

0x0267-0x026F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0270	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0271	PT1AD	R	PT1AD7	PT1AD6	PT1AD5	PT1AD4	PT1AD3	PT1AD2	PT1AD1	PT1AD0
		W								
0x0272	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0273	DDR1AD	R	DDR1AD7	DDR1AD6	DDR1AD5	DDR1AD4	DDR1AD3	DDR1AD2	DDR1AD1	DDR1AD0
		W								
0x0274	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0275	RDR1AD	R	RDR1AD7	RDR1AD6	RDR1AD5	RDR1AD4	RDR1AD3	RDR1AD2	RDR1AD1	RDR1AD0
		W								
0x0276	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0277	PER1AD	R	PER1AD7	PER1AD6	PER1AD5	PER1AD4	PER1AD3	PER1AD2	PER1AD1	PER1AD0
		W								
0x0278-0x027F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0280	PTR	R	PTR7	PTR6	PTR5	PTR4	PTR3	PTR2	PTR1	PTR0
		W								
0x0281	PTIR	R	PTIR7	PTIR6	PTIR5	PTIR4	PTIR3	PTIR2	PTIR1	PTIR0
		W								
0x0282	DDRR	R	DDRR7	DDRR6	DDRR5	DDRR4	DDRR3	DDRR2	DDRR1	DDRR0
		W								
0x0283	RDRR	R	RDRR7	RDRR6	RDRR5	RDRR4	RDRR3	RDRR2	RDRR1	RDRR0
		W								
0x0284	PERR	R	PERR7	PERR6	PERR5	PERR4	PERR3	PERR2	PERR1	PERR0
		W								
0x0285	PPSR	R	PPSR7	PPSR6	PPSR5	PPSR4	PPSR3	PPSR2	PPSR1	PPSR0
		W								
0x0286	WOMR	R	WOMR7	WOMR6	WOMR5	WOMR4	WOMR3	WOMR2	WOMR1	WOMR0
		W								
0x0287	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0288	PIET	R	PIET7	PIET6	PIET5	PIET4	PIET3	PIET2	PIET1	PIET0
		W								
0x0289	PIFT	R	PIFT7	PIFT6	PIFT5	PIFT4	PIFT3	PIFT2	PIFT1	PIFT0
		W								