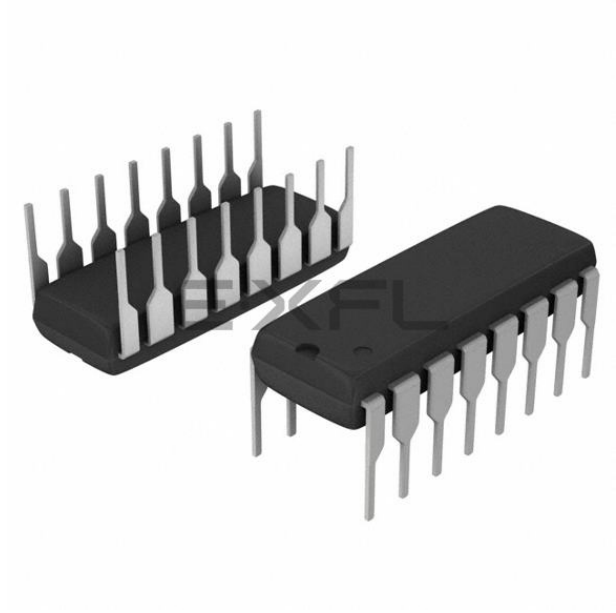

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp216-20pu

9. System Clock

The system clock is generated directly from one of three selectable clock sources. The three sources are the on-chip crystal oscillator, external clock source, and internal RC oscillator. The clock source is selected by the Clock Source User Fuses as shown in Table 9-1. No internal clock division is used to generate the CPU clock from the system clock. See “User Configuration Fuses” on page 71.

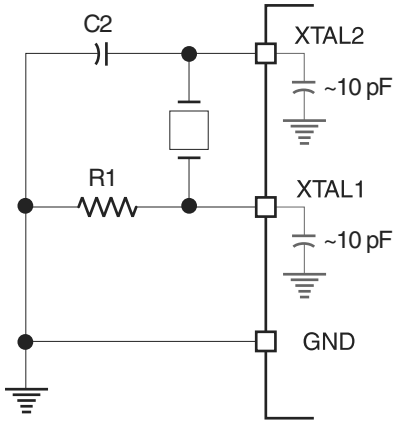
Table 9-1. Clock Source Settings

Clock Source Fuse 1	Clock Source Fuse 0	Selected Clock Source
0	0	Crystal Oscillator
0	1	Reserved
1	0	External Clock on XTAL1
1	1	Internal 8 MHz RC Oscillator

9.1 Crystal Oscillator

When enabled, the internal inverting oscillator amplifier is connected between XTAL1 and XTAL2. Note that the internal structure of the device adds about 10 pF of capacitance to both XTAL1 and XTAL2, so that in some cases an external capacitor may **NOT** be required. It is recommended that a resistor R1 be connected to XTAL1, instead of load capacitor C1, for improved startup performance. The total capacitance on XTAL1 or XTAL2, including the external load capacitor plus internal device load, board trace and crystal loadings, should not exceed 20 pF. When using the crystal oscillator, P3.2 and P3.3 will have their inputs and outputs disabled. When using the crystal oscillator, XTAL2 should not be used to drive a board-level clock without a buffer

Figure 9-1. Crystal Oscillator Connections



Note: 1. C2 = 0–10 pF for Crystals
= 0–10 pF for Ceramic Resonators
R1 = 4–5 M

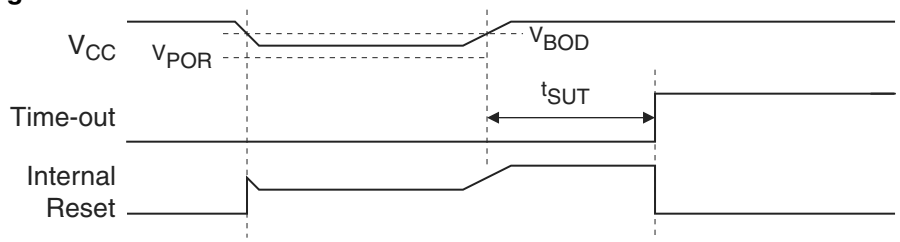
Table 10-1. Start-up Timer Settings

SUT Fuse 1	SUT Fuse 0	Clock Source	t_{SUT} (± 5%)
0	0	Internal RC/External Clock	16 µs
		Crystal Oscillator	1024 µs
0	1	Internal RC/External Clock	512 µs
		Crystal Oscillator	2048 µs
1	0	Internal RC/External Clock	1024 µs
		Crystal Oscillator	4096 µs
1	1	Internal RC/External Clock	4096 µs
		Crystal Oscillator	16384 µs

10.2 Brown-out Reset

The AT89LP216 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{CC} level during operation by comparing it to a fixed trigger level. The trigger level for the BOD is nominally 2.2V. The purpose of the BOD is to ensure that if V_{CC} fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. A BOD sequence is shown in Figure 10-3. When V_{CC} decreases to a value below the trigger level V_{BOD}, the internal reset is immediately activated. When V_{CC} increases above the trigger level, the start-up timer releases the internal reset after the specified time-out period has expired (Table 10-1). The Brown-out Detector must be enabled by setting the BOD Enable Fuse. (See “User Configuration Fuses” on page 71.)

Figure 10-3. Brown-out Detector Reset



10.3 External Reset

The P1.3/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital general-purpose I/O, P1.3. The Reset Pin Enable Fuse, when set to “1”, enables the external reset input function on P1.3. (See “User Configuration Fuses” on page 71.) When cleared, P1.3 may be used as an input or output pin. When configured as a reset input, the pin must be held low for at least two clock cycles to trigger the internal reset.

Note: During a power-up sequence, the fuse selection is always overridden and therefore the pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset until the pin transitions high**. After the power-up delay, this input will function either as an external reset input or as a digital input as defined by the fuse bit. Only a power-up reset will temporarily override the selection defined by the reset fuse bit. Other sources of reset will not override the reset fuse bit. P1.3/$\overline{\text{RST}}$ also serves as the In-System Programming (ISP) enable. ISP is enabled when the external reset pin is held low. When the reset pin is disabled by the fuse, ISP may only be entered by pulling P1.3 low during power-up.

Table 13-2. Configuration Modes for Port x, Bit y

PxM0.y	PxM1.y	Port Mode
0	0	Quasi-bidirectional
0	1	Push-pull Output
1	0	Input Only (High Impedance)
1	1	Open-drain Output

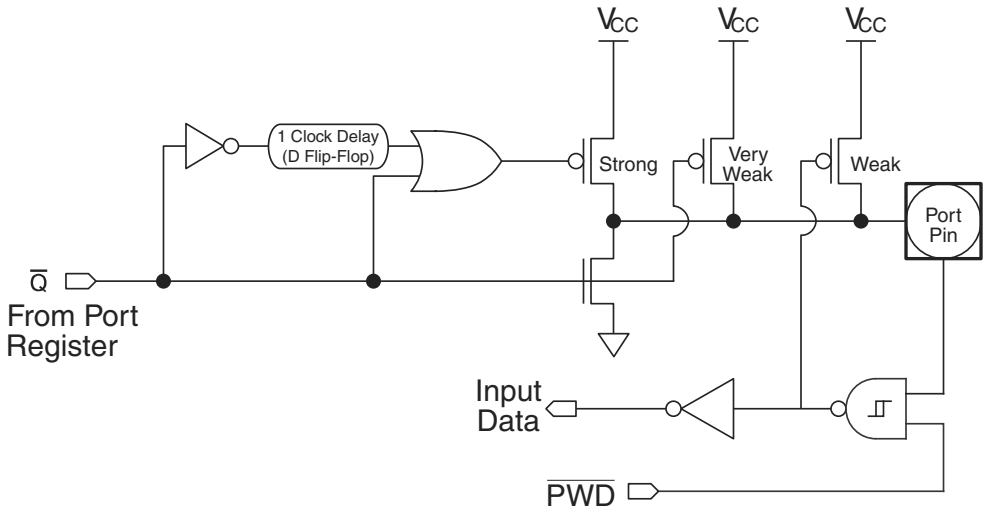
13.1.1 Quasi-bidirectional Output

Port pins in quasi-bidirectional output mode function similar to standard 8051 port pins. A Quasi-bidirectional port can be used both as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is driven low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a “1”. If this pin is pulled low by an external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the port pin below its input threshold voltage.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for two CPU clocks quickly pulling the port pin high. The quasi-bidirectional port configuration is shown in Figure 13-1. The input circuitry of P1.3, P3.2 and P3.3 is not disabled during Power-down (see Figure 13-3).

Figure 13-1. Quasi-bidirectional Output



13.1.2 Input-only Mode

The input only port configuration is shown in Figure 13-2. The output drivers are tristated. The input includes a Schmitt-triggered input for improved input noise rejection. The input circuitry of P1.3, P3.2 and P3.3 is not disabled during Power-down (see Figure 13-3). Input pins can be safely driven to 5.5V even when operating at lower V_{CC} levels; however, the input threshold of the Schmitt trigger will be set by the V_{CC} level and must be taken into consideration.

Figure 13-2. Input Only

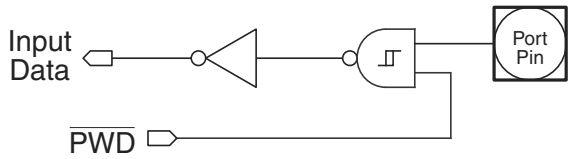
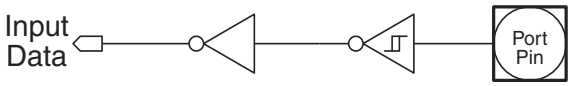


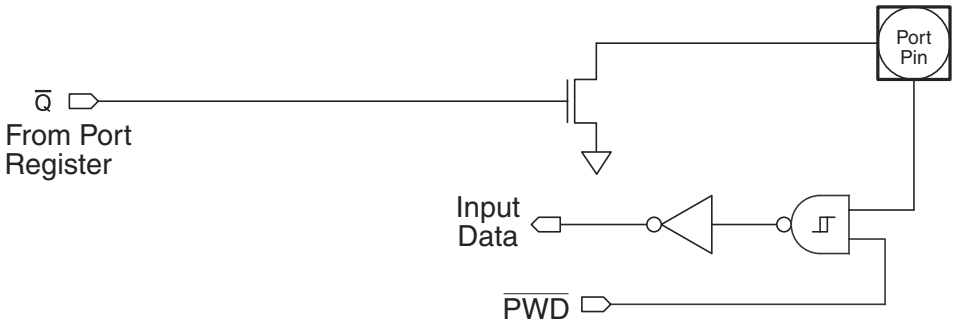
Figure 13-3. Input Only for P1.3, P3.2 and P3.3



13.1.3 Open-drain Output

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port pin when the port latch contains a logic “0”. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{CC}. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open-drain port configuration is shown in Figure 13-4.The input circuitry of P1.3, P3.2 and P3.3 is not disabled during Power-down (see Figure 13-3). Open-drain pins can be safely pulled high to 5.5V even when operating at lower V_{CC} levels; however, the input threshold of the Schmitt trigger will be set by the V_{CC} level and must be taken into consideration.

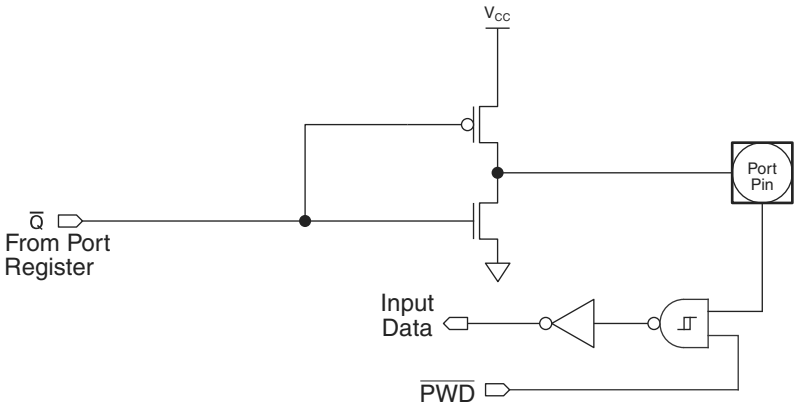
Figure 13-4. Open-drain Output



13.1.4 Push-pull Output

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic “1”. The push-pull mode may be used when more source current is needed from a port output. Note that due to the 5V tolerant architecture, the push-pull output will have reduced output high levels at DC operation and hot temperature. Under AC operation an integrated boost circuit provides more source current. The push-pull port configuration is shown in Figure 13-5. The input circuitry of P1.3, P3.2 and P3.3 is not disabled during Power-down (see Figure 13-3).

Figure 13-5. Push-pull Output



13.2 Port 1 Analog Functions

The AT89LP216 incorporates an analog comparator. In order to give the best analog performance and minimize power consumption, pins that are being used for analog functions must have both their digital outputs and digital inputs disabled. Digital outputs are disabled by putting the port pins into the input-only mode as described in "Port Configuration" on page 22. Digital inputs on P1.0 and P1.1 are disabled whenever the Analog Comparator is enabled by setting the CEN bit in ACSR. CEN forces the $\overline{PWD}$ input on P1.0 and P1.1 low, thereby disabling the Schmitt trigger circuitry. P1.0 and P1.1 will always default to input-only mode after reset regardless of the state of the Tristate-Port Fuse.

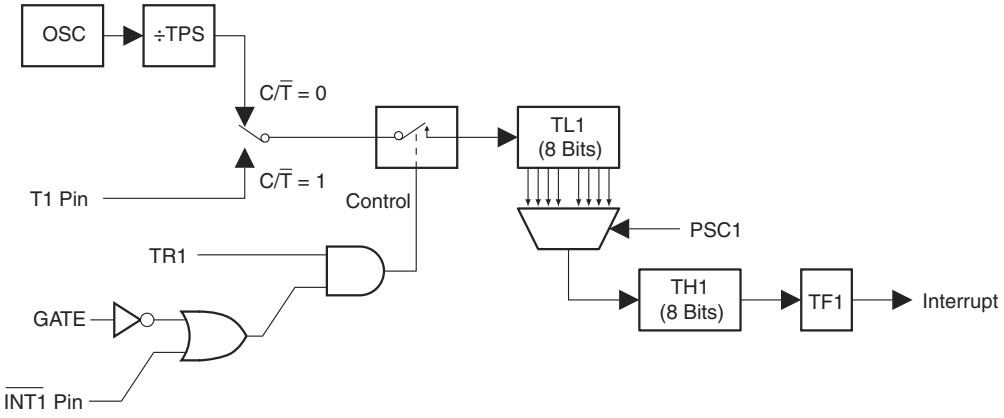
13.3 Port Read-modify-write

A read from a port will read either the state of the pins or the state of the port register depending on which instruction is used. Simple read instructions will always access the port pins directly. Read-modify-write instructions, which read a value, possibly modify it, and then write it back, will always access the port register. This includes bit write instructions such as CLR or SETB as they actually read the entire port, modify a single bit, then write the data back to the entire port. See Table 13-3 for a complete list of Read-modify-write instruction which may access the ports.

Table 13-3. Port Read-modify-write Instructions

Mnemonic	Instruction	Example
ANL	Logical AND	ANL P1, A
ORL	Logical OR	ORL P1, A
XRL	Logical EX-OR	XRL P1, A
JBC	Jump if bit set and clear bit	JBC P3.0, LABEL
CPL	Complement bit	CPL P3.1
INC	Increment	INC P1
DEC	Decrement	DEC P3
DJNZ	Decrement and jump if not zero	DJNZ P3, LABEL
MOV PX.Y, C	Move carry to bit Y of Port X	MOV P1.0, C
CLR PX.Y	Clear bit Y of Port X	CLR P1.1
SETB PX.Y	Set bit Y of Port X	SETB P3.2

Figure 14-1. Timer/Counter 1 Mode 0: Variable Width Counter



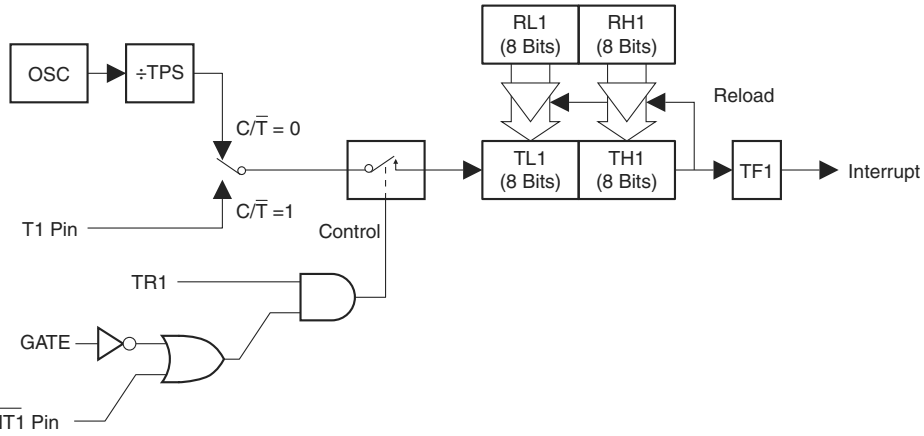
Mode 0 operation is the same for Timer 0 as for Timer 1, except that TR0, TF0 and $\overline{INT0}$ replace the corresponding Timer 1 signals in Figure 14-1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3). The $\overline{INT0}$ and $\overline{INT1}$ pins are shared with the XTAL oscillator. They may only be used for the GATE function when using the internal RC oscillator as the system clock.

14.2 Mode 1 – 16-bit Auto-Reload Timer/Counter

In Mode 1 the Timers are configured for 16-bit auto-reload. The Timer register is run with all 16 bits. The 16-bit reload value is stored in the high and low reload registers (RH1/RL1). The clock is applied to the combined high and low timer registers (TH1/TL1). As clock pulses are received, the timer counts up: 0000H, 0001H, 0002H, etc. An overflow occurs on the FFFFH-to-0000H transition, upon which the timer register is reloaded with the value from RH1/RL1 and the overflow flag bit in TCON is set. See Figure 14-2. The reload registers default to 0000H, which gives the full 16-bit timer period compatible with the standard 8051. Mode 1 operation is the same for Timer/Counter 0.

$$\text{Mode 1:} \qquad \text{Time-out Period} = \frac{(65536 - \{RH0, RL0\})}{\text{Oscillator Frequency}} \times (TPS + 1)$$

Figure 14-2. Timer/Counter 1 Mode 1: 16-bit Auto-reload

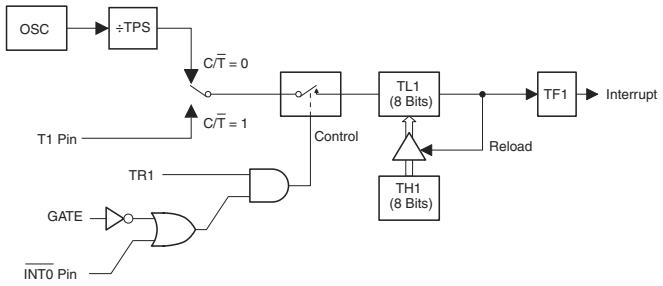


14.3 Mode 2 – 8-bit Auto-reload Timer/Counter

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 14-3. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves TH1 unchanged. Mode 2 operation is the same for Timer/Counter 0.

$$\text{Mode 2:} \qquad \text{Time-out Period} = \frac{(256 - \text{TH0})}{\text{Oscillator Frequency}} \times (\text{TPS} + 1)$$

Figure 14-3. Timer/Counter 1 Mode 2: 8-bit Auto-reload



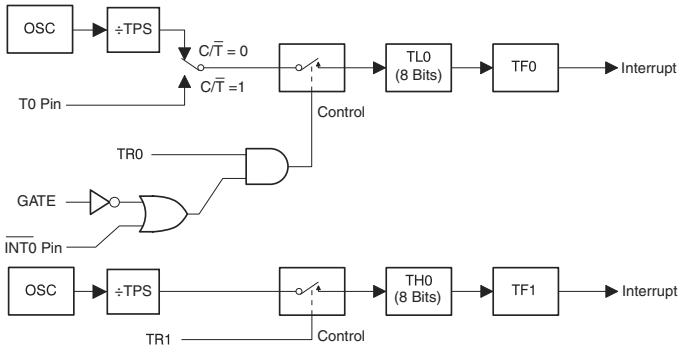
Note: RH1/RL1 are not required by Timer 1 during Mode 2 and may be used as temporary storage registers.

14.4 Mode 3 – 8-bit Split Timer

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 14-4. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, $\overline{\text{INT0}}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt. While Timer 0 is in Mode 3, Timer 1 will still obey its settings in TMOD but cannot generate an interrupt.

Mode 3 is for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, the AT89LP216 can appear to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt.

Figure 14-4. Timer/Counter 0 Mode 3: Two 8-bit Counters



Note: RH0/RL0 are not required by Timer 0 during Mode 3 and may be used as temporary storage registers.

15. External Interrupts

When the AT89LP216 is configured to use the internal RC Oscillator, XTAL1 and XTAL2 may be used as the $\overline{INT0}$ and $\overline{INT1}$ external interrupt sources. When the external clock source is used, XTAL2 is available as INT1. Neither interrupt is available in crystal oscillator mode.The external interrupts can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{INTx}$ pin. If ITx = 1, external interrupt x is edge-triggered. In this mode if successive samples of the $\overline{INTx}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt. Since the external interrupt pins are sampled once each clock cycle, an input high or low should hold for at least 2 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least two clock cycles, and then hold it low for at least two clock cycles to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called if generated in edge-triggered mode. If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then the external source must deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

16. General-purpose Interrupts

The General-purpose Interrupt (GPI) function provides 8 configurable external interrupts on Port 1. Each port pin can detect high/low levels or positive/negative edges. The GPIEN register select which bits of Port 1 are enabled to generate an interrupt. The GPMOD and GPLS registers determine the mode for each individual pin. GPMOD selects between level-sensitive and edge-triggered mode. GPLS selects between high/low in level mode and positive/negative in edge mode. The pins of Port 1 are sampled every clock cycle. In level-sensitive mode, a valid level must appear in two successive samples before generating the interrupt. In edge-triggered mode, a transition will be detected if the value changes from one sample to the next. When an interrupt condition on a pin is detected, and that pin is enabled, the appropriate flag in the GPIF register is set. The flags in GPIF must be cleared by software.

Table 16-1. GPMOD – General-purpose Interrupt Mode Register

GPMOD = 9AH — Reset Value = 0000 0000B

Not Bit Addressable

	GPMOD7	GPMOD6	GPMOD5	GPMOD4	GPMOD3	GPMOD2	GPMOD1	GPMOD0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = level-sensitive interrupt for P1.x

1 = edge-triggered interrupt for P1.x

Table 16-2. GPLS – General-purpose Interrupt Level Select Register

GPLS = 9BH — Reset Value = 0000 0000B

Not Bit Addressable

	GPLS7	GPLS6	GPLS5	GPLS4	GPLS3	GPLS2	GPLS1	GPLS0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = detect low level or negative edge on P1.x

1 = detect high level or positive edge on P1.x

Table 16-3. GPIEN – General-purpose Interrupt Enable Register

GPIEN = 9CH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIEN7	GPIEN6	GPIEN5	GPIEN4	GPIEN3	GPIEN2	GPIEN1	GPIEN0
Bit	7	6	5	4	3	2	1	0

GPIEN.x 0 = interrupt for P1.x disabled

1 = interrupt for P1.x enabled

Table 16-4. GPIF – General-purpose Interrupt Flag Register

GPIF = 9DH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIF7	GPIF6	GPIF5	GPIF4	GPIF3	GPIF2	GPIF1	GPIF0
Bit	7	6	5	4	3	2	1	0

GPIF.x 0 = interrupt on P1.x inactive

1 = interrupt on P1.x active. Must be cleared by software.

Figure 18-3. Serial Port Mode 2

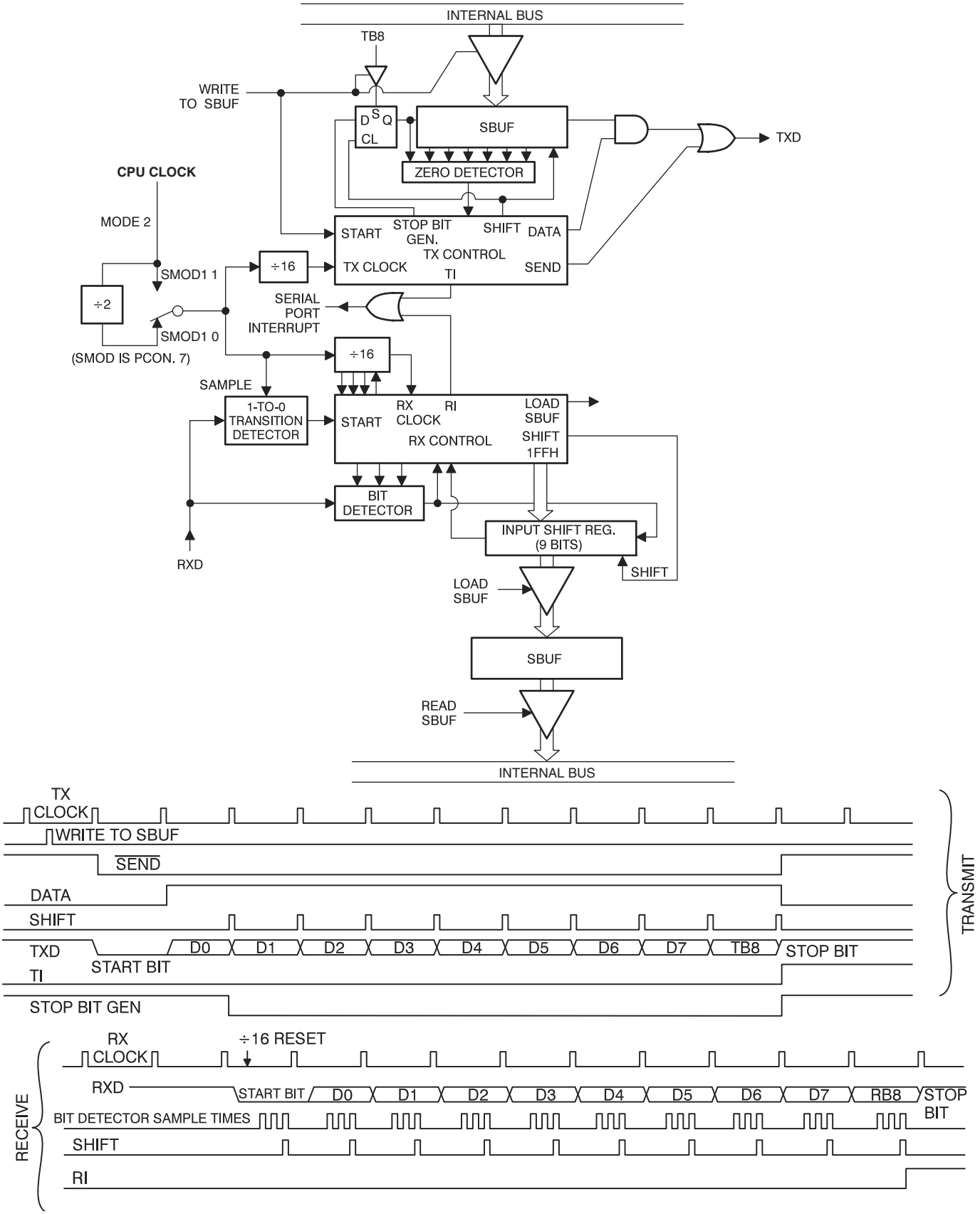


Figure 18-4. Serial Port Mode 3

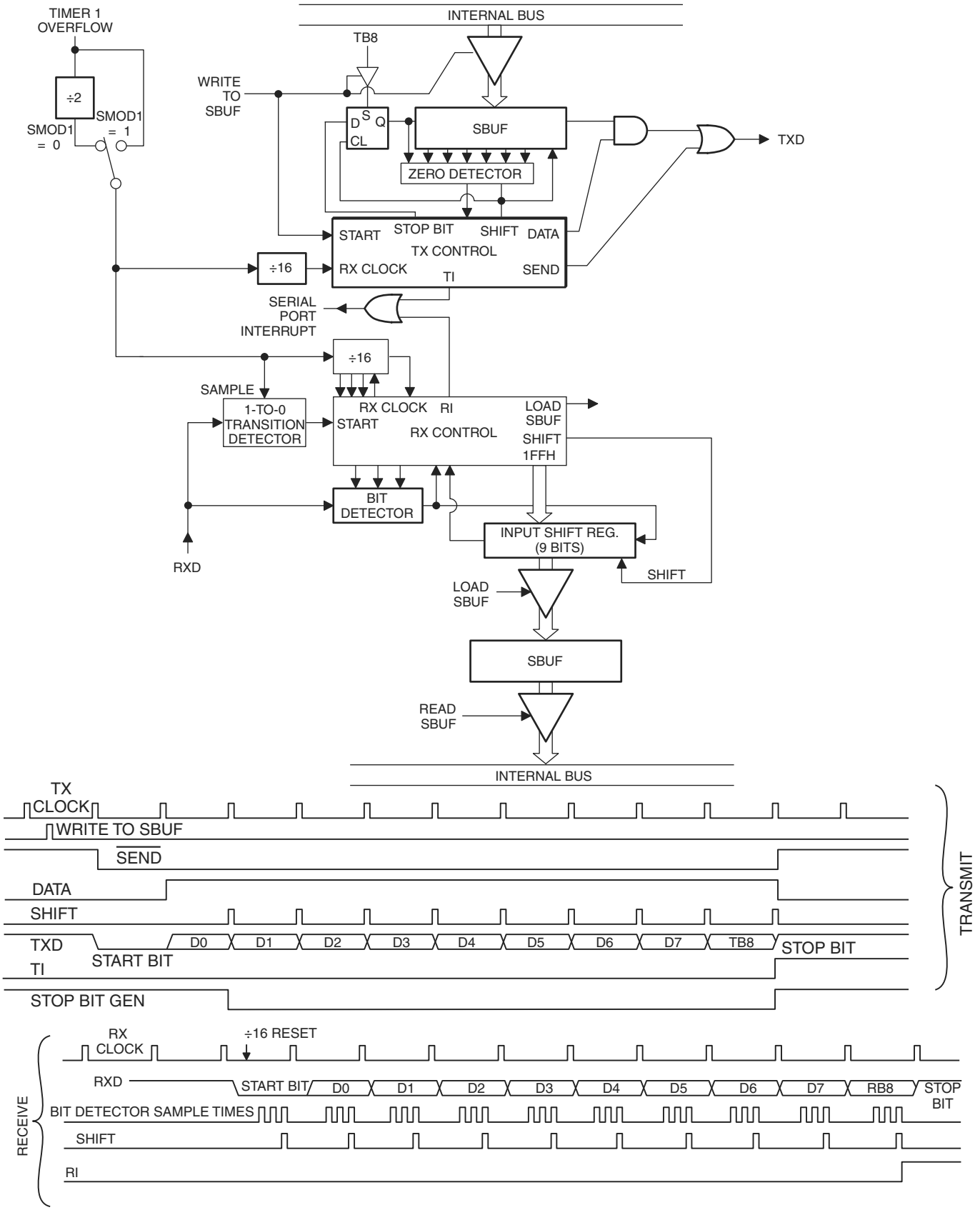


Table 19-1. SPCR – SPI Control Register

SPCR Address = E9H — Reset Value = 0000 0000B

Not Bit Addressable

	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI interrupt enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/slave select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects slave SPI mode.
CPOL	Clock polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI clock phase and polarity control.
CPHA	Clock phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI clock phase and polarity control.
SPR0 SPR1	SPI clock rate select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{OSC.}$, is as follows: SPR1 SPR0 SCK 0 0 $f_{OSC}/4$ 0 1 $f_{OSC}/8$ 1 0 $f_{OSC}/32$ 1 1 $f_{OSC}/64$

Notes: 1. Set up the clock mode before enabling the SPI: set all bits needed in SPCR except the SPE bit, then set SPE.
2. Enable the master SPI prior to the slave device.
3. Slave echoes master on the next Tx if not loaded with new data.

Table 19-2. SPDR – SPI Data Register

SPDR Address = EAH

Not Bit Addressable

Reset Value = 00H (after cold reset)
unchanged (after warm reset)

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Figure 19-2. SPI Shift Register Diagram

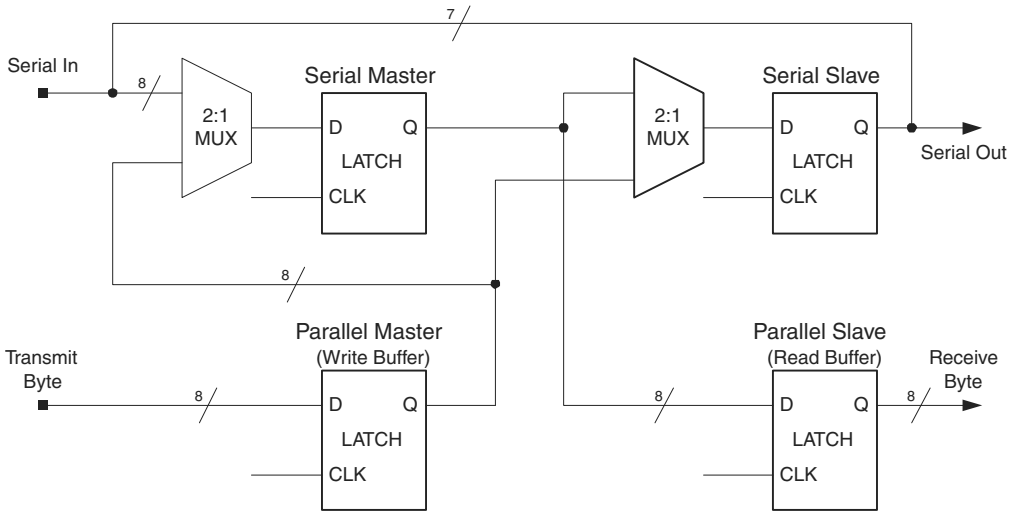
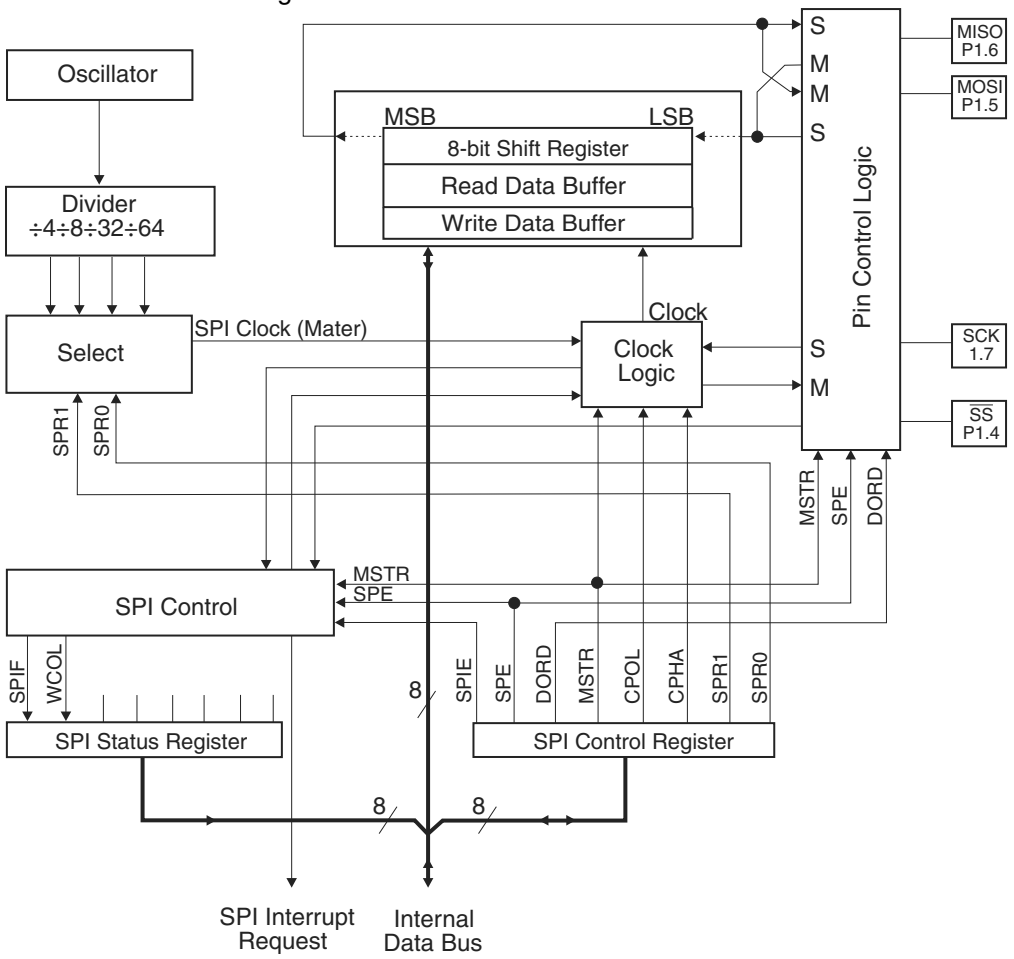
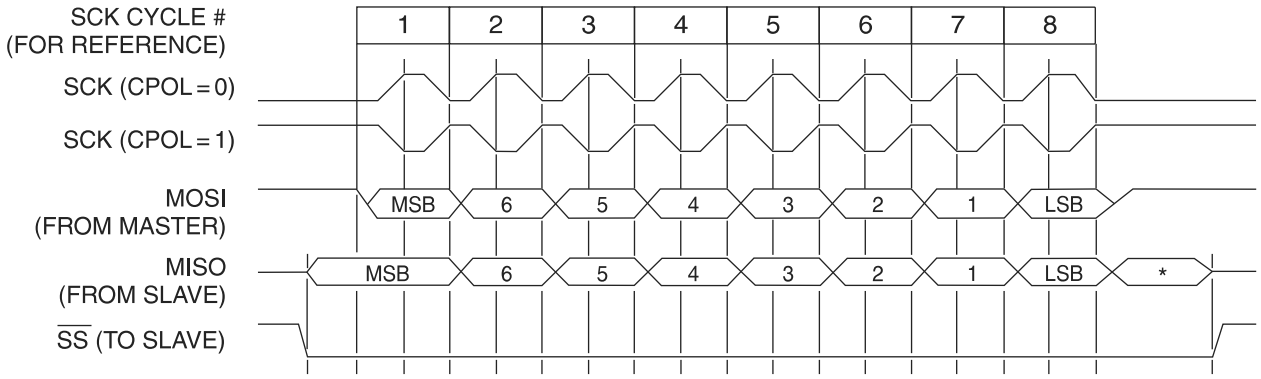


Figure 19-3. SPI Block Diagram



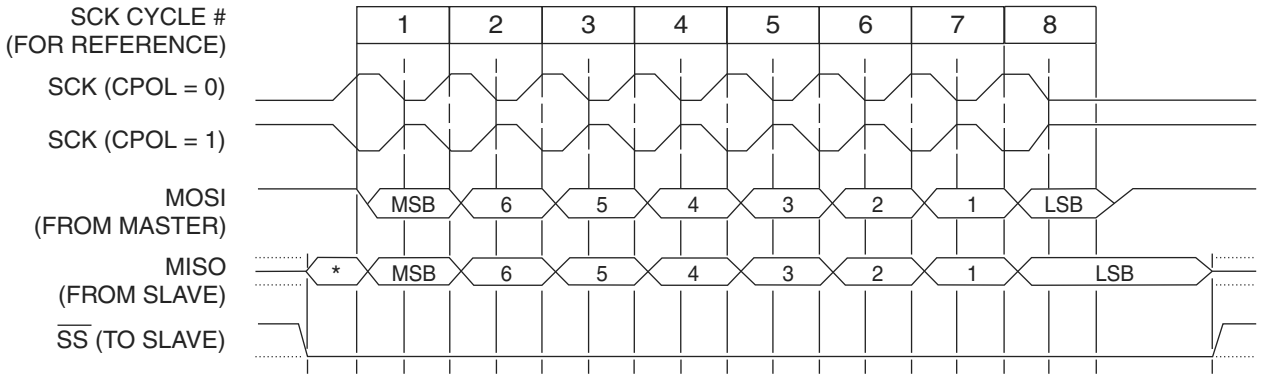
The CPHA (Clock PHAse), CPOL (Clock POLarity), and SPR (Serial Peripheral clock Rate = baud rate) bits in SPCR control the shape and rate of SCK. The two SPR bits provide four possible clock rates when the SPI is in master mode. In slave mode, the SPI will operate at the rate of the incoming SCK as long as it does not exceed the maximum bit rate. There are also four possible combinations of SCK phase and polarity with respect to the serial data. CPHA and CPOL determine which format is used for transmission. The SPI data transfer formats are shown in Figures 19-4 and 19-5. To prevent glitches on SCK from disrupting the interface, CPHA, CPOL, and SPR should not be modified while the interface is enabled, and the master device should be enabled before the slave device(s).

Figure 19-4. SPI Transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received.

Figure 19-5. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character.

Table 20-1. ACSR – Analog Comparator Control & Status Register

ACSR = 97H — Reset Value = XXX0 0000B

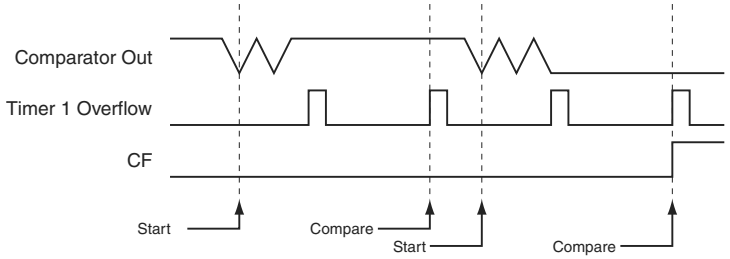
Not Bit Addressable

	–	–	CIDL	CF	CEN	CM3	CM1	CM0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Comparator Idle Enable. If CIDL = 1 the comparator will continue to operate during Idle mode. If CIDL = 0 the comparator is powered down during Idle mode. The comparator is always shut down during Power-down mode.
CF	Comparator Interrupt Flag. Set when the comparator output meets the conditions specified by the CM [2:0] bits and CEN is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
CEN	Comparator Enable. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CF. When CEN = 1 the analog input pins, P1.0 and P1.1, have their digital inputs disabled.
CM [2:0]	Comparator Interrupt Mode CM2 CM1 CM0 Interrupt Mode 0 0 0 Negative (Low) level 0 0 1 Positive edge 0 1 0 Toggle with debouncing(1) 0 1 1 Positive edge with debouncing(1) 1 0 0 Negative edge 1 0 1 Toggle 1 1 0 Negative edge with debouncing(1) 1 1 1 Positive (High) level

Note: 1. Debouncing modes require the use of Timer 1 to generate the sampling delay.

Figure 20-1. Negative Edge with Debouncing Example



21.1 Software Reset

A Software Reset of the AT89LP216 is accomplished by writing the software reset sequence 5AH/A5H to the WDTRST SFR. The WDT does not need to be enabled to generate the software reset. A normal software reset will set the SWRST flag in WDTCON. However, if at any time an incorrect sequence is written to WDTRST (i.e. anything other than 1EH/E1H or 5AH/A5H), a software reset will immediately be generated and both the SWRST and WDTOVF flags will be set. In this manner an intentional software reset may be distinguished from a software error-generated reset. The program sequence to generate a software reset is as follows:

```
MOV WDTRST, #05Ah

MOV WDTRST, #0A5h
```

Table 21-2. WDTCON – Watchdog Control Register

WDTCON Address = A7H — Reset Value = 0000 X000B

Not Bit Addressable

	PS2	PS1	PS0	WDIDLE	–	SWRST	WDTOVF	WDTEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler bits for the watchdog timer (WDT). When all three bits are cleared to 0, the watchdog timer has a nominal period of 16K clock cycles. When all three bits are set to 1, the nominal period is 2048K clock cycles.
WDIDLE	Disable/enable the Watchdog Timer in IDLE mode. When WDIDLE = 0, WDT continues to count in IDLE mode. When WDIDLE = 1, WDT freezes while the device is in IDLE mode.
SWRST	Software Reset Flag. Set when a software reset is generated by writing the sequence 5AH/A5H to WDTRST. Also set when an incorrect sequence is written to WDTRST. Must be cleared by software.
WDTOVF	Watchdog Overflow Flag. Set when a WDT rest is generated by the WDT timer overflow. Also set when an incorrect sequence is written to WDTRST. Must be cleared by software.
WDTEN	Watchdog Enable Flag. This bit is READ-ONLY and reflects the status of the WDT (whether it is running or not). The WDT is disabled after any reset and must be re-enabled by writing 1EH/E1H to WDTRST

Table 21-3. WDTRST – Watchdog Reset Register

WDTCON Address = A6H — (Write-Only)

Not Bit Addressable

	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0

The WDT is enabled by writing the sequence 1EH/E1H to the WDTRST SFR. The current status may be checked by reading the WDTEN bit in WDTCON. To prevent the WDT from resetting the device, the same sequence 1EH/E1H must be written to WDTRST before the time-out interval expires. A software reset is generated by writing the sequence 5AH/A5H to WDTRST.

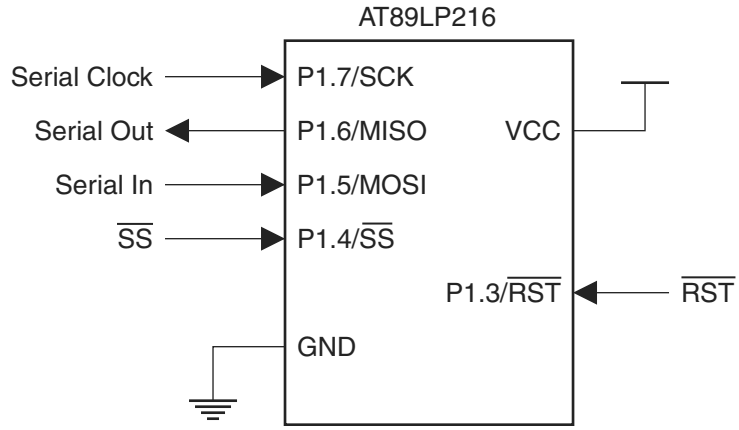
- Flexible Page Programming
- Row Erase Capability
- Page Write with Auto-Erase Commands
- Programming Status Register

For more detailed information on In-System Programming, refer to the Application Note entitled “AT89LP In-System Programming Specification”.

24.1 Physical Interface

In-System Programming utilizes the Serial Peripheral Interface (SPI) pins of an AT89LP216 microcontroller. The SPI is a full duplex synchronous serial interface consisting of four wires: Serial Clock (SCK), Master-In/Slave-out (MISO), Master-out/Slave-in (MOSI), and an active-low Slave Select ($\overline{SS}$). When programming an AT89LP216 device, the programmer always operates as the SPI master, and the target system always operates as the SPI slave. To enter or remain in In-System Programming mode the device’s reset line ($\overline{RST}$) must be held active (low). With the addition of VCC and GND, an AT89LP216 microcontroller can be programmed with a minimum of seven connections as shown in Figure 24-1.

Figure 24-1. In-System Programming Device Connections



The In-System Programming Interface is the only means of externally programming the AT89LP216 microcontroller. The ISP Interface can be used to program the device both in-system and in a stand-alone serial programmer. The ISP Interface does not require any clock other than SCK and is not limited by the system clock frequency. During In-System programming the system clock source of the target device can operate normally.

When designing a system where In-System Programming will be used, the following observations must be considered for correct operation:

- The ISP interface uses the SPI clock mode 0 (CPOL = 0,CPHA = 0) exclusively with a maximum frequency of 5 MHz.
- The AT89LP216 will enter programming mode only when its reset line ($\overline{RST}$) is active (low). To simplify this operation, it is recommended that the target reset can be controlled by the In-System programmer. To avoid problems, the In-System programmer should be able to keep the entire target system reset for the duration of the programming cycle. The target system should never attempt to drive the four SPI lines while reset is active.

24.7 User Configuration Fuses

The AT89LP216 includes 19 user fuses for configuration of the device. Each fuse is accessed at a separate address in the User Fuse Row as listed in Table 24-5. Fuses are cleared by programming 00h to their locations. Programming FFh to fuse location will cause that fuse to maintain its previous state. To set a fuse (set to FFh) the fuse row must be erased and then reprogrammed using the Fuse Write with Auto-erase command. The default state for all fuses is FFh.

Table 24-5. User Configuration Fuse Definitions

Address	Fuse Name	Description
00 – 01h	Clock Source – CS[0:1](2)	Selects source for the system clock: CS1 CS0 Selected Source 00h 00h Crystal Oscillator (XTAL) 00h FFh Reserved FFh 00h External Clock on XTAL1 (XCLK) FFh FFh Internal RC Oscillator (IRC)
02 – 03h	Start-up Time – SUT[0:1]	Selects time-out delay for the POR/BOD/PWD wake-up period: SUT1 SUT0 Selected Time-out 00h 00h 1 ms (XTAL); 16 µs (XCLK/IRC) 00h FFh 2 ms (XTAL); 512 µs (XCLK/IRC) FFh 00h 4 ms (XTAL); 1 ms (XCLK/IRC) FFh FFh 16 ms (XTAL); 4 ms (XCLK/IRC)
04h	Reset Pin Enable(3)	FFh: $\overline{\text{RST}}$ pin functions as reset 00h: $\overline{\text{RST}}$ pin functions as general purpose I/O
05h	Brown-out Detector Enable	FFh: Brown-out Detector Enabled 00h: Brown-out Detector Disabled
06h	On-chip Debug $\overline{\text{Enable}}$	FFh: On-chip Debug Disabled 00h: On-chip Debug Enabled
07h	ISP Enable(3)	FFh: In-System Programming Enabled 00h: In-System Programming Disabled (Enabled at POR only)
08 – 0FH	RC Oscillator Frequency Adjustment [0:7]	Adjusts the frequency of the internal RC oscillator. A copy of the 8MHz factory setting is stored at location 0008h of the Atmel Signature.
10H	User Signature Programming	FFh: Programming of User Signature Disabled 00h: Programming of User Signature Enabled
11H	Tristate Ports(4)	FFh: I/O Ports start in input-only mode (tristated) after reset 00h: I/O Ports start in quasi-bidirectional mode after reset
12H	OCD Interface Select	FFh: Fast two-wire interface 00h: Do not use

Notes:
1. The default state for all fuses is FFh.
2. Changes to these fuses will only take effect after a device POR.
3. Changes to these fuses will only take effect after the ISP session terminates by bringing $\overline{\text{RST}}$ high.
4. AIN0 (P1.0) and AIN1 (P1.1) always reset to input-only mode. $\overline{\text{SS}}$ (P1.4) always resets to quasi-bidirectional mode.

25. Electrical Characteristics

25.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +5.5V
Maximum Operating Voltage	5.5V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

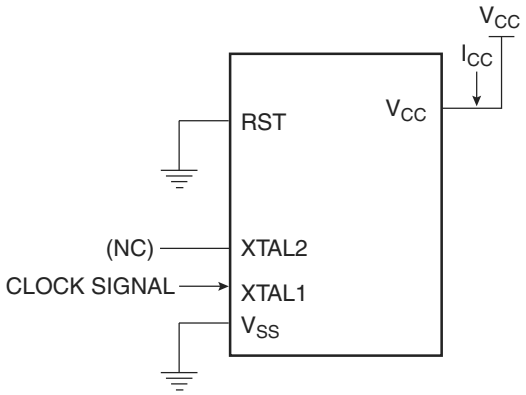
25.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.4V to 5.5V (unless otherwise noted)

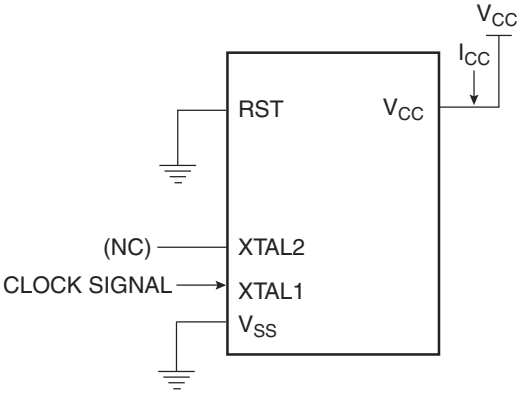
Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.3 V_{CC}	V
V_{IH}	Input High-voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1, 3)	I_{OL} = 10 mA, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3) With Weak Pull-ups Enabled	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.7 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Ports 1, 3) With Strong Pull-ups Enabled(2)	I_{OH} = -2 mA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -500 µA, V_{CC} = 5V ±10%	0.6 V_{CC}		V
		I_{OH} = -100 µA	0.6 V_{CC}		V
I_{IL}	Logic 0 Input Current (Quasi-Bidirectional Mode)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logic 1 to 0 Transition Current (Quasi-Bidirectional Mode)	V_{IN} = 2V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input Leakage Current (Input-Only Mode)	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-up Resistor		50	150	k
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5V/3V		10/6	mA
		Idle Mode, 12 MHz, V_{CC} = 5./3V		3/1.5	mA
	Power-down Mode(3)	V_{CC} = 5V, P1.0 & P1.1 = 0V or V_{CC}		5	µA
		V_{CC} = 3V, P1.0 & P1.1 = 0V or V_{CC}		2	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 15 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. V_{OH1} levels are listed for DC operation. Under AC conditions a boost circuit provides additional source current.
3. Minimum V_{CC} for Power-down is 2V.

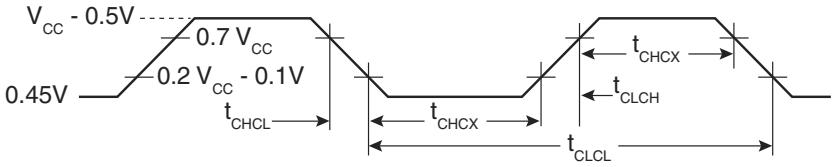
25.7.3 I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected



25.7.4 I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



25.7.5 Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns



25.7.6 I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{CC} = 2V to 5.5V