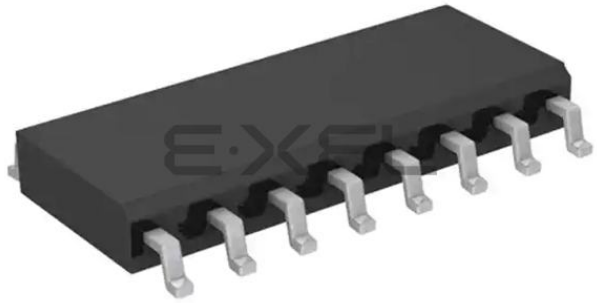

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp216-20su

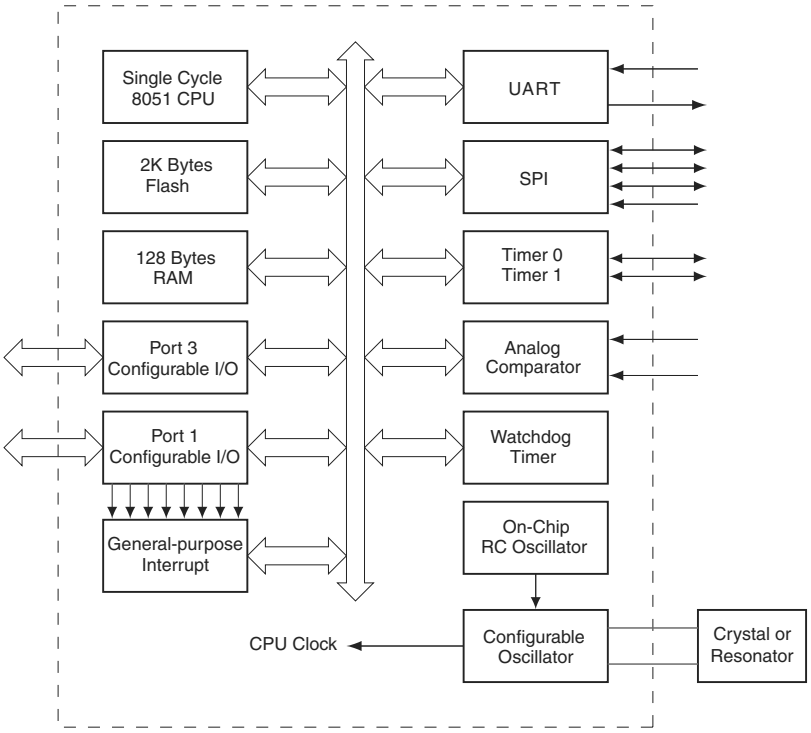
3. Pin Description

Table 3-1. Pin Description

Pin	Symbol	Type	Description
1	P1.5	I/O I/O I	**P1.5**: User-configurable I/O Port 1 bit 5. **MOSI**: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input. **GPI5**: General-purpose Interrupt input 5.
2	P1.7	I/O I/O I	**P1.7**: User-configurable I/O Port 1 bit 7. **SCK**: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input. **GPI7**: General-purpose Interrupt input 7.
3	P1.3	I/O I I I	**P1.3**: User-configurable I/O Port 1 bit 3 (if Reset Fuse is disabled). **$\overline{\text{RST}}$**: External **Active-Low** Reset input (if Reset Fuse is enabled, see Section 10.3 “External Reset” on page 15) **GPI3**: General-purpose Interrupt input 3. **DCL**: Serial Clock input for On-Chip Debug Interface when OCD is enabled.
4	GND	I	Ground
5	P1.2	I/O I	**P1.2**: User-configurable I/O Port 1 bit 2. **GPI2**: General-purpose Interrupt input 2.
6	P3.0	I/O I	**P3.0**: User-configurable I/O Port 3 bit 0. **RXD**: Serial Port Receiver Input.
7	P3.4	I/O I/O	**P3.4**: User-configurable I/O Port 3 bit 4. **T0**: Timer/Counter 0 External Input or PWM Output.
8	P3.2	I/O I I/O	**P3.2**: User-configurable I/O Port 3 bit 2. **XTAL1**: Input to the inverting oscillator amplifier and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source. **DDA**: Serial Data input/output for On-Chip Debug Interface when OCD is enabled and the internal RC oscillator is selected as the clock source.
9	P3.3	I/O O O I/O	**P3.3**: User-configurable I/O Port 3 bit 3. **XTAL2**: Output from inverting oscillator amplifier. It may be used as a port pin if the internal RC oscillator is selected as the clock source. **CLKOUT**: When the internal RC oscillator is selected as the clock source, may be used to output the internal clock divided by 2. **DDA**: Serial Data input/output for On-Chip Debug Interface when OCD is enabled and the external clock is selected as the clock source.
10	P3.5	I/O I/O	**P3.5**: User-configurable I/O Port 3 bit 5. **T1**: Timer/Counter 1 External input or PWM output.
11	P3.1	I/O O	**P3.1**: User-configurable I/O Port 3 bit 1. **TXD**: Serial Port Transmitter Output.
12	VDD	I	Supply Voltage
13	P1.0	I/O I I	**P1.0**: User-configurable I/O Port 1 bit 0. **AIN0**: Analog Comparator Positive input. **GPI0**: General-purpose Interrupt input 0.
14	P1.1	I/O I I	**P1.1**: User-configurable I/O Port 1 bit 1. **AIN1**: Analog Comparator Negative input. **GPI1**: General-purpose Interrupt input 1
15	P1.4	I/O I I	**P1.4**: User-configurable I/O Port 1 bit 4. **$\overline{\text{SS}}$**: SPI slave select input. **GPI4**: General-purpose Interrupt input 4.
16	P1.6	I/O I/O I	**P1.6**: User-configurable I/O Port 1 bit 6. **MISO**: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output. **GPI6**: General-purpose Interrupt input 6.

4. Block Diagram

Figure 4-1. AT89LP216 Block Diagram



5. Comparison to Standard 8051

The AT89LP216 is part of a family of devices with enhanced features that are fully binary compatible with the MCS-51 instruction set. In addition, most SFR addresses, bit assignments, and pin alternate functions are identical to Atmel's existing standard 8051 products. However, due to the high performance nature of the device, some system behaviors are different from those of Atmel's standard 8051 products such as AT89S52 or AT89S2051. The differences from the standard 8051 are outlined in the following paragraphs.

5.1 System Clock

The CPU clock frequency equals the external XTAL1 frequency. The oscillator is no longer divided by 2 to provide the internal clock and x2 mode is not supported.

5.2 Instruction Execution with Single-cycle Fetch

The CPU fetches one code byte from memory every clock cycle instead of every six clock cycles. This greatly increases the throughput of the CPU. As a consequence, the CPU no longer executes instructions in 12 to 48 clock cycles. Each instruction executes in only 1 to 4 clock cycles. See “Instruction Set Summary” on page 59 for more details.

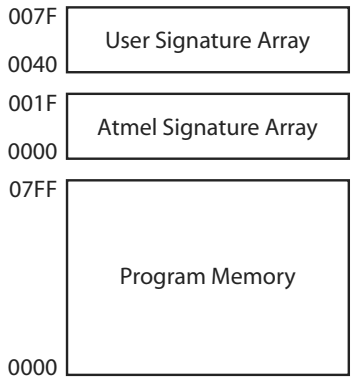
6. Memory Organization

The AT89LP216 uses a Harvard Architecture with separate address spaces for program and data memory. The program memory has a regular linear address space with support for up to 64K bytes of directly addressable application code. The data memory has 128 bytes of internal RAM and 128 bytes of Special Function Register I/O space. The AT89LP216 does not support external data memory or external program memory.

6.1 Program Memory

The AT89LP216 contains 2K bytes of on-chip In-System Programmable Flash memory for program storage. The Flash memory has an endurance of at least 10,000 write/erase cycles and a minimum data retention time of 10 years. The reset and interrupt vectors are located within the first 59 bytes of program memory (refer to Table 12-1 on page 19). Constant tables can be allocated within the entire 2K program memory address space for access by the MOVC instruction. The AT89LP216 does not support external program memory.

Figure 6-1. Program Memory Map



A map of the AT89LP216 program memory is shown in Figure 6-1. In addition to the 2K code space from 0000h to 07FFh, the AT89LP216 also supports a 64-byte User Signature Array and a 32-byte Atmel Signature Array that are accessible by the CPU in a read-only fashion. In order to read from the signature arrays, the SIGEN bit in AUXR1 must be set. While SIGEN is one, MOVC A,@A+DPTR will access the signature arrays. The User Signature Array is mapped to addresses 0040h to 007Fh and the Atmel Signature Array is mapped to addresses 0000h to 001Fh. SIGEN must be cleared before using MOVC to access the code memory.

The Atmel Signature Array is initialized with the Device ID in the factory. The User Signature Array is available for user identification codes or constant parameter data. Data stored in the signature array is not secure. Security bits will disable writes to the array; however, reads are always allowed.

Table 6-1. AUXR1 – Auxiliary Register 1

AUXR1 = A2H — Reset Value = XXXX 0XXXB

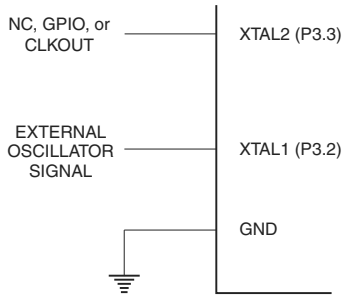
Not Bit Addressable

	–	–	–	–	SIGEN	–	–	–
Bit	7	6	5	4	3	2	1	0

9.2 External Clock Source

The external clock option disables the oscillator amplifier and allows XTAL1 to be driven directly by the clock source as shown in Figure 9-2. XTAL2 may be left unconnected, used as P3.3 I/O, or configured to output a divided version of the system clock.

Figure 9-2. External Clock Drive Configuration



9.3 Internal RC Oscillator

The AT89LP216 has an internal RC oscillator tuned to 8.0 MHz ±1.0% at 5.0V and 25· C. When enabled as the clock source, XTAL1 and XTAL2 may be used as P3.2 and P3.3, respectively. The XTAL2 may also be configured to output a divided version of the system clock. The frequency of the oscillator may be adjusted by changing the RC Adjust Fuses. (See “User Configuration Fuses” on page 71.) A copy of the initial factory setting is stored at location 0007h of the Atmel Signature.

9.4 System Clock Out

When the AT89LP216 is configured to use either an external clock or the internal RC oscillator, a divided version of the system clock may be output on XTAL2 (P3.3). The Clock Out feature is enabled by setting the COE bit in CLKREG. The two CDV bits determine the clock divide ratio. For example, setting COE = “1” and CDIV = “00” when using the internal oscillator will result in a 4.0 MHz clock output on P3.3. P3.3 must be configured as an output in order to use the clock out feature.

Table 9-2. CLKREG – Clock Control Register

CLKREG = 8FH — Reset Value = 0000 0000B

Not Bit Addressable

	TPS3	TPS2	TPS1	TPS0	–	CDV1	CDV0	COE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TPS3 TPS2 TPS1 TPS0	Timer Prescaler. The Timer Prescaler selects the time base for Timer 0, Timer 1 and the Watchdog Timer. The prescaler is implemented as a 4-bit binary down counter. When the counter reaches zero it is reloaded with the value stored in the TPS bits to give a division ratio between 1 and 16. By default the timers will count every clock cycles (TPS = 0000B). To configure the timers to count at a standard 8051 rate of once every 12 clock cycles, TPS should be set to 1011B.
CDV1 CDV0	Clock Out Division. Determines the frequency of the clock output relative to the system clock. CDIV1 CDIV0 Clock Out Frequency 0 0 f/2 0 1 f/4 1 0 f/8 1 1 f/16
COE	Clock Out Enable. Set COE to output a divided version of the system clock on XTAL2 (P3.3). The internal RC oscillator or external clock source must be selected in order to use this feature.

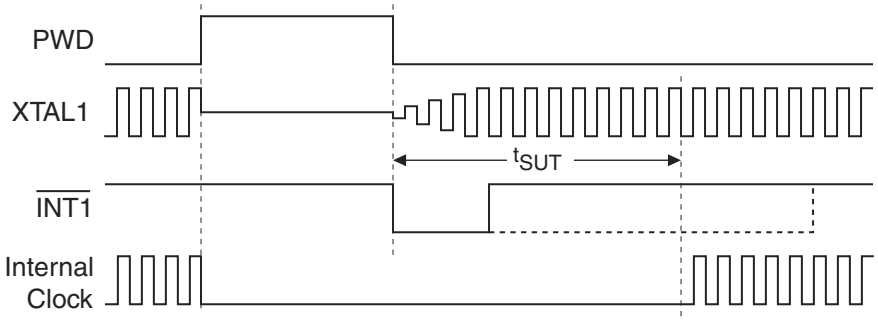
10. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tristated, and the program starts execution from the Reset Vector, 0000H. The AT89LP216 has five sources of reset: power-on reset, brown-out reset, external reset, watchdog reset, and software reset.

10.1 Power-on Reset

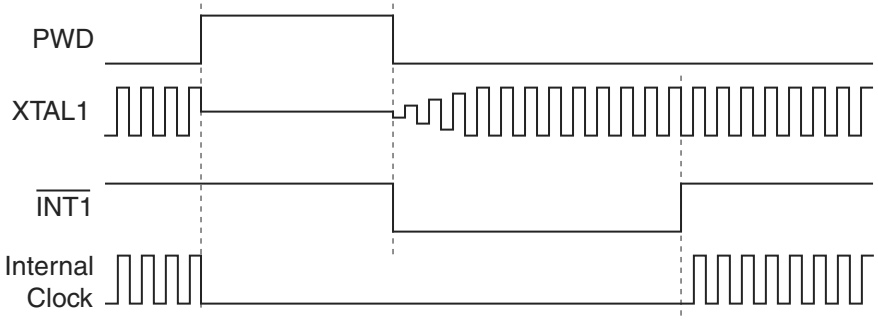
A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. A power-on sequence is shown in Figure 10-1. When V_{CC} reaches the Power-on Reset threshold voltage V_{POR}, an initialization sequence lasting t_{POR} is started. When the initialization sequence completes, the start-up timer determines how long the device is kept in POR after V_{CC} rise. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON. The internally generated reset can be extended beyond the power-on period by holding the $\overline{RST}$ pin low longer than the time-out.

Figure 11-1. Interrupt Recovery from Power-down (PWDEX = 0)



When PWDEX = “1”, the wake-up period is controlled externally by the interrupt. Again, at the falling edge on the interrupt pin, power-down is exited and the oscillator is restarted. However, the internal clock will not propagate until the rising edge of the interrupt pin as shown in Figure 11-2. The interrupt pin should be held low long enough for the selected clock source to stabilize. After the rising edge on the pin the interrupt service routine will be executed.

Figure 11-2. Interrupt Recovery from Power-down (PWDEX = 1)



11.2.2 Reset Recovery from Power-down

The wake-up from Power-down through an external reset is similar to the interrupt with PWDEX = “0”. At the falling edge of $\overline{RST}$, Power-down is exited, the oscillator is restarted, and an internal timer begins counting as shown in Figure 11-3. The internal clock will not be allowed to propagate to the CPU until after the timer has timed out. The time-out period is controlled by the Start-up Timer Fuses. (See Table 10-1 on page 15). If $\overline{RST}$ returns high before the time-out, a two clock cycle internal reset is generated when the internal clock restarts. Otherwise the device will remain in reset until $\overline{RST}$ is brought high.

Figure 11-3. Reset Recovery from Power-down.

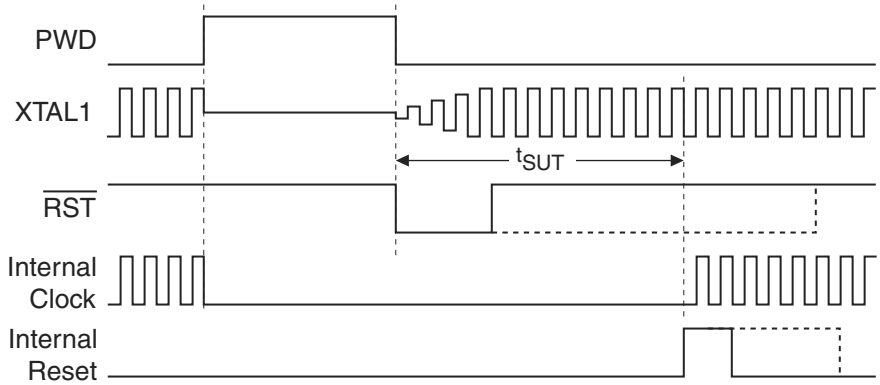


Table 14-2. TMOD: Timer/Counter Mode Control Register

TMOD = 89H — Reset Value = 0000 0000B

Not Bit Addressable

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
7	$\overline{6}$	5	4	3	$\overline{2}$	1	0
Timer1				**Timer0**			

Gate	Gating control when set. Timer/Counter x is enabled only while $\overline{INTx}$ pin is high and TRx control pin is set. When cleared, Timer x is enabled whenever TRx control bit is set.	Timer 0 gate bit
C/$\overline{T}$	Timer or Counter Selector cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).	Timer 0 counter/timer select bit
M1	Timer 1 Mode bit 1	Timer 0 M1 bit
M0	Timer 1 Mode bit 0	Timer 0 M0 bit

M1	M0	Mode	Operating Mode
0	0	0	Variable 9 - 16-bit Timer mode. 8-bit Timer/Counter THx with TLx as 1 - 8-bit prescaler.
0	1	1	16-bit auto-reload mode. 16-bit Timer/Counters THx and TLx are cascaded; there is no prescaler.
1	0	2	8-bit auto reload. 8-bit auto-reload Timer/Counter THx holds a value which is to be reloaded into TLx each time it overflows.
1	1	3	Split Timer mode. (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 stopped.

Timer SFR	Purpose	Address	Bit-Addressable
TCON	Control	88H	Yes
TMOD	Mode	89H	No
TL0	Timer 0 low-byte	8AH	No
TL1	Timer 1 low-byte	8BH	No
TH0	Timer 0 high-byte	8CH	No
TH1	Timer 1 high-byte	8DH	No
TCONB	Mode	91H	No
RL0	Timer 0 reload low-byte	92H	No
RL1	Timer 1 reload low-byte	93H	No
RH0	Timer 0 reload high-byte	94H	No
RH1	Timer 1 reload high-byte	95H	No

20. Analog Comparator

A single analog comparator is provided on the AT89LP216. The analog comparator has the following features:

- Comparator Output Flag and Interrupt
- Selectable Interrupt Condition
  - High- or Low-level
  - Rising- or Falling-edge
  - Output Toggle
- Hardware Debouncing Modes

Comparator operation is such that the output is a logic “1” when the positive input AIN0 (P1.0]) is greater than the negative input AIN1 (P1.1). Otherwise the output is a zero. Setting the CEN bit in ACSR enables the comparator. When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 µs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service. Before enabling the comparator the analog inputs should be tristated by putting P1.0 and P1.1 into input-only mode. See “Port 1 Analog Functions” on page 25.

The comparator may be configured to cause an interrupt under a variety of output value conditions by setting the CM bits in ACSR. The comparator interrupt flag CF in ACSR is set whenever the comparator output matches the condition specified by CM. The flag may be polled by software or may be used to generate an interrupt and must be cleared by software.

20.1 Comparator Interrupt with Debouncing

The comparator output is sampled every clock cycle. The conditions on the analog inputs may be such that the comparator output will toggle excessively. This is especially true if applying slow moving analog inputs. Three debouncing modes are provided to filter out this noise. In debouncing mode, the comparator uses Timer 1 to modulate its sampling time. When a relevant transition occurs, the comparator waits until two Timer 1 overflows have occurred before resampling the output. If the new sample agrees with the expected value, CF is set. Otherwise, the event is ignored. The filter may be tuned by adjusting the time-out period of Timer 1. Because Timer 1 is free running, the debouncer must wait for two overflows to guarantee that the sampling delay is at least 1 time-out period. Therefore, after the initial edge event, the interrupt may occur between 1 and 2 time-out periods later. See Figure 20-1 on page 56.

By default the comparator is disabled during Idle mode. To allow the comparator to function during Idle, the CIDL bit is ACSR must be set. When CIDL is set, the comparator can be used to wake-up the CPU from Idle if the comparator interrupt is enabled. The comparator is always disabled during Power-down mode.

- The $\overline{RST}$ input may be disabled to gain an extra I/O pin. In these cases the $\overline{RST}$ pin will always function as a reset during power up. To enter programming the $\overline{RST}$ pin must be driven low prior to the end of Power-On Reset (POR). After POR has completed the device will remain in ISP mode until $\overline{RST}$ is brought high. Once the initial ISP session has ended, the power to the target device must be cycled OFF and ON to enter another session.
- The $\overline{SS}$ pin should not be left floating during reset if ISP is enabled.
- The ISP Enable Fuse must be set to allow programming during any reset period. If the ISP Fuse is disabled, ISP may only be entered at POR.

24.2 Memory Organization

The AT89LP216 offers 2K bytes of In-System Programmable (ISP) nonvolatile Flash code memory. In addition, the device contains a 64-byte User Signature Array and a 32-byte read-only Atmel Signature Array. The memory organization is shown in Table 24-1 and Figure 24-2. The memory is divided into pages of 32 bytes each. A single read or write command may only access a single page in the memory. Each memory type resides in its own address space and is accessed by commands specific to that memory. However, all memory types share the same page size.

User configuration fuses are mapped as a row in the memory, with each byte representing one fuse. From a programming standpoint, fuses are treated the same as normal code bytes except they are not affected by Chip Erase. Fuses can be enabled at any time by writing 00h to the appropriate locations in the fuse row. However, to disable a fuse, i.e. set it to FFh, the **entire** fuse row must be erased and then reprogrammed. The programmer should read the state of all the fuses into a temporary location, modify those fuses which need to be disabled, then issue a Fuse Write with Auto-Erase command using the temporary data. Lock bits are treated in a similar manner to fuses except they may only be erased (unlocked) by Chip Erase.

Table 24-1. Code Memory Sizes

Device #	Code Size	Page Size	# Pages	Address Range
AT89LP216	2K bytes	32 bytes	64	0000H - 07FFH

Figure 24-2. AT89LP216 Memory Organization

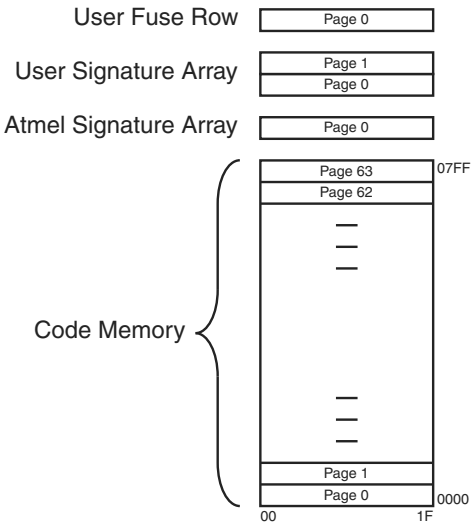


Table 24-2. Programming Command Summary

Command	Opcode	Addr High	Addr Low	Data 0	Data n
Program Enable[1]	1010 1100	0101 0011	–	–	–
Chip Erase	1000 1010	–	–	–	–
Read Status	0110 0000	xxxx xxxx	xxxx xxxx	Status Out	
Load Page Buffer[2]	0101 0001	xxxx xxxx	xxxb bbbb	DataIn 0 ... DataIn n	
Write Code Page[2]	0101 0000	xxxx xaaa	aaab bbbb	DataIn 0 ... DataIn n	
Write Code Page with Auto-Erase[2]	0111 0000	xxxx xaaa	aaab bbbb	DataIn 0 ... DataIn n	
Read Code Page[2]	0011 0000	xxxx xaaa	aaab bbbb	DataOut 0 ... DataOut n	
Write User Fuses[2][3][4]	1110 0001	0000 0000	000b bbbb	DataIn 0 ... DataIn n	
Write User Fuses with Auto-Erase[2][3][4]	1111 0001	0000 0000	000b bbbb	DataIn 0 ... DataIn n	
Read User Fuses[2][3][4]	0110 0001	0000 0000	000b bbbb	DataOut 0 ... DataOut n	
Write Lock Bits[2][3][5]	1110 0100	0000 0000	000b bbbb	DataIn 0 ... DataIn n	
Read Lock Bits[2][3][5]	0110 0100	0000 0000	000b bbbb	DataOut 0 ... DataOut n	
Write User Signature Page[2]	0101 0010	xxxx xxxx	xaab bbbb	DataIn 0 ... DataIn n	
Write User Signature Page with Auto-Erase[2]	0111 0010	xxxx xxxx	xaab bbbb	DataIn 0 ... DataIn n	
Read User Signature Page[2]	0011 0010	xxxx xxxx	xaab bbbb	DataOut 0 ... DataOut n	
Read Atmel Signature Page[2][6]	0011 1000	xxxx xxxx	xxxb bbbb	DataOut 0 ... DataOut n	

Notes:
1. Program Enable must be the **first** command issued after entering into programming mode.
2. Any number of Data bytes from 1 to 32 may be written/read. The internal address is incremented between each byte.
3. Each byte address selects one fuse or lock bit. Data bytes must be 00h or FFh.
4. See Table 24-5 on page 71 for Fuse definitions.
5. See Table 24-4 on page 70 for Lock Bit definitions.
6. **Atmel Signature Bytes**:

   AT89LP216: Address 00H = 1EH
   01H = 29H
   02H = FFH

7. **Symbol Key**:

   a: Page Address Bit
   b: Byte Address Bit
   x: Don't Care Bit

24.4 Status Register

The current state of the memory may be accessed by reading the status register. The status register is shown in Table 24-3.

Table 24-3. Status Register

	–	–	–	–	LOAD	SUCCESS	WRTINH	BUSY
Bit	7	6	5	4	3	2	1	0

Symbol	Function
LOAD	Load flag. Cleared low by the load page buffer command and set high by the next memory write. This flag signals that the page buffer was previously loaded with data by the load page buffer command.
SUCCESS	Success flag. Cleared low at the start of a programming cycle and will only be set high if the programming cycle completes without interruption from the brownout detector.
WRTINH	Write Inhibit flag. Cleared low by the brownout detector (BOD) whenever programming is inhibited due to V_{CC} falling below the minimum required programming voltage. If a BOD episode occurs during programming, the SUCCESS flag will remain low after the cycle is complete. $\overline{\text{WRTINH}}$ low also forces $\overline{\text{BUSY}}$ low.
BUSY	Busy flag. Cleared low whenever the memory is busy programming or if write is currently inhibited.

24.5 $\overline{\text{DATA}}$ Polling

The AT89LP216 implements $\overline{\text{DATA}}$ polling to indicate the end of a programming cycle. While the device is busy, any attempted read of the last byte written will return the data byte with the MSB complemented. Once the programming cycle has completed, the true value will be accessible. During Erase the data is assumed to be FFH and $\overline{\text{DATA}}$ polling will return 7FH. When writing multiple bytes in a page, the $\overline{\text{DATA}}$ value will be the last data byte loaded before programming begins, not the written byte with the highest physical address within the page.

24.6 Flash Security

The AT89LP216 provides two Lock Bits for Flash Code Memory security. Lock bits can be left unprogrammed (FFh) or programmed (00h) to obtain the protection levels listed in Table 24-4. Lock bits can only be erased (set to FFh) by Chip Erase. Lock bit mode 2 disables programming of all memory spaces, including the User Signature Array and User Configuration Fuses. User fuses must be programmed before enabling Lock bit mode 2 or 3. Lock bit mode 3 implemented mode 2 and also blocks reads from the code memory; however, reads of the User Signature Array, Atmel Signature Array, and User Configuration Fuses are still allowed.

Table 24-4. Lock Bit Protection Modes

Program Lock Bits (by address)			
Mode	**00h**	**01h**	**Protection Mode**
1	FFh	FFh	No program lock features
2	00h	FFh	Further programming of the Flash is disabled
3	00h	00h	Further programming of the Flash is disabled and verify (read) is also disabled; OCD is disabled

24.7 User Configuration Fuses

The AT89LP216 includes 19 user fuses for configuration of the device. Each fuse is accessed at a separate address in the User Fuse Row as listed in Table 24-5. Fuses are cleared by programming 00h to their locations. Programming FFh to fuse location will cause that fuse to maintain its previous state. To set a fuse (set to FFh) the fuse row must be erased and then reprogrammed using the Fuse Write with Auto-erase command. The default state for all fuses is FFh.

Table 24-5. User Configuration Fuse Definitions

Address	Fuse Name	Description
00 – 01h	Clock Source – CS[0:1](2)	Selects source for the system clock: CS1 CS0 Selected Source 00h 00h Crystal Oscillator (XTAL) 00h FFh Reserved FFh 00h External Clock on XTAL1 (XCLK) FFh FFh Internal RC Oscillator (IRC)
02 – 03h	Start-up Time – SUT[0:1]	Selects time-out delay for the POR/BOD/PWD wake-up period: SUT1 SUT0 Selected Time-out 00h 00h 1 ms (XTAL); 16 µs (XCLK/IRC) 00h FFh 2 ms (XTAL); 512 µs (XCLK/IRC) FFh 00h 4 ms (XTAL); 1 ms (XCLK/IRC) FFh FFh 16 ms (XTAL); 4 ms (XCLK/IRC)
04h	Reset Pin Enable(3)	FFh: $\overline{\text{RST}}$ pin functions as reset 00h: $\overline{\text{RST}}$ pin functions as general purpose I/O
05h	Brown-out Detector Enable	FFh: Brown-out Detector Enabled 00h: Brown-out Detector Disabled
06h	On-chip Debug $\overline{\text{Enable}}$	FFh: On-chip Debug Disabled 00h: On-chip Debug Enabled
07h	ISP Enable(3)	FFh: In-System Programming Enabled 00h: In-System Programming Disabled (Enabled at POR only)
08 – 0FH	RC Oscillator Frequency Adjustment [0:7]	Adjusts the frequency of the internal RC oscillator. A copy of the 8MHz factory setting is stored at location 0008h of the Atmel Signature.
10H	User Signature Programming	FFh: Programming of User Signature Disabled 00h: Programming of User Signature Enabled
11H	Tristate Ports(4)	FFh: I/O Ports start in input-only mode (tristated) after reset 00h: I/O Ports start in quasi-bidirectional mode after reset
12H	OCD Interface Select	FFh: Fast two-wire interface 00h: Do not use

Notes:
1. The default state for all fuses is FFh.
2. Changes to these fuses will only take effect after a device POR.
3. Changes to these fuses will only take effect after the ISP session terminates by bringing $\overline{\text{RST}}$ high.
4. AIN0 (P1.0) and AIN1 (P1.1) always reset to input-only mode. $\overline{\text{SS}}$ (P1.4) always resets to quasi-bidirectional mode.

25. Electrical Characteristics

25.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +5.5V
Maximum Operating Voltage	5.5V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

25.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.4V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.3 V_{CC}	V
V_{IH}	Input High-voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1, 3)	I_{OL} = 10 mA, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3) With Weak Pull-ups Enabled	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.7 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Ports 1, 3) With Strong Pull-ups Enabled(2)	I_{OH} = -2 mA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -500 µA, V_{CC} = 5V ±10%	0.6 V_{CC}		V
		I_{OH} = -100 µA	0.6 V_{CC}		V
I_{IL}	Logic 0 Input Current (Quasi-Bidirectional Mode)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logic 1 to 0 Transition Current (Quasi-Bidirectional Mode)	V_{IN} = 2V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input Leakage Current (Input-Only Mode)	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-up Resistor		50	150	kΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5V/3V		10/6	mA
		Idle Mode, 12 MHz, V_{CC} = 5./3V		3/1.5	mA
	Power-down Mode(3)	V_{CC} = 5V, P1.0 & P1.1 = 0V or V_{CC}		5	µA
		V_{CC} = 3V, P1.0 & P1.1 = 0V or V_{CC}		2	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 15 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. V_{OH1} levels are listed for DC operation. Under AC conditions a boost circuit provides additional source current.
3. Minimum V_{CC} for Power-down is 2V.

25.3.6 Crystal Oscillator

Figure 25-10. Quartz Crystal Input at 5V

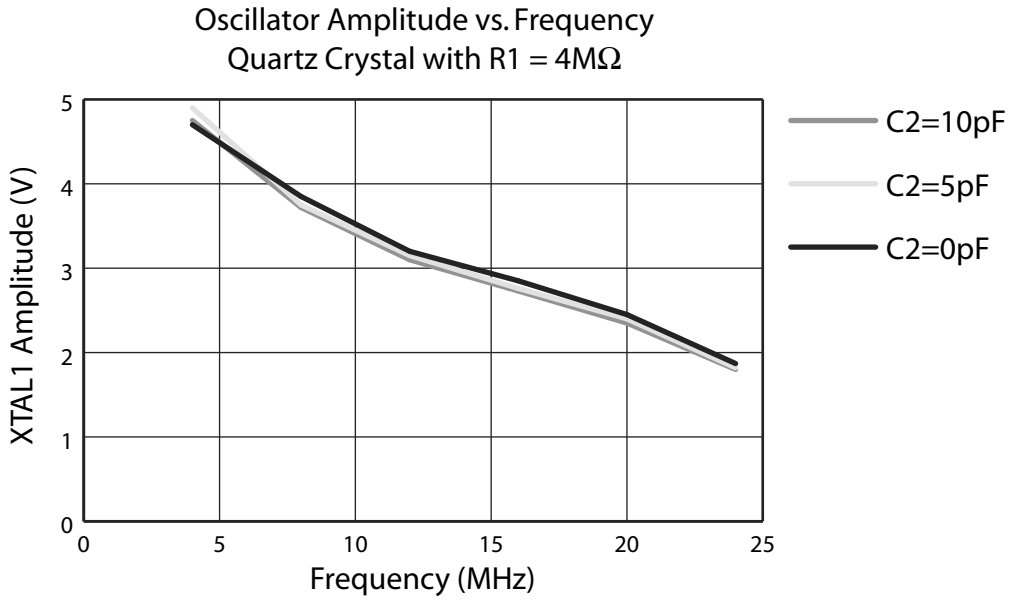


Figure 25-11. Ceramic Resonator Input at 5V

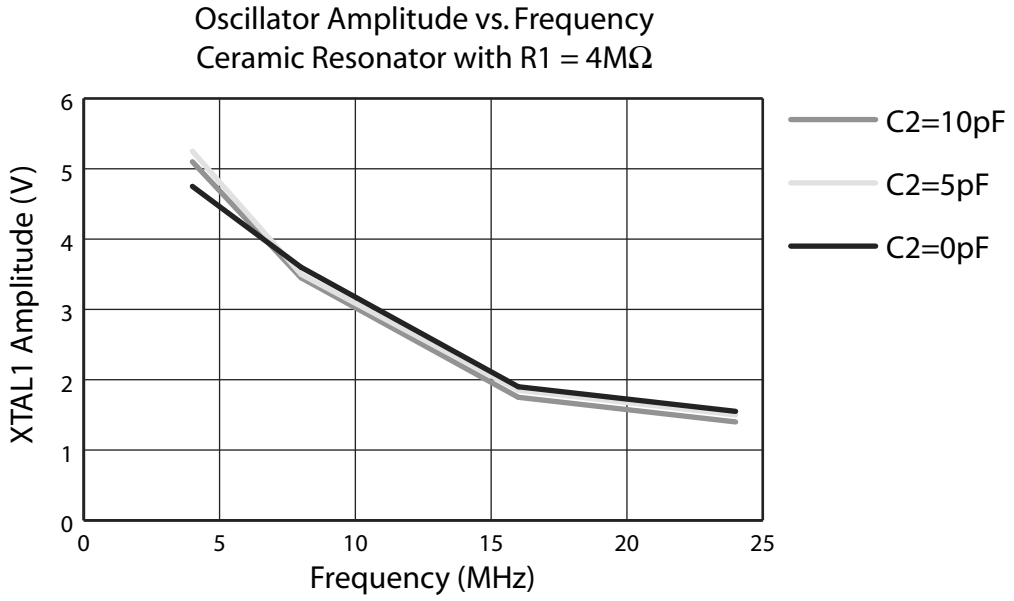


Figure 25-15. SPI Master Timing (CPHA = 1)

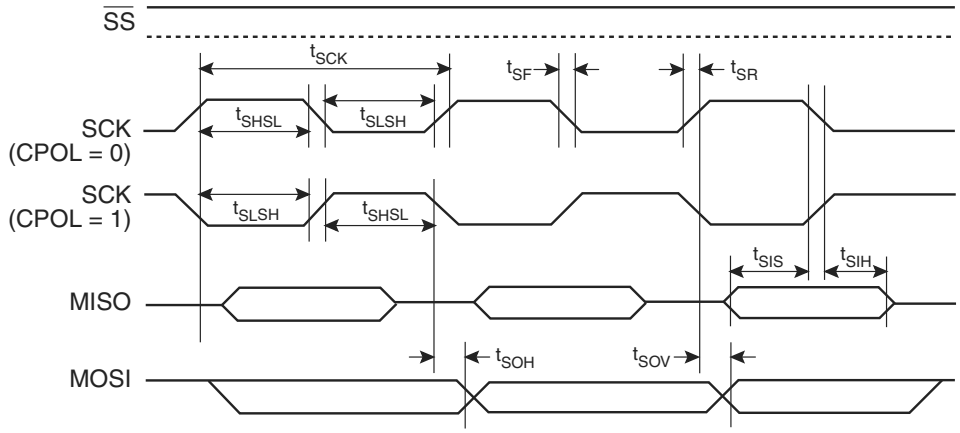
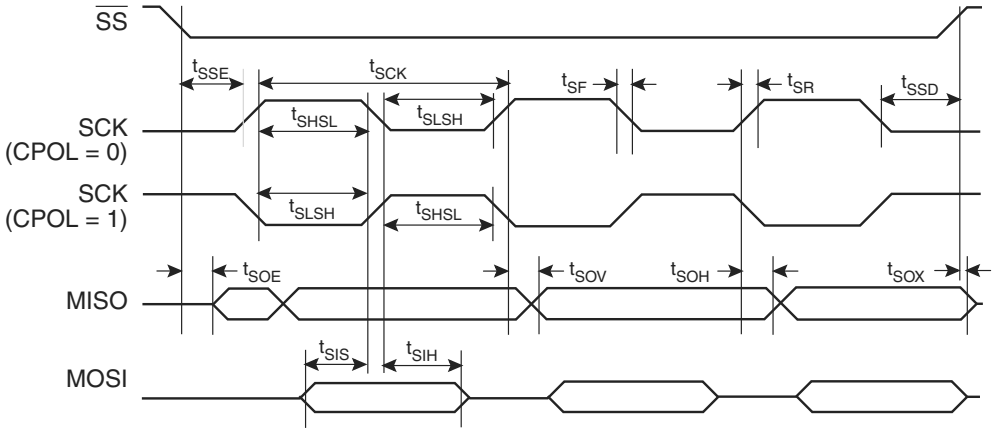


Figure 25-16. SPI Slave Timing (CPHA = 1)

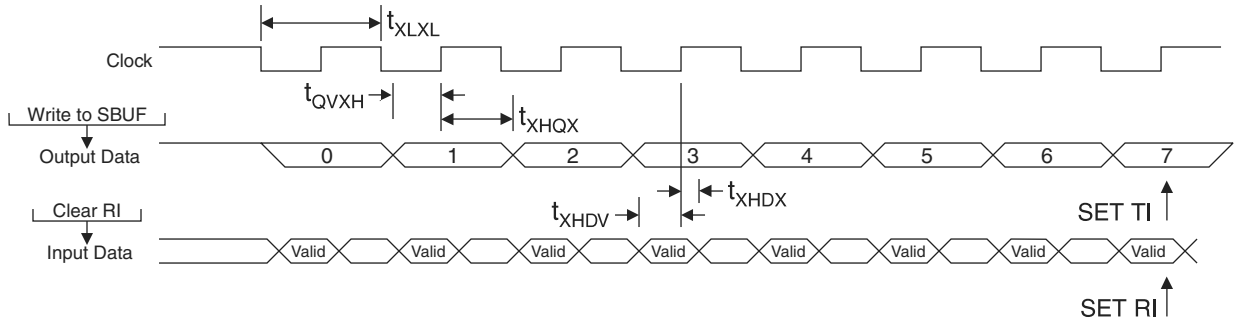


25.6 Serial Port Timing: Shift Register Mode Test Conditions

The values in this table are valid for V_{CC} = 2.4V to 5.5V and Load Capacitance = 80 pF.

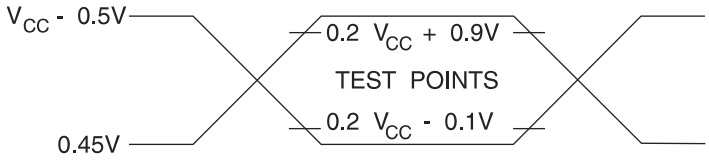
Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$2t_{CLCL}$ -15		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	t_{CLCL} -15		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	t_{CLCL} -15		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Input Data Valid to Clock Rising Edge	15		ns

Figure 25-17. Shift Register Mode Timing Waveform



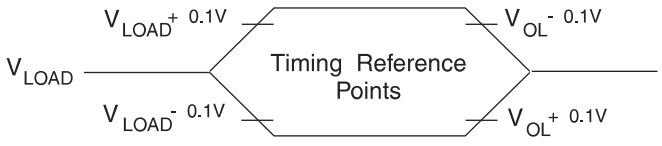
25.7 Test Conditions

25.7.1 AC Testing Input/Output Waveform(1)



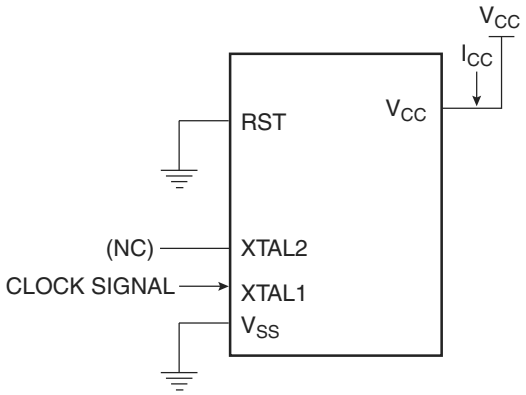
Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic “1” and 0.45V for a logic “0”. Timing measurements are made at V_{IH} min. for a logic “1” and V_{IL} max. for a logic “0”.

25.7.2 Float Waveform(1)

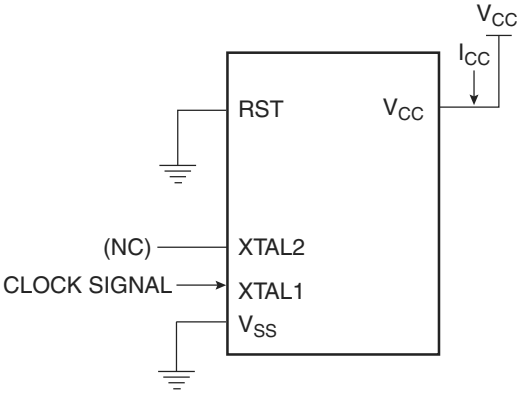


Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

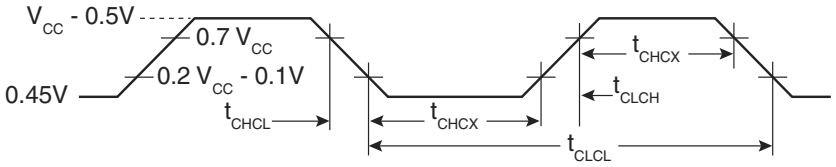
25.7.3 I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected



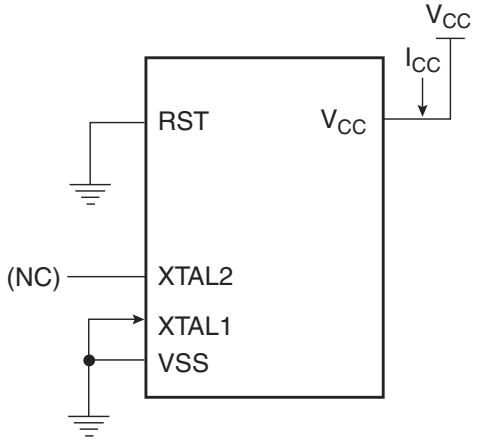
25.7.4 I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



25.7.5 Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns

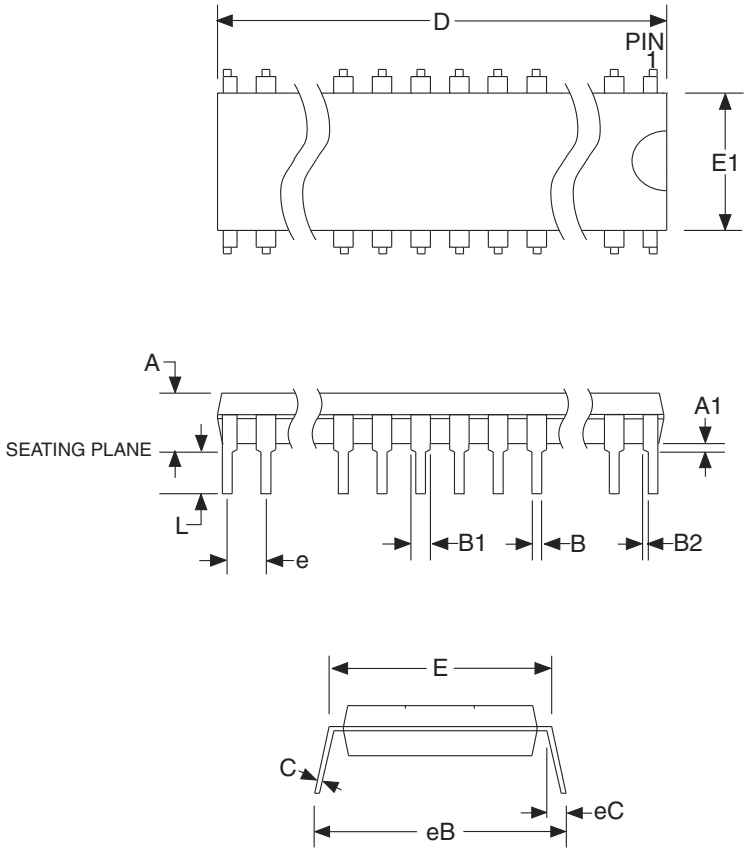


25.7.6 I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{CC} = 2V to 5.5V



27. Packaging Information

27.1 16P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	19.81	–	20.32	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.143	–	1.778	
B2	0.762	–	1.143	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AB.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/02/05

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**16P3**, 16-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	16P3	A

28. Revision History

Revision No.	History
Revision A – July 2006	• Initial Preliminary Release
Revision B – Nov. 2007	• Removed “Preliminary” status from the datasheet.
Revision C – June 2008	• Added oscillator connection diagram, Figure 9-1 on page 11 • Added external clock connection diagram, Figure 9-2 on page 12 • Added PWM Mode 2 waveform, Figure 14-9 on page 34 • Updated SPI connection diagram, Figure 19-1 on page 50 • Add note for Tristate Ports Fuse on page 71 • Updated definition for OCD Interface Fuse on page 71 • Updated DC Parameters on page 76 • Added typical power consumption characteristics on page 77 • Added typical frequency characteristics on page 79 • Added typical I/O characteristics on page 80 • Updated Clock Parameters on page 83 • Removed Standard Packaging Offering
Revision D – Oct. 2009	• Replaced C1 with R1 in oscillator diagram Figure 9-1 on page 11. • Added oscillator input characteristics on page 82.
Revision E – Nov. 2010	• Noted output levels as TTL. See Section 13. on page 22.

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