Welcome to E-XFL.COM
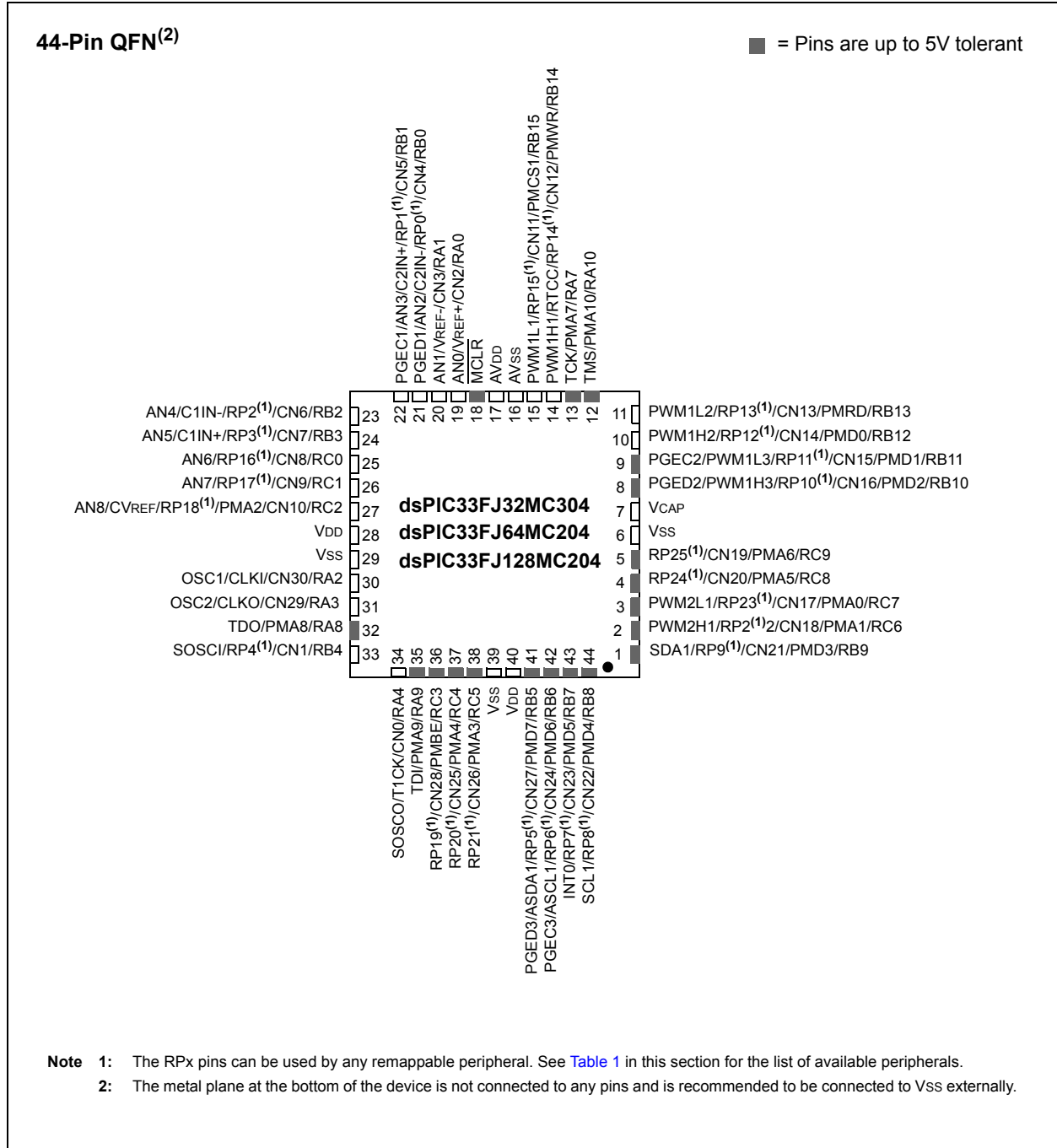
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128mc802-e-sp

Pin Diagrams (Continued)

44-Pin QFN[2]

■ = Pins are up to 5V tolerant

Top pins (left to right, 22–12):
- 22: PGEC1/AN3/C2IN+/RP1[1]/CN5/RB1
- 21: PGED1/AN2/C2IN-/RP0[1]/CN4/RB0
- 20: AN1/VREF-/CN3/RA1
- 19: AN0/VREF+/CN2/RA0
- 18: MCLR
- 17: AVDD
- 16: AVSS
- 15: PWM1L1/RP15[1]/CN11/PMCS1/RB15
- 14: PWM1H1/RTCC/RP14[1]/CN12/PMWR/RB14
- 13: TCK/PMA7/RA7
- 12: TMS/PMA10/RA10

Left pins (23–33):
- 23: AN4/C1IN-/RP2[1]/CN6/RB2
- 24: AN5/C1IN+/RP3[1]/CN7/RB3
- 25: AN6/RP16[1]/CN8/RC0
- 26: AN7/RP17[1]/CN9/RC1
- 27: AN8/CVREF/RP18[1]/PMA2/CN10/RC2
- 28: VDD
- 29: VSS
- 30: OSC1/CLKI/CN30/RA2
- 31: OSC2/CLKO/CN29/RA3
- 32: TDO/PMA8/RA8
- 33: SOSCI/RP4[1]/CN1/RB4

dsPIC33FJ32MC304
dsPIC33FJ64MC204
dsPIC33FJ128MC204

Right pins (11–1):
- 11: PWM1L2/RP13[1]/CN13/PMRD/RB13
- 10: PWM1H2/RP12[1]/CN14/PMD0/RB12
- 9: PGEC2/PWM1L3/RP11[1]/CN15/PMD1/RB11
- 8: PGED2/PWM1H3/RP10[1]/CN16/PMD2/RB10
- 7: VCAP
- 6: VSS
- 5: RP25[1]/CN19/PMA6/RC9
- 4: RP24[1]/CN20/PMA5/RC8
- 3: PWM2L1/RP23[1]/CN17/PMA0/RC7
- 2: PWM2H1/RP2[1]2/CN18/PMA1/RC6
- 1: SDA1/RP9[1]/CN21/PMD3/RB9

Bottom pins (34–44):
- 34: SOSCO/T1CK/CN0/RA4
- 35: TDI/PMA9/RA9
- 36: RP19[1]/CN28/PMBE/RC3
- 37: RP20[1]/CN25/PMA4/RC4
- 38: RP21[1]/CN26/PMA3/RC5
- 39: VSS
- 40: VDD
- 41: PGED3/ASDA1/RP5[1]/CN27/PMD7/RB5
- 42: PGEC3/ASCL1/RP6[1]/CN24/PMD6/RB6
- 43: INT0/RP7[1]/CN23/PMD5/RB7
- 44: SCL1/RP8[1]/CN22/PMD4/RB8

Note 1: The RPx pins can be used by any remappable peripheral. See Table 1 in this section for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

3.5   CPU Resources

Many useful resources related to the CPU are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:**   In the event you are not able to access the product page using the link above, enter this URL in your browser:
> http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en532315

3.5.1   KEY RESOURCES

- **Section 2. "CPU"** (DS70204)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 3-2:   CORCON: CORE CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R-0	R-0	R-0
—	—	—	US	EDT[1]	DL<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3[2]	PSV	RND	IF
bit 7							bit 0

Legend:			
	C = Clear only bit		
R = Readable bit	W = Writable bit	-n = Value at POR	'1' = Bit is set
'0' = Bit is cleared	'x' = Bit is unknown	U = Unimplemented bit, read as '0'	

bit 15-13   **Unimplemented:** Read as '0'

bit 12   **US:** DSP Multiply Unsigned/Signed Control bit

1 = DSP engine multiplies are unsigned
0 = DSP engine multiplies are signed

bit 11   **EDT:** Early DO Loop Termination Control bit[1]

1 = Terminate executing DO loop at end of current loop iteration
0 = No effect

bit 10-8   **DL<2:0>:** DO Loop Nesting Level Status bits

111 = 7 DO loops active
•
•
•
001 = 1 DO loop active
000 = 0 DO loops active

bit 7   **SATA:** ACCA Saturation Enable bit

1 = Accumulator A saturation enabled
0 = Accumulator A saturation disabled

bit 6   **SATB:** ACCB Saturation Enable bit

1 = Accumulator B saturation enabled
0 = Accumulator B saturation disabled

bit 5   **SATDW:** Data Space Write from DSP Engine Saturation Enable bit

1 = Data space write saturation enabled
0 = Data space write saturation disabled

bit 4   **ACCSAT:** Accumulator Saturation Mode Select bit

1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3   **IPL3:** CPU Interrupt Priority Level Status bit 3[2]

1 = CPU interrupt priority level is greater than 7
0 = CPU interrupt priority level is 7 or less

bit 2   **PSV:** Program Space Visibility in Data Space Enable bit

1 = Program space visible in data space
0 = Program space not visible in data space

Note 1:   This bit is always read as '0'.
    2:   The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU interrupt priority level.

TABLE 4-1: CPU CORE REGISTERS MAP (CONTINUED)

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
MODCON	0046	XMODEN	YMODEN	—	—	BWM<3:0>				YWM<3:0>				XWM<3:0>				0000
XMODSRT	0048	XS<15:1>															0	xxxx
XMODEND	004A	XE<15:1>															1	xxxx
YMODSRT	004C	YS<15:1>															0	xxxx
YMODEND	004E	YE<15:1>															1	xxxx
XBREV	0050	BREN	XB<14:0>															xxxx
DISICNT	0052	—	—	Disable Interrupts Counter Register														xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-8:   IFS3: INTERRUPT FLAG STATUS REGISTER 3

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0
FLTA1IF	RTCIF	DMA5IF	—	—	QEI1IF	PWM1IF	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **FLTA1IF:** PWM1 Fault A Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 14   **RTCIF:** Real-Time Clock and Calendar Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13   **DMA5IF:** DMA Channel 5 Data Transfer Complete Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-11   **Unimplemented:** Read as '0'

bit 10   **QEI1IF:** QEI1 Event Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9   **PWM1IF:** PWM1 Event Interrupt Flag Status bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8-0   **Unimplemented:** Read as '0'

11.6.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. The dsPIC33F devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

11.6.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers;
clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) the IOLOCK bit as a single operation.

> **Note:** MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:
>
> ```
> __builtin_write_OSCCONL(value)
> __builtin_write_OSCCONH(value)
> ```
>
> See MPLAB IDE Help for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the peripheral pin selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

11.6.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset is triggered.

11.6.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY Configuration bit (FOSC<5>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the peripheral pin select registers.

REGISTER 11-13: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INDX2R<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **INDX2R<4:0>:** Assign QEI2 INDEX (INDX2) to the corresponding RPn pin
11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

REGISTER 18-3:   SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	FRMDLY	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15   **FRMEN:** Framed SPIx Support bit

   1 = Framed SPIx support enabled ($\overline{\text{SSx}}$ pin used as frame sync pulse input/output)
   0 = Framed SPIx support disabled

bit 14   **SPIFSD:** Frame Sync Pulse Direction Control bit

   1 = Frame sync pulse input (slave)
   0 = Frame sync pulse output (master)

bit 13   **FRMPOL:** Frame Sync Pulse Polarity bit

   1 = Frame sync pulse is active-high
   0 = Frame sync pulse is active-low

bit 12-2   **Unimplemented:** Read as '0'

bit 1   **FRMDLY:** Frame Sync Pulse Edge Select bit

   1 = Frame sync pulse coincides with first bit clock
   0 = Frame sync pulse precedes first bit clock

bit 0   **Unimplemented:** This bit must not be set to '1' by the user application

19.2   I^{2}C Resources

Many useful resources related to I^{2}C are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
> http://www.microchip.com/wwwprod-ucts/Devices.aspx?dDoc-Name=en532315

19.2.1   KEY RESOURCES

- **Section 19. "Inter-Integrated Circuit™ (I^{2}C™)" (DS70195)**
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

19.3   I^{2}C Registers

The I2CxCON and I2CxSTAT are control and status registers, respectively. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CxSTAT are read/write:

- I2CxRSR is the shift register used for shifting data internal to the module and the user application has no access to it
- I2CxRCV is the receive buffer and the register to which data bytes are written, or from which data bytes are read
- I2CxTRN is the transmit register to which bytes are written during a transmit operation
- The I2CxADD register holds the slave address
- A status bit, ADD10, indicates 10-bit Address mode
- The I2CxBRG acts as the Baud Rate Generator (BRG) reload value

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV, and an interrupt pulse is generated.

REGISTER 19-3:   I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK9	AMSK8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10   **Unimplemented:** Read as '0'

bit 9-0   **AMSKx:** Mask for Address bit x Select bit

1 = Enable masking for bit x of incoming message address; bit match not required in this position
0 = Disable masking for bit x; bit match required in this position

REGISTER 21-4:   CiFCTRL: ECAN™ FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS<2:0>			—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13   **DMABS<2:0>:** DMA Buffer Size bits

111 = Reserved
110 = 32 buffers in DMA RAM
101 = 24 buffers in DMA RAM
100 = 16 buffers in DMA RAM
011 = 12 buffers in DMA RAM
010 = 8 buffers in DMA RAM
001 = 6 buffers in DMA RAM
000 = 4 buffers in DMA RAM

bit 12-5   **Unimplemented:** Read as '0'

bit 4-0   **FSA<4:0>:** FIFO Area Starts with Buffer bits

11111 = Read buffer RB31
11110 = Read buffer RB30
•
•
•
00001 = TX/RX buffer TRB1
00000 = TX/RX buffer TRB0

REGISTER 21-7: CiINTE: ECAN™ INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'

bit 7   **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

bit 6   **WAKIE:** Bus Wake-up Activity Interrupt Flag bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

bit 5   **ERRIE:** Error Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

bit 4   **Unimplemented:** Read as '0'

bit 3   **FIFOIE:** FIFO Almost Full Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

bit 2   **RBOVIE:** RX Buffer Overflow Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

bit 1   **RBIE:** RX Buffer Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

bit 0   **TBIE:** TX Buffer Interrupt Enable bit
1 = Interrupt Request Enabled
0 = Interrupt Request not enabled

23.4 DAC CLOCK

The DAC clock signal clocks the internal logic of the Audio DAC module. The data sample rate of the Audio DAC is an integer division of the rate of the DAC clock. The DAC clock is generated via a clock divider circuit that accepts an auxiliary clock from the auxiliary oscillator. The divisor ratio is programmed by clock divider bits (DACFDIV<6:0>) in the DAC Control register (DAC1CON). The resulting DAC clock must not exceed 25.6 MHz. If lower sample rates are to be used, then the DAC filter clock frequency may be reduced to reduce power consumption. The DAC clock frequency is 256 times the sampling frequency.

FIGURE 23-1: **BLOCK DIAGRAM OF AUDIO DIGITAL-TO-ANALOG CONVERTER (DAC)**

Note 1: If DAC1RDAT and DAC1LDAT are empty, data will be taken from the DACDFLT register.
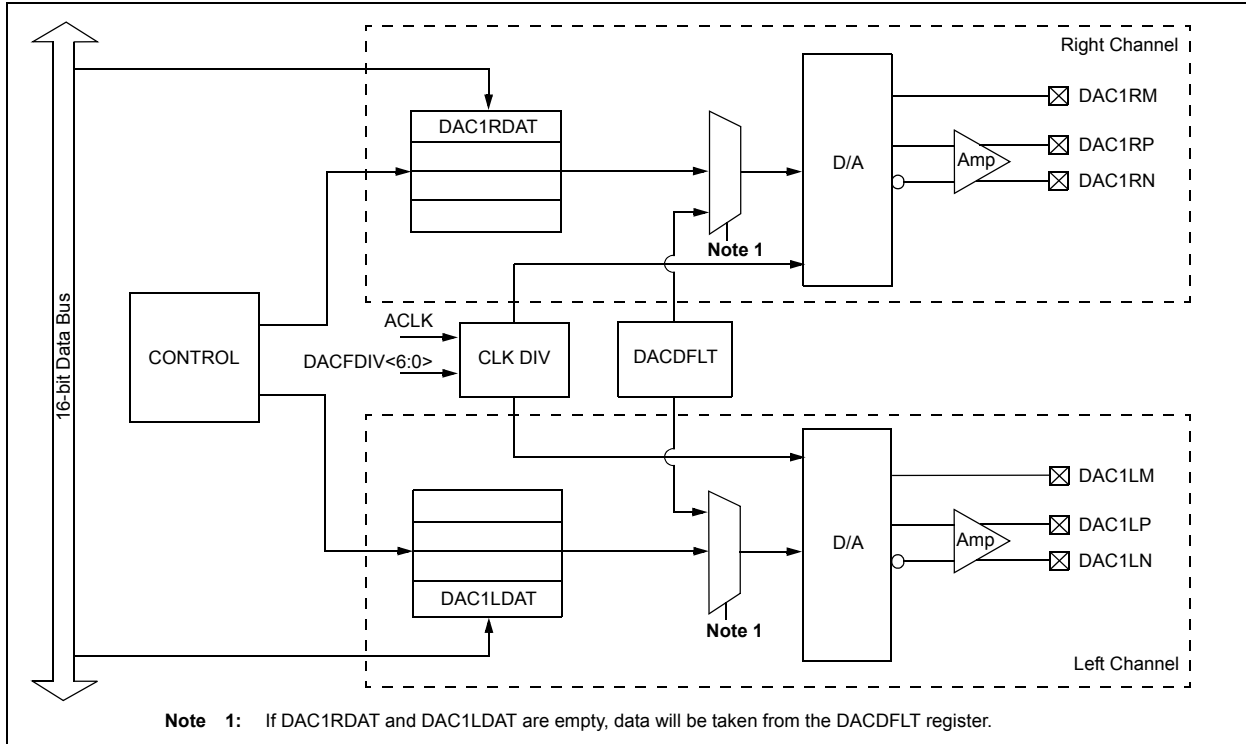
FIGURE 23-2: **AUDIO DAC OUTPUT FOR RAMP INPUT (UNSIGNED)**

Note: $V_{OD}+ = V_{DACH} - V_{DACL}$, $V_{OD}- = V_{DACL} - V_{DACH}$; refer to Audio DAC Module Specifications, Table 31-48, for typical values.
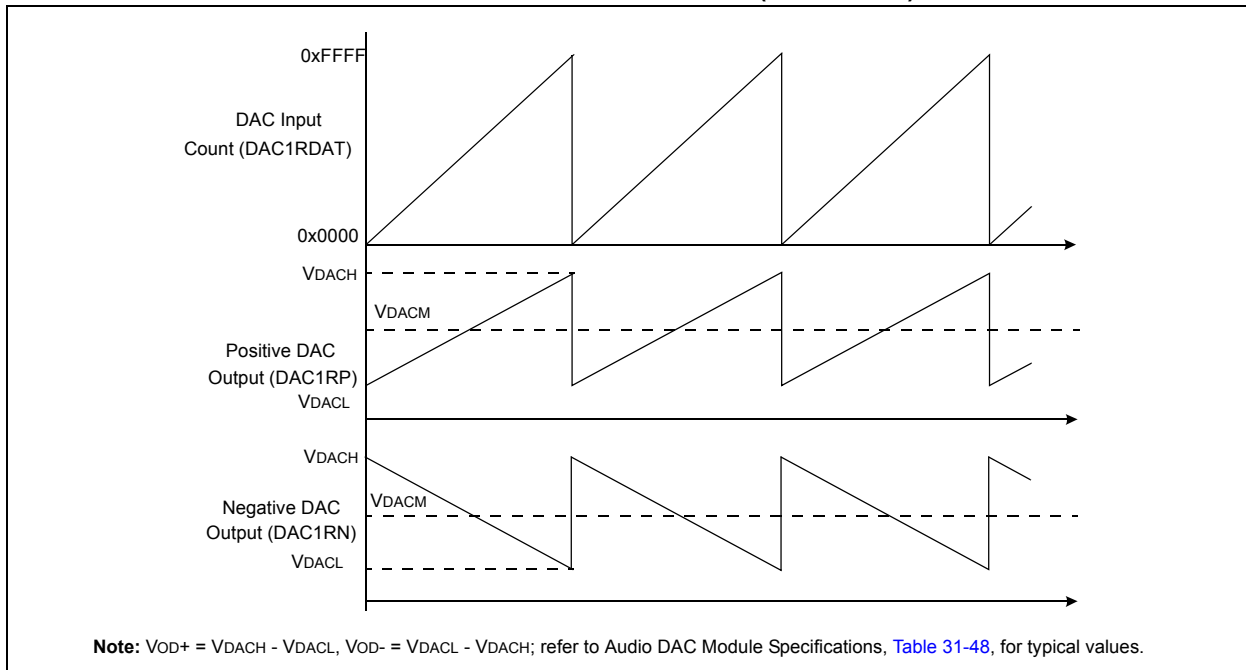
REGISTER 24-2: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR	CVRSS	CVR<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit

1 = CVREF circuit powered on
0 = CVREF circuit powered down

bit 6 **CVROE:** Comparator VREF Output Enable bit

1 = CVREF voltage level is output on CVREF pin
0 = CVREF voltage level is disconnected from CVREF pin

bit 5 **CVRR:** Comparator VREF Range Selection bit

1 = CVRSRC range should be 0 to 0.625 CVRSRC with CVRSRC/24 step size
0 = CVRSRC range should be 0.25 to 0.719 CVRSRC with CVRSRC/32 step size

bit 4 **CVRSS:** Comparator VREF Source Selection bit

1 = Comparator reference source CVRSRC = VREF+ – VREF-
0 = Comparator reference source CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>:** Comparator VREF Value Selection $0 \leq CVR<3:0> \leq 15$ bits

When CVRR = 1:
$CV_{REF} = (CVR<3:0>/\ 24) \bullet (CV_{RSRC})$

When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (CVR<3:0>/32) \bullet (CV_{RSRC})$

FIGURE 26-2: **CRC GENERATOR RECONFIGURED FOR $x^{16} + x^{12} + x^5 + 1$**
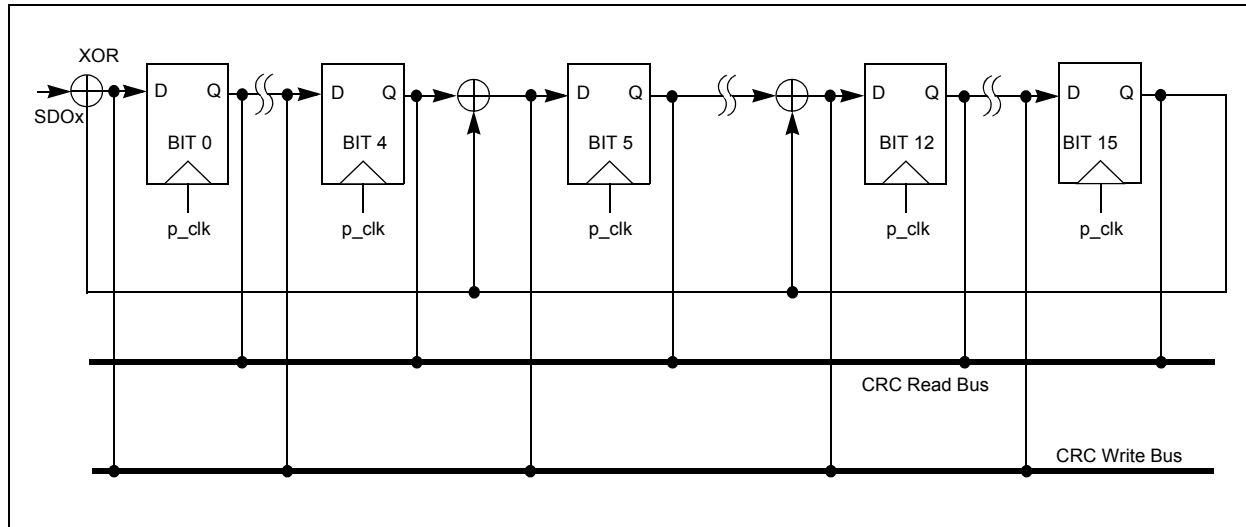
26.2 User Interface

26.2.1 DATA INTERFACE

To start serial shifting, a '1' must be written to the CRCGO bit.

The module incorporates a FIFO that is 8 deep when PLEN (PLEN<3:0>) > 7, and 16 deep, otherwise. The data for which the CRC is to be calculated must first be written into the FIFO. The smallest data element that can be written into the FIFO is one byte. For example, if PLEN = 5, then the size of the data is PLEN + 1 = 6. The data must be written as follows:

```
data[5:0] = crc_input[5:0]
data[7:6] = 'bxx
```

Once data is written into the CRCWDAT MSb (as defined by PLEN), the value of VWORD (VWORD<4:0>) increments by one. The serial shifter starts shifting data into the CRC engine when CRCGO = 1 and VWORD > 0. When the MSb is shifted out, VWORD decrements by one. The serial shifter continues shifting until the VWORD reaches 0. Therefore, for a given value of PLEN, it will take (PLEN + 1) * VWORD number of clock cycles to complete the CRC calculations.

When VWORD reaches 8 (or 16), the CRCFUL bit will be set. When VWORD reaches 0, the CRCMPT bit will be set.

To continually feed data into the CRC engine, the recommended mode of operation is to initially "prime" the FIFO with a sufficient number of words so no interrupt is generated before the next word can be written. Once that is done, start the CRC by setting the CRCGO bit to '1'. From that point onward, the VWORD bits should be polled. If they read less than 8 or 16, another word can be written into the FIFO.

To empty words already written into a FIFO, the CRCGO bit must be set to '1' and the CRC shifter allowed to run until the CRCMPT bit is set.

Also, to get the correct CRC reading, it will be necessary to wait for the CRCMPT bit to go high before reading the CRCWDAT register.

If a word is written when the CRCFUL bit is set, the VWORD Pointer will roll over to 0. The hardware will then behave as if the FIFO is empty. However, the condition to generate an interrupt will not be met; therefore, no interrupt will be generated (See **Section 26.2.2 "Interrupt Operation"**).

At least one instruction cycle must pass after a write to CRCWDAT before a read of the VWORD bits is done.

26.2.2 INTERRUPT OPERATION

When the VWORD4:VWORD0 bits make a transition from a value of '1' to '0', an interrupt will be generated.

26.3 Operation in Power-Saving Modes

26.3.1 SLEEP MODE

If Sleep mode is entered while the module is operating, the module will be suspended in its current state until clock execution resumes.

26.3.2 IDLE MODE

To continue full module operation in Idle mode, the CSIDL bit must be cleared prior to entry into the mode.

If CSIDL = 1, the module will behave the same way as it does in Sleep mode; pending interrupt events will be passed on, even though the module clocks are not available.

TABLE 28-3:   CODE FLASH SECURITY SEGMENT SIZES FOR 32 KB DEVICES

CONFIG BITS	BSS<2:0> = x11 0K	BSS<2:0> = x10 1K	BSS<2:0> = x01 4K	BSS<2:0> = x00 8K
SSS<2:0> = x11 0K	VS = 256 IW GS = 11008 IW	VS = 256 IW BS = 768 IW GS = 10240 IW	VS = 256 IW BS = 3840 IW GS = 7168 IW	VS = 256 IW BS = 7936 IW GS = 3072 IW

Address markers for each column:
000000h
0001FEh
000200h
0007FEh
000800h
001FFEh
002000h
003FFEh
004000h
0057FEh
0157FEh

TABLE 29-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0...W15}
Wnd	One of 16 destination working registers ∈ {W0...W15}
Wns	One of 16 source working registers ∈ {W0...W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X data space prefetch address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X data space prefetch destination register for DSP instructions ∈ {W4...W7}
Wy	Y data space prefetch address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y data space prefetch destination register for DSP instructions ∈ {W4...W7}

FIGURE 31-18: **SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**

Note: Refer to Figure 31-1 for load conditions.

TABLE 32-17: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+150°C for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Clock Parameters							
HAD50	TAD	ADC Clock Period[1]	147	—	—	ns	—
Conversion Rate							
HAD56	FCNV	Throughput Rate[1]	—	—	400	Ksps	—

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 32-18: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+150°C for High Temperature					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Clock Parameters							
HAD50	TAD	ADC Clock Period[1]	104	—	—	ns	—
Conversion Rate							
HAD56	FCNV	Throughput Rate[1]	—	—	800	Ksps	—

Note 1: These parameters are characterized but not tested in manufacturing.

NOTES: