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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K × 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b; D/A 6x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj128mc804-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 AND dsPIC33FJ128MCX02/X04 PRODUCT FAMILIES

The device names, pin counts, memory sizes, and peripheral availability of each device are listed in Table 1. The pages that follow show their pinout diagrams.

TABLE 1:dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 AND dsPIC33FJ128MCX02/X04CONTROLLER FAMILIES

						l	Remap	pable F	eriphe	ral			1).			
Device	Pins	Pins Program Flash Memory (Kbyte)		Remappable Pins	16-bit Timer ⁽²⁾	Input Capture	Output Compare Standard PWM	Motor Control PWM (Channels) ⁽³⁾	Quadrature Encoder Interface	UART	IdS	ECANTM	External Interrupts ⁽⁴⁾	RTCC	I²C™	CRC Generator	10-bit/12-bit ADC (Channels)	6-pin 16-bit DAC	Analog Comparator (2 Channels/Voltage Regulat	8-bit Parallel Master Port (Address Lines)	I/O Pins	Packages
dsPIC33FJ128MC804	44	128	16	26	5	4	4	6, 2	2	2	2	1	3	1	1	1	9	1	1/1	11	35	QFN TQFP
dsPIC33FJ128MC802	28	128	16	16	5	4	4	6, 2	2	2	2	1	3	1	1	1	6	0	1/0	2	21	SPDIP SOIC QFN-S
dsPIC33FJ128MC204	44	128	8	26	5	4	4	6, 2	2	2	2	0	3	1	1	1	9	0	1/1	11	35	QFN TQFP
dsPIC33FJ128MC202	28	128	8	16	5	4	4	6, 2	2	2	2	0	3	1	1	1	6	0	1/0	2	21	SPDIP SOIC QFN-S
dsPIC33FJ64MC804	44	64	16	26	5	4	4	6, 2	2	2	2	1	3	1	1	1	9	1	1/1	11	35	QFN TQFP
dsPIC33FJ64MC802	28	64	16	16	5	4	4	6, 2	2	2	2	1	3	1	1	1	6	0	1/0	2	21	SPDIP SOIC QFN-S
dsPIC33FJ64MC204	44	64	8	26	5	4	4	6, 2	2	2	2	0	3	1	1	1	9	0	1/1	11	35	QFN TQFP
dsPIC33FJ64MC202	28	64	8	16	5	4	4	6, 2	2	2	2	0	3	1	1	1	6	0	1/0	2	21	SPDIP SOIC QFN-S
dsPIC33FJ32MC304	44	32	4	26	5	4	4	6, 2	2	2	2	0	3	1	1	1	9	0	1/1	11	35	QFN TQFP
dsPIC33FJ32MC302	28	32	4	16	5	4	4	6, 2	2	2	2	0	3	1	1	1	6	0	1/0	2	21	SPDIP SOIC QFN-S

Note 1: RAM size is inclusive of 2 Kbytes of DMA RAM for all devices except dsPIC33FJ32MC302/304, which include 1 Kbyte of DMA RAM.

2: Only four out of five timers are remappable.

3: Only PWM fault pins are remappable.

4: Only two out of three interrupts are remappable.

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

- Note 1: This data sheet summarizes the features dsPIC33FJ32MC302/304. of the dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual". Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/ X04 family of 16-bit Digital Signal Controllers (DSC) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins
 (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVSS pins (regardless if ADC module is not used)
- (see Section 2.2 "Decoupling Capacitors")
 VCAP
 (see Section 2.3 "CPUL origination capacitor
- (see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")
- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see Section 2.5 "ICSP Pins")
- OSC1 and OSC2 pins when external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: Recommendation of 0.1 μ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high frequency noise: If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

TABL	E 4-2:	CHA	ANGE N	OTIFICA	TION R	EGISTEI	R MAP F	OR dsP	IC33FJ1	28MC20	2/802, d	IsPIC33I	J64MC	202/802	AND de	sPIC33F	J32MC3	;02
SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	—	—	—	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	CN30IE	CN29IE	-	CN27IE	—	—	CN24IE	CN23IE	CN22IE	CN21IE	_	-	_	_	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	—	—	—	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	_	CN30PUE	CN29PUE	_	CN27PUE	—	_	CN24PUE	CN23PUE	CN22PUE	CN21PUE	_	_	_	_	CN16PUE	0000
1							D											

x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

CHANGE NOTIFICATION REGISTER MAP FOR dsPIC33FJ128MC204/804, dsPIC33FJ64MC204/804 AND dsPIC33FJ32MC304 **TABLE 4-3**:

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	CN30IE	CN29IE	CN28IE	CN27IE	CN26IE	CN25IE	CN24IE	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	0068	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	CN30PUE	CN29PUE	CN28PUE	CN27PUE	CN26PUE	CN25PUE	CN24PUE	CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: I2C1 REGISTER MAP

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	_	_		_	_	_	_					Receive	Register				0000
I2C1TRN	0202	—	_	_	—	_	—	—	_				Transmit	Register				OOFF
I2C1BRG	0204	—	_	_	—	_	—	—	Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	_	—	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	_	_	—	—	_	Address Register								0000		
I2C1MSK	020C	_	_		_	_	_	Address Mask Register								0000		
Legend:	egend: x = unknown value on Reset. — = unimplemented, read as '0', Reset values are shown in hexadecimal.																	

TABLE 4-13: UART1 REGISTER MAP

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXISI	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	_	_	_	_	_	_	_	UTX8			U	IART Transn	nit Register				XXXX
U1RXREG	0226	_	_	_	_	_	_	_	URX8	UART Received Register						0000		
U1BRG	0228	Baud Rate Generator Prescaler										0000						

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-14: UART2 REGISTER MAP

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	-	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	_	_	_	_	_	UTX8			U	ART Transn	nit Register				XXXX
U2RXREG	0236	_	_	_	_	_	_	_	URX8	UART Receive Register							0000	
U2BRG	0238	Baud Rate Generator Prescaler										0000						

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

bit 2	CMIF: Comparator Interrupt Flag Status bit
	1 = Interrupt request has occurred0 = Interrupt request has not occurred
bit 1	MI2C1IF: I2C1 Master Events Interrupt Flag Status bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 0	SI2C1IF: I2C1 Slave Events Interrupt Flag Status bit
	 I = Interrupt request has occurred

0 = Interrupt request has not occurred

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—		T1IP<2:0>		—		OC1IP<2:0>	
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—		IC1IP<2:0>				INT0IP<2:0>	
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable I	bit	U = Unimple	mented bit, rea	ad as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cl	eared	x = Bit is unkr	nown
bit 15	Unimpleme	ented: Read as ')'				
bit 14-12	T1IP<2:0>:	Timer1 Interrupt	Priority bits				
	111 = Interr	rupt is priority 7 (I	nighest prior	ity interrupt)			
	•						
	•						
	001 = Interr	rupt is priority 1					
	000 = Interr	upt source is dis	abled				
bit 11	Unimpleme	ented: Read as '0)'				
bit 10-8	OC1IP<2:0	>: Output Compa	re Channel	1 Interrupt Prio	rity bits		
	111 = Interr	rupt is priority 7 (r	nignest prior	ity interrupt)			
	•						
	•						
	001 = Interr	rupt is priority 1	ablad				
hit 7		upt source is us	abieu				
bit 6 4		Input Conturo C) bonnol 1 Int	orrupt Drigrity	aita		
DIL 0-4	111 = Inter	unt is priority 7 (k	highest prior	ity interrunt)	JIIS		
	•	upt is priority 7 (i	ingricot prior	ity interrupt)			
	•						
	•	untin minute (
	001 = Interr	rupt is priority i rupt source is dis	abled				
bit 3	Unimpleme	ented: Read as ')'				
bit 2-0	INT0IP<2:0	>: External Interr	upt 0 Priority	/ bits			
	111 = Interr	rupt is priority 7 (I	nighest prior	ity interrupt)			
	•			- • • •			
	•						
	• 001 = Interr	rupt is priority 1					
	000 = Interr	rupt source is disa	abled				

DECISTED 7 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA	<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

REGISTER 8-3: DMAxSTA: DMA CHANNEL x RAM START ADDRESS REGISTER A⁽¹⁾

bit 15-0 STA<15:0>: Primary DMA RAM Start Address bits (source or destination)

Note 1: A read of this address register returns the current contents of the DMA RAM Address register, not the contents written to STA<15:0>. If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-4: DMAxSTB: DMA CHANNEL x RAM START ADDRESS REGISTER B⁽¹⁾

10.00-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		STB	<15:8>			
						bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		STE	3<7:0>			
						bit 0
	W = Writable bi	it	U = Unimplen	nented bit, rea	d as '0'	
ł	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
	R/W-0	R/W-0 R/W-0 W = Writable b '1' = Bit is set	STB R/W-0 R/W-0 R/W-0 STE W = Writable bit to '1' = Bit is set	STB<15:8> R/W-0 R/W-0 R/W-0 STB<7:0> STB<7:0> W = Writable bit U = Unimplen et '1' = Bit is set '0' = Bit is clear	STB<15:8> R/W-0 R/W-0 R/W-0 R/W-0 STB<7:0> STB<7:0> W = Writable bit U = Unimplemented bit, read V = Writable bit U = Unimplemented bit, read V = Writable bit 0' = Bit is cleared	STB<15:8> R/W-0 R/W-0 R/W-0 R/W-0 STB<7:0> STB<7:0>

bit 15-0 STB<15:0>: Secondary DMA RAM Start Address bits (source or destination)

Note 1: A read of this address register returns the current contents of the DMA RAM Address register, not the contents written to STB<15:0>. If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-7: DMACS0: DMA CONTROLLER STATUS REGISTER 0 (CONTINUED)

bit 3	XWCOL3: Channel 3 DMA RAM Write Collision Flag bit
	1 = Write collision detected0 = No write collision detected
bit 2	XWCOL2: Channel 2 DMA RAM Write Collision Flag bit
	1 = Write collision detected0 = No write collision detected
bit 1	XWCOL1: Channel 1 DMA RAM Write Collision Flag bit
	1 = Write collision detected0 = No write collision detected
bit 0	XWCOL0: Channel 0 DMA RAM Write Collision Flag bit
	1 = Write collision detected0 = No write collision detected

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	_			IC2R<4:0>		
bit 15							bit
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—			IC1R<4:0>		
bit 7							bit
Legend:	1- 6:4		L :4				
R = Readab		vv = vvritable	DIT		mented bit, rea		
-n = Value a	t POR	'1' = Bit is se	t	'0' = Bit is cle	eared	x = Bit is unkr	nown
	11001 = Inp • • • • • •	ut tied to RP25 ut tied to RP1					
	00000 = Inp	ut tied to RP0					
bit 7-5	Unimpleme	nted: Read as	·0 [·]				
bit 4-0	IC1R<4:0>:. 11111 = Inp 11001 = Inp	Assign Input Ca ut tied to Vss ut tied to RP25	apture 1 (IC1)†	to the correspo	onding RPn pii	n	
	00001 = Inp	ut tied to RP1 ut tied to RP0					

REGISTER 11-5: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

REGISTER	13-2. Tycow	. TIMER CO		GISTER (y -	3013)				
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
TON ⁽²⁾		TSIDL ⁽¹⁾	_	—	_	—			
bit 15						· · ·	bit 8		
U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0		
_	TGATE ⁽²⁾	TCKPS	<1:0> ⁽²⁾	_	—	TCS ⁽²⁾			
bit 7							bit C		
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	own		
bit 15	TON: Timery	On bit ⁽²⁾							
	1 = Starts 16-	bit Timerx							
	0 = Stops 16-		- 1						
Dit 14	Unimplemen	ted: Read as "). (1)						
DIT 13	I SIDL: Stop I	TSIDL: Stop in Idle Mode bit'							
	1 = Discontinue 0 = Continue	timer operation	i in Idle mode	nce enters idie	mode				
bit 12-7	Unimplemen	ted: Read as ') '						
bit 6	TGATE: Time	rx Gated Time	Accumulation	n Enable bit ⁽²⁾					
	When TCS =	1:							
	This bit is igno	ored.							
	When TCS =	<u>0:</u>							
	1 = Gated tim 0 = Gated tim	e accumulation	n disabled						
bit 5-4	TCKPS<1:0>	: Timerx Input	Clock Presca	le Select bits ⁽²)				
	11 = 1:256 pr	escale value							
	10 = 1:64 pre	scale value							
	01 = 1:8 pres	cale value							
	00 = 1:1 pres	cale value	- 1						
Dit 3-2		ted: Read as 1) [.]						
bit 1	1CS: TimerX								
	$\perp = \Box x e mai c$	ock (Fosc/2)	ν μιτ						
bit 0	Unimplement	ted: Read as '	ר י						
5.0	emplemen		<u>,</u>						

REGISTER 13-2: TyCON: TIMER CONTROL REGISTER (y = 3 or 5)

Note 1: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

2: When the 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), these bits have no effect.

dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 AND dsPIC33FJ128MCX02/X04

REGISTER 2	21-8: CiEC:	ECAN™ TRA	ANSMIT/RE	CEIVE ERRO	R COUNT RI	EGISTER	
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TERRC	NT<7:0>			
pit 15							bit
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RERRC	CNT<7:0>			
pit 7							bit (
_egend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
oit 15-8	TERRCNT<	7:0>: Transmit I	Error Count bi	its			
oit 7-0	RERRCNT<	7:0>: Receive E	Error Count bi	ts			
REGISTER 2	21-9: CiCF	G1: ECAN™ E	BAUD RATE		ATION REGI	STER 1	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	_	_	_
pit 15							bit 8
DAMA		DAMO	DAMA	DAMA	DAMA	DAMA	DAMA
R/W-U	R/W-U	R/W-U	R/W-0		R/W-U	R/W-0	R/W-0
	/~1.0/			DRI			hit (
							Ditt
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown
oit 15-8	Unimpleme	nted: Read as '	0'				
bit 7-6	SJW<1:0>:	Synchronization	Jump Width	bits			
	11 = Length	is 4 x TQ					
	10 = Length is 3 x To						
	01 = Length is 2 x 1Q						
Nit 5 0		Baud Pata Pros	calor bite				
bit 5-0 BRP<5:0>: Baud Rate		bauu Rate Fles					
	11 1111 =	$1Q = 2 \times 64 \times 1/$	FCAN				
	•						
	•						
	•						
	00 0010 =	TQ = 2 x 3 x 1/F	CAN				
	00 0001 =	$IQ = 2 \times 2 \times 1/F$	CAN				
	00 0000 =	1	CAN				

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REGISTER 24-1: CMCON: COMPARATOR CONTROL REGISTER (CONTINUED)

bit 6	C1OUT: Comparator 1 Output bit
	When C1INV = 0:
	1 = C1 VIN + > C1 VIN
	0 = C1 VIN + < C1 VIN -
	When $C1INV = 1$:
	0 = C1 VIN + > C1 VIN - 1 = C1 VIN + < C1
DIT 5	C2INV: Comparator 2 Output Inversion bit
	1 = C2 output inverted
DIT 4	CTINV: Comparator 1 Output Inversion bit
	1 = C1 output inverted
bit 3	C2NEG: Comparator 2 Negative Input Configure bit
	1 = Input is connected to VIN+
	See Figure 24-1 for Comparator modes
hit 2	C2POS: Comparator 2 Positivo Input Configuro bit
	1 = Input is connected to Vint
	$\Omega = Input is connected to CVREF$
	See Figure 24-1 for Comparator modes.
bit 1	C1NEG: Comparator 1 Negative Input Configure bit
	1 = Input is connected to ViN+
	0 = Input is connected to VIN-
	See Figure 24-1 for Comparator modes.
bit 0	C1POS: Comparator 1 Positive Input Configure bit
	1 = Input is connected to VIN+
	0 = Input is connected to CVREF
	See Figure 24-1 for Comparator modes.

- **Note 1:** If C2OUTEN = 1, the C2OUT peripheral output must be configured to an available RPx pin. See **Section 11.6 "Peripheral Pin Select"** for more information.
 - 2: If C1OUTEN = 1, the C1OUT peripheral output must be configured to an available RPx pin. See Section 11.6 "Peripheral Pin Select" for more information.

25.1 RTCC Module Registers

The RTCC module registers are organized into three categories:

- RTCC Control Registers
- RTCC Value Registers
- Alarm Value Registers

25.1.1 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding register pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTR bits (RCFGCAL<9:8>) to select the desired timer register pair (see Table 25-1).

By writing the RTCVALH byte, the RTCC Pointer value, RTCPTR<1:0> bits, decrement by one until they reach '00'. Once they reach '00', the MINUTES and SECONDS value will be accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

RTCPTR	RTCC Value Register Window			
<1:0>	RTCVAL<15:8>	RTCVAL<7:0>		
00	MINUTES	SECONDS		
01	WEEKDAY	HOURS		
10	MONTH	DAY		
11	_	YEAR		

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTR bits (ALCFGRPT<9:8>) to select the desired Alarm register pair (see Table 25-2).

By writing the ALRMVALH byte, the Alarm Pointer value, ALRMPTR<1:0> bits, decrement by one until they reach '00'. Once they reach '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.

TABLE 25-2: ALRMVAL REGISTER MAPPING

ALRMPTR	Alarm Value Register Window		
<1:0>	ALRMVAL<15:8>	ALRMVAL<7:0>	
00	ALRMMIN	ALRMSEC	
01	ALRMWD	ALRMHR	
10	ALRMMNTH	ALRMDAY	
11	—	—	

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL bytes will decrement the ALRMPTR<1:0> value. The same applies to the RTCVALH or RTCVALL bytes with the RTCPTR<1:0> being decremented.

Note:	This only applies to read operations and				
	not write operations.				

25.1.2 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RCFGCAL<13>) must be set (refer to Example 25-1).

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only 1 instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN; therefore, it is recommended that code follow the procedure in Example 25-1.

EXAMPLE 25-1: SETTING THE RTCWREN BIT

MOV MOV	#NVMKEY, W1 #0x55, W2	;move the address of NVMKEY into W1
MOV	#0xAA, W3	
MOV	W2, [W1]	;start 55/AA sequence
MOV	W3, [W1]	
BSET	RCFGCAL, #13	;set the RTCWREN bit

25.2 RTCC Resources

Many useful resources related to RTCC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwprod-
	ucts/Devices.aspx?dDoc-
	Name=en532315

25.2.1 KEY RESOURCES

- Section 37. "Real-Time Clock and Calendar (RTCC)" (DS70301)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 25-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾ (CONTINUED)

bit 7-0	CAL<7:0>: RTC Drift Calibration bits				
	11111111 = Minimum negative adjustment; subtracts 4 RTC clock pulses every one minute				
	•				
	•				
	•				
	10000000 = Maximum negative adjustment; subtracts 512 RTC clock pulses every one minute 01111111 = Maximum positive adjustment; adds 508 RTC clock pulses every one minute				
	•				
	•				
	•				
	00000001 = Minimum positive adjustment; adds 4 RTC clock pulses every one minute 00000000 = No adjustment				

- Note 1: The RCFGCAL register is only affected by a POR.
 - 2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
 - 3: This bit is read-only. It is cleared to '0' on a write to the lower half of the MINSEC register.

REGISTER 25-4:	RTCVAL (W	HEN RTCPTR<1:0> = 1	L): YEAR VALUE REGISTER ⁽¹⁾
----------------	-----------	---------------------	--

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	_	_	—	—	—		
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
	YRTEN	 <3:0>		YRONE<3:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'					
-n = Value at POR (1' = Bit is set				'0' = Bit is cleared x = Bit is unknown				

bit 15-8 Unimplemented: Read as '0'

bit 7-4 YRTEN<3:0>: Binary Coded Decimal Value of Year's Tens Digit; contains a value from 0 to 9

bit 3-0 YRONE<3:0>: Binary Coded Decimal Value of Year's Ones Digit; contains a value from 0 to 9

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 25-5: RTCVAL (WHEN RTCPTR<1:0> = 10): MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
—	—	—	MTHTEN0		MTHOM	NE<3:0>	
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTE	N<1:0>		DAYON	IE<3:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12 MTHTEN0: Binary Coded Decimal Value of Month's Tens Digit; contains a value of 0 or 1

bit 11-8MTHONE<3:0>: Binary Coded Decimal Value of Month's Ones Digit; contains a value from 0 to 9bit 7-6Unimplemented: Read as '0'

bit 5-4 DAYTEN<1:0>: Binary Coded Decimal Value of Day's Tens Digit; contains a value from 0 to 3

bit 3-0 DAYONE<3:0>: Binary Coded Decimal Value of Day's Ones Digit; contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
48	MPY	MPY Wm*Wn,Ad	cc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,A	cc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
49	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd		-(Multiply Wm by Wn) to Accumulator	1	1	None
50	MSC	MSC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd , AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
51	MUL	MUL.SS	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd {Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)		1	1	None	
		MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL	f	W3:W2 = f * WREG	1	1	None
52	NEG	NEG	Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = \overline{f} + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	C,DC,N,OV,Z
53	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
54	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)		2	None
		POP.S		Pop Shadow Registers	1	1	All
55	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
56	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
57	RCALL	RCALL	Expr	Relative Call	1	2	None
		RCALL	Wn	Computed Call	1	2	None
58	REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
59	RESET	RESET		Software device Reset	1	1	None
60	RETFIE	RETFIE		Return from interrupt	1	3 (2)	None
61	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	3 (2)	None
62	RETURN	RETURN		Return from Subroutine	1	3 (2)	None
63	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
<u> </u>		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
64	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f		1	N,Z
L		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
65	RRC	RRC	f	t = Rotate Right through Carry f	1	1	C,N,Z
		RRC	±,WREG	WKEG = Rotate Right through Carry f	1	1	C,N,Z
1	1	RRC	Ws,Wd	vva = Rotate Right through Carry Ws	1	1	C,N,Z

TABLE 29-2: INSTRUCTION SET OVERVIEW (CONTINUED)

TABLE 31-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le + 85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le + 125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions	
Operati	ng Voltag	e						
DC10	Supply \	/oltage						
	Vdd		3.0	_	3.6	V	Industrial and Extended	
DC12	Vdr	RAM Data Retention Voltage ⁽²⁾	1.8	_	—	V	—	
DC16	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal			Vss	V	_	
DC17	Svdd	VDD Rise Rate to ensure internal Power-on Reset signal	0.03	_	—	V/ms	0-3.0V in 0.1s	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

31.2 AC Characteristics and Timing Parameters

This section defines dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 AC characteristics and timing parameters.

TABLE 31-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)					
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial -40^{\circ}C < TA $\le +125^{\circ}C$ for Extended					
	Operating voltage VDD range as described in Table 31-1.					

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 31-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
DO50	Cosco	OSC2/SOSCO pin	_	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	Сю	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	Св	SCLx, SDAx	—	_	400	pF	In I ² C™ mode

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimens	Dimension Limits				
Contact Pitch	E		0.65 BSC		
Optional Center Pad Width	W2			6.80	
Optional Center Pad Length	T2			6.80	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.80	
Distance Between Pads	G	0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A