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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

⊡XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	64KB (64K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc202-i-mm

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.7 Arithmetic Logic Unit (ALU)

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register. The C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

3.7.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- · 8-bit unsigned x 8-bit unsigned

3.7.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.8 DSP Engine

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/ subtracter (with two target accumulators, round and saturation logic).

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 is a single-cycle instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources can be used concurrently by the same instruction (e.g., ED, EDAC).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- · Fractional or integer DSP multiply (IF)
- Signed or unsigned DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

A block diagram of the DSP engine is shown in Figure 3-3.

TABLE 3-1:	DSP INSTRUCTIONS
	SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \bullet y)$	Yes
MAC	A = A + x2	No
MOVSAC	No change in A	Yes
MPY	$A = x \bullet y$	No
MPY	A = x 2	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

5.2 RTSP Operation

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions) at a time, and to program one row or one word at a time. Table 31-12 shows typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 TBLWTL and TBLWTH instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 31-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time, and Word Write Cycle Time parameters (see Table 31-12).

EQUATION 5-1: PROGRAMMING TIME



For example, if the device is operating at +125°C, the FRC accuracy will be \pm 5%. If the TUN<5:0> bits (see Register 9-4) are set to `b111111, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \ Cycles}{7.37 \ MHz \times (1 + 0.05) \times (1 - 0.00375)} = 1.435 ms$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \text{ Cycles}}{7.37 \text{ MHz} \times (1 - 0.05) \times (1 - 0.00375)} = 1.586 \text{ms}$$

Setting the WR bit (NVMCON<15>) starts the operation, and the WR bit is automatically cleared when the operation is finished.

5.4 Control Registers

Two SFRs are used to read and write the program Flash memory:

- NVMCON: The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.
- NVMKEY: NVMKEY (Register 5-2) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to Section 5.3 "Programming Operations" for further details.

5.5 Flash Programming Resources

Many useful resources related to Flash programming are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en532315

5.5.1 KEY RESOURCES

- Section 5. "Flash Programming" (DS70191)
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

7.0 INTERRUPT CONTROLLER

- This data sheet summarizes the features Note 1: of dsPIC33FJ32MC302/304, the dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 32. "Interrupts (Part III)" (DS70214) of the "dsPIC33F/ PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with up to 118 vectors
- A unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Alternate Interrupt Vector Table (AIVT) for debug support
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The Interrupt Vector Table (IVT) shown in Figure 7-1, resides in program memory, starting at location 000004h. The IVT contains 126 vectors consisting of eight nonmaskable trap vectors plus up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with vector 0 takes priority over interrupts at any other vector address.

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 devices implement up to 53 unique interrupts and five nonmaskable traps. These are summarized in Table 7-1.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 7-1. Access to the AIVT is provided by the ALTIVT control bit (INTCON2<15>). If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time. If the AIVT is not needed, the AIVT should be programmed with the same addresses used in the IVT.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 device clears its registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT and AIVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

11.6 Peripheral Pin Select

Peripheral pin select configuration enables peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, programmers can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Programmers can independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral pin select is performed in software, and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping, once it has been established.

11.6.1 AVAILABLE PINS

The peripheral pin select feature is used with a range of up to 26 pins. The number of available pins depends on the particular device and its pin count. Pins that support the peripheral pin select feature include the designation RPn in their full pin designation, where RP designates a remappable peripheral and n is the remappable pin number.

11.6.2 CONTROLLING PERIPHERAL PIN SELECT

Peripheral pin select features are controlled through two sets of special function registers: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.6.2.1 Input Mapping

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. A control register associated with a peripheral dictates the pin it is mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-20). Each register contains sets of 5-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 5-bit value maps the RPn pin with that value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of peripheral pin selections supported by the device.

Figure 11-2 Illustrates remappable pin selection for U1RX input.

Note:	For input mapping only, the Peripheral Pin
	Select (PPS) functionality does not have
	priority over the TRISx settings.
	Therefore, when configuring the RPx pin
	for input, the corresponding bit in the
	TRISx register must also be configured for
	input (i.e., set to '1').

FIGURE 11-2: REMAPPABLE MUX INPUT FOR U1RX



REGISTER 11-13: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	—			INDX2R<4:0>		
bit 7		•					bit 0
Legend:							
R = Readable I	oit	W = Writable	bit U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-5 Unimplemented: Read as '0'

bit 4-0

INDX2R<4:0>: Assign QEI2 INDEX (INDX2) to the corresponding RPn pin 11111 = Input tied to Vss

11001 = Input tied to RP25

•

00001 = Input tied to RP1 00000 = Input tied to RP0

REGISTER 16-10:	PxOVDCON: OVERRIDE CONTROL REGISTER ⁽¹⁾	
REGISTER 16-10:	PxOVDCON: OVERRIDE CONTROL REGISTER ⁽¹⁾	

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L
bit 7				·	•		bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown			nown	
bit 15-14	Unimplemer	ted: Read as ')'				
bit 13-8	POVDxH<3:1>:POVDxL<3:1>: PWM Output Override bits						

 1 = Output on PWMx I/O pin is controlled by the PWM generator

 0 = Output on PWMx I/O pin is controlled by the value in the corresponding POUTxH:POUTxL bit

 bit 7-6
 Unimplemented: Read as '0'

 bit 5-0
 POUTxH<3:1>:POUTxL<3:1>: PWM Manual Output bits

1 = PWMx I/O pin is driven active when the corresponding POVDxH:POVDxL bit is cleared

 $_{0}$ = PWMx I/O pin is driven inactive when the corresponding POVDxH:POVDxL bit is cleared

Note 1: PWM2 supports only one PWM I/O pin pair.

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1 (CONTINUED)

- Note 1: This bit is not used in Framed SPI modes. Program this bit to '0' for the Framed SPI modes (FRMEN = 1).
 - 2: Do not set both Primary and Secondary prescalers to a value of 1:1.
 - **3:** This bit must be cleared when FRMEN = 1.

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT		_	_	BCL	GCSTAT	ADD10
bit 15							bit 8
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0
Legend:		C = Clear onl	y bit	U = Unimpler	mented bit, read	d as '0'	
R = Readable	bit	W = Writable	bit	HS = Set in h	ardware	HSC = Hardwa	are set/cleared
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
bit 15	ACKSTAT: Ac (when operati 1 = NACK rec 0 = ACK rece Hardware set	cknowledge St ing as I ² C™ m ceived from slav ived from slav or clear at enc	atus bit aster, applical ve e d of slave Acki	ble to master t	ransmit operati	on)	
bit 14	 TRSTAT: Transmit Status bit (when operating as I²C master, applicable to master transmit operation 1 = Master transmit is in progress (8 bits + ACK) 0 = Master transmit is not in progress Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge. 					smit operation) nowledge.	
bit 13-11	Unimplemen	ted: Read as '	0'				
bit 10	BCL: Master	Bus Collision [Detect bit				
	 1 = A bus collision has been detected during a master operation 0 = No collision Hardware set at detection of bus collision. 						
dit 9	GCSTAT: General Call Status bit 1 = General call address was received 0 = General call address was not received Hardware set when address matches general call address. Hardware clear at Stop detection.					ection.	
bit 8	ADD10: 10-bit Address Status bit						
	 1 = 10-bit address was matched 0 = 10-bit address was not matched Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection. 					detection.	
bit 7	IWCOL: Write	e Collision Dete	ect bit				
	1 = An attempt to write the I2CxTRN register failed because the I ² C module is busy 0 = No collision Hardware set at occurrence of write to I2CxTRN while busy (cleared by software)						
bit 6	I2COV: Recei	ive Overflow F	lag bit			,	
	 1 = A byte was received while the I2CxRCV register is still holding the previous byte 0 = No overflow Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software). 						
bit 5	 D_A: Data/Address bit (when operating as I²C slave) 1 = Indicates that the last byte received was data 0 = Indicates that the last byte received was device address Hardware clear at device address match. Hardware set by reception of slave byte 						
bit 4	P: Stop bit						
	1 = Indicates 0 = Stop bit w Hardware set	that a Stop bit as not detecte or clear when	has been dete d last Start, Repeat	ected last ed Start or Sto	p detected.		

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

REGISTER	21-5: CiFI	FO: ECAN™ F	FO STATUS	S REGISTER			
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_				FBF	P<5:0>		
bit 15							bit 8
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
				FNR	B<5:0>		
bit 7							bit 0
l egend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	nented bit. rea	ad as '0'	
-n = Value a	It POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 15-14	Unimpleme	ented: Read as '	0'				
bit 13-8	FBP<5:0>:	FIFO Buffer Poir	nter bits				
	011111 = F	RB31 buffer					
	011110 = F	RB30 buffer					
	•						
	•						
	•						
	000001 =]	TRB1 buffer					
	000000 = 1	RB0 buffer					
bit 7-6	Unimpleme	ented: Read as '	0'				
bit 5-0	FNRB<5:0>	>: FIFO Next Rea	ad Buffer Poin	iter bits			
	011111 = F	RB31 buffer					
	011110 = F	RB30 puffer					
	•						
	•						
	•						
	000001 =]	RB1 buffer					
	000000 = 1	I RBU DUTTER					

			• • • • • • • • • •					
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F7B	P<3:0>			F6BF	² <3:0>		
bit 15				·			bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F5BP<3:0>				F4BF	°<3:0>			
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	k = Bit is unknown	
bit 15-12	F7BP<3:0>	: RX Buffer Mas	k for Filter 7					
	1111 = Filte	er hits received in	n RX FIFO bu	ıffer				
	1110 = Filte	er hits received ir	n RX Buffer 1	4				
	•							
	•							
	•							
	0001 = Filte	er hits received ir	n RX Buffer 1					
	0000 = Filte	er hits received in	n RX Buffer 0					
bit 11-8	F6BP<3:0>	: RX Buffer Mas	k for Filter 6 (same values as	bit 15-12)			
bit 7-4	F5BP<3:0>	: RX Buffer Mas	k for Filter 5 (same values as	bit 15-12)			
					,			

REGISTER 21-13: CIBUFPNT2: ECAN™ FILTER 4-7 BUFFER POINTER REGISTER

bit 3-0	F4BP<3:0>: RX Buffer Mask for Filter 4	(same values as bit 15-12)

REGISTER 21-14: CIBUFPNT3: ECAN™ FILTER 8-11 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	F11BP	<3:0>			F10BI	P<3:0>				
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	F9BP	<3:0>			F8BF	°<3:0>				
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplen	U = Unimplemented bit, read as '0'					
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown						
bit 15-12	F11BP<3:0>:	RX Buffer Ma	sk for Filter 11	1						
	1111 = Filter	hits received in	RX FIFO bu	ffer						
	1110 = Filter	hits received in	n RX Buffer 1	4						
	•									
	•									
	•									
	0001 = Filter	hits received in	n RX Buffer 1							
h:+ 44 0	0000 = Filter hits received in RX Buffer 0									
DIT 11-8	F10BP<3:0>: RX Buffer Mask for Filter 10 (same values as bit 15-12)									
DIT 7-4	F9BP<3:0>: RX Buffer Mask for Filter 9 (same values as bit 15-12)									
DIT 3-U	F8B5<3:0>:	RX Buffer Mas	k for Filter 8 (same values as	DIT 15-12)					

REGISTER 22-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

```
bit 4-0 CH0SA<4:0>: Channel 0 Positive Input Select for Sample A bits

dsPIC33FJ32MC304, dsPIC33FJ64MC204/804 and dsPIC33FJ128MC204/804 devices only:

01000 = Channel 0 positive input is AN8

.

00010 = Channel 0 positive input is AN2

00001 = Channel 0 positive input is AN1

00000 = Channel 0 positive input is AN0

dsPIC33FJ32MC302, dsPIC33FJ64MC202/802 and dsPIC33FJ128MC202/802 devices only:

00101 = Channel 0 positive input is AN5

.
```

00010 = Channel 0 positive input is AN2 00001 = Channel 0 positive input is AN1 00000 = Channel 0 positive input is AN0

25.3 RTCC Registers

R/W-0 U-0 R/W-0 R-0 R-0 R/W-0 R/W-0 R/W-0 RTCEN⁽²⁾ RTCWREN RTCSYNC HALFSEC⁽³⁾ RTCOE RTCPTR<1:0> ____ bit 15 bit 8 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 CAL<7:0> bit 7 bit 0 Leaend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown RTCEN: RTCC Enable bit⁽²⁾ bit 15 1 = RTCC module is enabled 0 = RTCC module is disabled bit 14 Unimplemented: Read as '0' bit 13 RTCWREN: RTCC Value Registers Write Enable bit 1 = RTCVALH and RTCVALL registers can be written to by the user 0 = RTCVALH and RTCVALL registers are locked out from being written to by the user bit 12 RTCSYNC: RTCC Value Registers Read Synchronization bit 1 = RTCVALH, RTCVALL and ALCFGRPT registers can change while reading due to a rollover ripple resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid 0 = RTCVALH, RTCVALL or ALCFGRPT register can be read without concern over a rollover ripple HALFSEC: Half-Second Status bit(3) bit 11 1 = Second half period of a second 0 = First half period of a second bit 10 RTCOE: RTCC Output Enable bit 1 = RTCC output enabled 0 = RTCC output disabled bit 9-8 RTCPTR<1:0>: RTCC Value Register Window Pointer bits Points to the corresponding RTCC Value registers when reading RTCVALH and RTCVALL registers; the RTCPTR<1:0> value decrements on every read or write of RTCVALH until it reaches '00'. RTCVAL<15:8>: 11 = Reserved 10 = MONTH 01 = WEEKDAY 00 = MINUTESRTCVAL<7:0>: 11 = YEAR 10 = DAY 01 = HOURS 00 = SECONDS

REGISTER 25-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾

Note 1: The RCFGCAL register is only affected by a POR.

- 2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
- 3: This bit is read-only. It is cleared to '0' on a write to the lower half of the MINSEC register.

							- 4 · · · -
R-0	R/W-0	R/W-0	R/W-0 R/W-0 R/W		R/W-0	R/W-0	R/W-0
BUSY	IRQM	/<1:0>	INCI	//<1:0>	MODE16	MODE	<u>=<1:0></u>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAITB	<1:0> ⁽¹⁾		WAIT	M<3:0>	1011 0	WAITE	<1:0> ⁽¹⁾
bit 7	-						bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	BUSV BUSY	hit (Master mor	le only)				
bit 15	1 = Port is bu	isv (not useful v	when the proc	essor stall is a	active)		
	0 = Port is no	ot busy					
bit 14-13	IRQM<1:0>:	Interrupt Reque	est Mode bits				
	11 = Interrup	t generated who	en Read Buffe	er 3 is read or	Write Buffer 3 is	written (Buffere	ed PSP mode)
	or on a r	read or write op	processor st	PMA<1:0> = : all activated	11 (Addressable	PSP mode on	IY)
	01 = Interrup	t generated at t	he end of the	read/write cyc	cle		
	00 = No inter	rupt generated					
bit 12-11	INCM<1:0>:	Increment Mod	e bits				
	11 = PSP rea	ad and write but	fers auto-incr	rement (Legac	y PSP mode onl	у)	
	01 = Increme	ent ADDR<10:0	> by 1 every	read/write cycl	e		
	00 = No incre	ement or decrer	ment of addre	SS			
bit 10	MODE16: 8/1	16-bit Mode bit					
	1 = 16-bit mo 0 = 8-bit mod	de: data registe le: data register	er is 16 bits, a r is 8 bits, a re	read or write t ad or write to	to the data regist the data register	er invokes two invokes one 8	8-bit transfers -bit transfer
bit 9-8	MODE<1:0>:	Parallel Port M	lode Select b	its			
	11 = Master I	mode 1 (PMCS	1, PMRD/PM	WR, PMENB,	PMBE, PMA <x:< td=""><td>0> and PMD<7</td><td>(<0>)</td></x:<>	0> and PMD<7	(<0>)
	10 = Master mode 2 (PMUS1, PMRD, PMWR, PMBE, PMA <x:0> and PMD<7:0>) 0.1 = Enhanced PSP control signals (PMRD PMWR PMCS1 PMD<7:0> and PMA<1:0>)</x:0>						:0>)
	00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1 and PMD<7:0>)						0>)
bit 7-6	WAITB<1:0>: Data Setup to Read/Write Wait State Configuration bits ⁽¹⁾						
	11 = Data wa	ait of 4 TCY; mul	tiplexed addr	ess phase of 4	TCY		
	10 = Data wa	ait of 3 ICY; mul	tiplexed addre	ess phase of 3 ess phase of 2	ICY CCY		
	00 = Data wa	ait of 1 TCY; mul	tiplexed addr	ess phase of 1	TCY		
bit 5-2	WAITM<3:0>	Read to Byte	Enable Strob	e Wait State C	onfiguration bits	i	
	1111 = Wait	of additional 15	TCY				
	•						
	•		F =				
	0001 = Walt = 0000 = No ac	of additional 1	ICY (cles (operation)	on forced into	one Tcy)		
bit 1-0	WAITE<1:0>	: Data Hold Affe	er Strobe Wai	t State Config	uration bits ⁽¹⁾		
	11 = Wait of 4	4 TCY					
	10 = Wait of 3	3 Тсү					
	01 = Wait of 2 00 = Wait of 2	∠ ICY 1 TCY					

Register 27-2: PMMODE: PARALLEL PORT MODE REGISTER

Note 1: WAITB and WAITE bits are ignored whenever WAITM3:WAITM0 = 0000.

28.0 SPECIAL FEATURES

- Note 1: This data sheet summarizes the features dsPIC33FJ32MC302/304. of the dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual". Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 devices include the following features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components:

- Flexible configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- · JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation

Address Bit 7 Bit 6 Bit 1 Bit 0 Name Bit 5 Bit 4 Bit 3 Bit 2 0xF80000 FBS RBS<1:0> BSS<2:0> BWRP FSS⁽¹⁾ 0xF80002 RSS<1:0> SSS<2:0> SWRP 0xF80004 GWRP FGS ____ ____ GSS<1:0> ____ ____ ____ 0xF80006 FOSCSEL FNOSC<2:0> IESO OSCIOFNC POSCMD<1:0> 0xF80008 FOSC FCKSM<1:0> **IOL1WAY** 0xF8000A FWDT FWDTEN WINDIS _ WDTPRE WDTPOST<3:0> PWMPIN 0xF8000C FPOR HPOL LPOL ALTI2C FPWRT<2:0> Reserved⁽²⁾ 0xF8000E FICD **JTAGEN** ICS<1:0> 0xF80010 FUID0 User Unit ID Byte 0 0xF80012 FUID1 User Unit ID Byte 1 0xF80014 FUID2 User Unit ID Byte 2 0xF80016 FUID3 User Unit ID Byte 3

TABLE 28-1: DEVICE CONFIGURATION REGISTER MAP

Legend: — = unimplemented bit, read as '0'.

Note 1: This Configuration register is not available and reads as 0xFF on dsPIC33FJ32MC302/304 devices.

2: These bits are reserved for use by development tools and must be programmed as '1'.

28.1 Configuration Bits

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/ X04 and dsPIC33FJ128MCX02/X04 devices provide nonvolatile memory implementations for device Configuration bits. Refer to **Section 25.** "**Device Configuration**" (DS70194) in the "*dsPIC33F/PIC24H Family Reference Manual*" for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 28-2.

Note that address 0xF80000 is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using table reads and table writes.

The Device Configuration register map is shown in Table 28-1.

DC CHARACT	ERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le + 85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Parameter No. ⁽³⁾	Typical ⁽²⁾	Мах	Units Conditions					
Operating Cur	rent (IDD) ⁽¹⁾							
DC20d	18	21	mA	-40°C				
DC20a	18	22	mA	+25°C	2.3//			
DC20b	18	22	mA	+85°C	5.3V	10 1011-3		
DC20c	18	25	mA	+125°C				
DC21d	30	35	mA	-40°C		16 MIPS		
DC21a	30	34	mA	+25°C	2.3//			
DC21b	30	34	mA	+85°C	5.3V	10 1011-5		
DC21c	30	36	mA	+125°C				
DC22d	34	42	mA	-40°C		20 MIPS		
DC22a	34	41	mA	+25°C	2 2)/			
DC22b	34	42	mA	+85°C	5.3V			
DC22c	35	44	mA	+125°C				
DC23d	49	58	mA	-40°C				
DC23a	49	57	mA	+25°C	2 2)/			
DC23b	49	57	mA	+85°C	5.3V	30 IVIIF 3		
DC23c	49	60	mA	+125°C				
DC24d	63	75	mA	-40°C				
DC24a	63	74	mA	+25°C	2 2)/			
DC24b	63	74	mA	+85°C	3.3V	40 101175		
DC24c	63	76	mA	+125°C				

TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

• Oscillator is configured in EC mode, no PLL until 10 MIPS, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero)
- CPU executing while (1) statement
- JTAG is disabled
- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- 3: These parameters are characterized but not tested in manufacturing.

31.2 AC Characteristics and Timing Parameters

This section defines dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 AC characteristics and timing parameters.

TABLE 31-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)					
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial -40^{\circ}C < TA $\le +125^{\circ}C$ for Extended					
	Operating voltage VDD range as described in Table 31-1.					

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 31-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
DO50	Cosco	OSC2/SOSCO pin	_	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	Сю	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	Св	SCLx, SDAx	—	_	400	pF	In I ² C™ mode







FIGURE 31-27: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0. SSRC<2:0> = 000)

TABLE 31-51: COMPARATOR REFERENCE VOLTAGE SETTLING TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
VR310	TSET	Settling Time ⁽¹⁾	—	_	10	μs	—

Note 1: Setting time measured while CVRR = 1 and CVR3:CVR0 bits transition from '0000' to '1111'.

TABLE 31-52: COMPARATOR REFERENCE VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \leq TA \leq +85^{\circ}C$ for Industrial $-40^{\circ}C \leq TA \leq +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic	Min	Тур	Мах	Units	Conditions
VRD310	CVRES	Resolution	CVRSRC/24	_	CVRSRC/32	LSb	—
VRD311	CVRAA	Absolute Accuracy	—		0.5	LSb	—
VRD312	CVRur	Unit Resistor Value (R)	—	2k	—	Ω	—

FIGURE 31-30: PARALLEL SLAVE PORT TIMING DIAGRAM



Revision D (November 2009)

The revision includes the following global update:

• Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers"	Added information on high temperature operation (see " Operating Range: ").
Section 11.0 "I/O Ports"	Changed the reference to digital-only pins to 5V tolerant pins in the second paragraph of Section 11.2 " Open-Drain Configuration ".
Section 20.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the two baud rate range features to: 10 Mbps to 38 bps at 40 MIPS.
Section 22.0 "10-bit/12-bit Analog-to-Digital Converter (ADC1)"	Updated the ADC block diagrams (see Figure 22-1 and Figure 22-2).
Section 23.0 "Audio Digital-to-Analog	Removed last sentence of the first paragraph in the section.
Converter (DAC)"	Added a shaded note to Section 23.2 "DAC Module Operation".
	Updated Figure 23-2: "Audio DAC Output for Ramp Input (Unsigned)".
Section 28.0 "Special Features"	Updated the second paragraph and removed the fourth paragraph in Section 28.1 "Configuration Bits" .
	Updated the Device Configuration Register Map (see Table 28-1).
Section 31.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings for high temperature and added Note 4.
	Removed parameters DI26, DI28 and DI29 from the I/O Pin Input Specifications (see Table 31-9).
	Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics (see Figure 31-17).
	Removed Table 31-45: Audio DAC Module Specifications. Original contents were updated and combined with Table 31-44 of the same name.
Section 32.0 "High Temperature Electrical Characteristics"	Added new chapter with high temperature specifications.
"Product Identification System"	Added the "H" definition for high temperature.