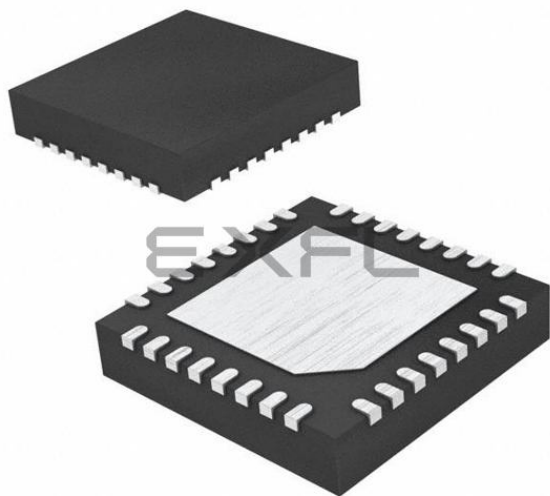




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc202t-i-mm

TABLE 4-20: DMA REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
DMA0CON	0380	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA0REQ	0382	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA0STA	0384	STA<15:0>																	0000
DMA0STB	0386	STB<15:0>																	0000
DMA0PAD	0388	PAD<15:0>																	0000
DMA0CNT	038A	—	—	—	—	—	—	CNT<9:0>											0000
DMA1CON	038C	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA1REQ	038E	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA1STA	0390	STA<15:0>																	0000
DMA1STB	0392	STB<15:0>																	0000
DMA1PAD	0394	PAD<15:0>																	0000
DMA1CNT	0396	—	—	—	—	—	—	CNT<9:0>											0000
DMA2CON	0398	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA2REQ	039A	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA2STA	039C	STA<15:0>																	0000
DMA2STB	039E	STB<15:0>																	0000
DMA2PAD	03A0	PAD<15:0>																	0000
DMA2CNT	03A2	—	—	—	—	—	—	CNT<9:0>											0000
DMA3CON	03A4	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA3REQ	03A6	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA3STA	03A8	STA<15:0>																	0000
DMA3STB	03AA	STB<15:0>																	0000
DMA3PAD	03AC	PAD<15:0>																	0000
DMA3CNT	03AE	—	—	—	—	—	—	CNT<9:0>											0000
DMA4CON	03B0	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA4REQ	03B2	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA4STA	03B4	STA<15:0>																	0000
DMA4STB	03B6	STB<15:0>																	0000
DMA4PAD	03B8	PAD<15:0>																	0000
DMA4CNT	03BA	—	—	—	—	—	—	CNT<9:0>											0000
DMA5CON	03BC	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA5REQ	03BE	FORCE	—	—	—	—	—	—	—	—	IRQSEL<6:0>								0000
DMA5STA	03C0	STA<15:0>																	0000
DMA5STB	03C2	STB<15:0>																	0000

Legend: — = unimplemented, read as '0'.

TABLE 7-1: INTERRUPT VECTORS

Vector Number	IVT Address	AIVT Address	Interrupt Source
0	0x000004	0x000104	Reserved
1	0x000006	0x000106	Oscillator Failure
2	0x000008	0x000108	Address Error
3	0x00000A	0x00010A	Stack Error
4	0x00000C	0x00010C	Math Error
5	0x00000E	0x00010E	DMA Error
6-7	0x000010-0x000012	0x000110-0x000112	Reserved
8	0x000014	0x000114	INT0 – External Interrupt 0
9	0x000016	0x000116	IC1 – Input Capture 1
10	0x000018	0x000118	OC1 – Output Compare 1
11	0x00001A	0x00011A	T1 – Timer1
12	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	0x00001E	0x00011E	IC2 – Input Capture 2
14	0x000020	0x000120	OC2 – Output Compare 2
15	0x000022	0x000122	T2 – Timer2
16	0x000024	0x000124	T3 – Timer3
17	0x000026	0x000126	SPI1E – SPI1 Error
18	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	0x00002A	0x00012A	U1RX – UART1 Receiver
20	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	0x00002E	0x00012E	ADC1 – ADC 1
22	0x000030	0x000130	DMA1 – DMA Channel 1
23	0x000032	0x000132	Reserved
24	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	0x000038	0x000138	CM – Comparator Interrupt
27	0x00003A	0x00013A	Change Notification Interrupt
28	0x00003C	0x00013C	INT1 – External Interrupt 1
29	0x00003E	0x00013E	Reserved
30	0x000040	0x000140	IC7 – Input Capture 7
31	0x000042	0x000142	IC8 – Input Capture 8
32	0x000044	0x000144	DMA2 – DMA Channel 2
33	0x000046	0x000146	OC3 – Output Compare 3
34	0x000048	0x000148	OC4 – Output Compare 4
35	0x00004A	0x00014A	T4 – Timer4
36	0x00004C	0x00014C	T5 – Timer5
37	0x00004E	0x00014E	INT2 – External Interrupt 2
38	0x000050	0x000150	U2RX – UART2 Receiver
39	0x000052	0x000152	U2TX – UART2 Transmitter
40	0x000054	0x000154	SPI2E – SPI2 Error
41	0x000056	0x000156	SPI2 – SPI2 Transfer Done
42	0x000058	0x000158	C1RX – ECAN1 RX Data Ready
43	0x00005A	0x00015A	C1 – ECAN1 Event
44	0x00005C	0x00015C	DMA3 – DMA Channel 3
45-52	0x00005E-0x00006C	0x00015E-0x00016C	Reserved
53	0x00006E	0x00016E	PMP – Parallel Master Port
54	0x000070	0x000170	DMA – DMA Channel 4

REGISTER 7-16: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T2IP<2:0>			—	OC2IP<2:0>		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC2IP<2:0>			—	DMA0IP<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OC2IP<2:0>:** Output Compare Channel 2 Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IC2IP<2:0>:** Input Capture Channel 2 Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DMA0IP<2:0>:** DMA Channel 0 Data Transfer Complete Interrupt Priority bits
 111 = Interrupt is priority 7 (highest priority interrupt)
 •
 •
 •
 001 = Interrupt is priority 1
 000 = Interrupt source is disabled

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CMPMD	RTCCMD	PMPMD
bit 15					bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
CRCMD	DAC1MD	QE12MD	PWM2MD	—	—	—	—
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **CMPMD:** Comparator Module Disable bit
 - 1 = Comparator module is disabled
 - 0 = Comparator module is enabled
- bit 9 **RTCCMD:** RTCC Module Disable bit
 - 1 = RTCC module is disabled
 - 0 = RTCC module is enabled
- bit 8 **PMPMD:** PMP Module Disable bit
 - 1 = PMP module is disabled
 - 0 = PMP module is enabled
- bit 7 **CRCMD:** CRC Module Disable bit
 - 1 = CRC module is disabled
 - 0 = CRC module is enabled
- bit 6 **DAC1MD:** DAC1 Module Disable bit
 - 1 = DAC1 module is disabled
 - 0 = DAC1 module is enabled
- bit 5 **QE12MD:** QE12 Module Disable bit
 - 1 = QE12 module is disabled
 - 0 = QE12 module is enabled
- bit 4 **PWM2MD:** PWM2 Module Disable bit
 - 1 = PWM2 module is disabled
 - 0 = PWM2 module is enabled
- bit 3-0 **Unimplemented:** Read as '0'

REGISTER 11-4: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T5CKR<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T4CKR<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **T5CKR<4:0>:** Assign Timer5 External Clock (T5CK) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **T4CKR<4:0>:** Assign Timer4 External Clock (T4CK) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

REGISTER 11-18: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SCK2R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SDI2R<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **SCK2R<4:0>:** Assign SPI2 Clock Input (SCK2) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **SDI2R<4:0>:** Assign SPI2 Data Input (SDI2) to the corresponding RPn pin

11111 = Input tied to Vss

11001 = Input tied to RP25

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

REGISTER 11-31: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10⁽¹⁾

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP21R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP20R<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **RP21R<4:0>**: Peripheral Output Function is Assigned to RP21 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP20R<4:0>**: Peripheral Output Function is Assigned to RP20 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)

Note 1: This register is implemented in 44-pin devices only.

REGISTER 11-32: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11⁽¹⁾

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP23R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP22R<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

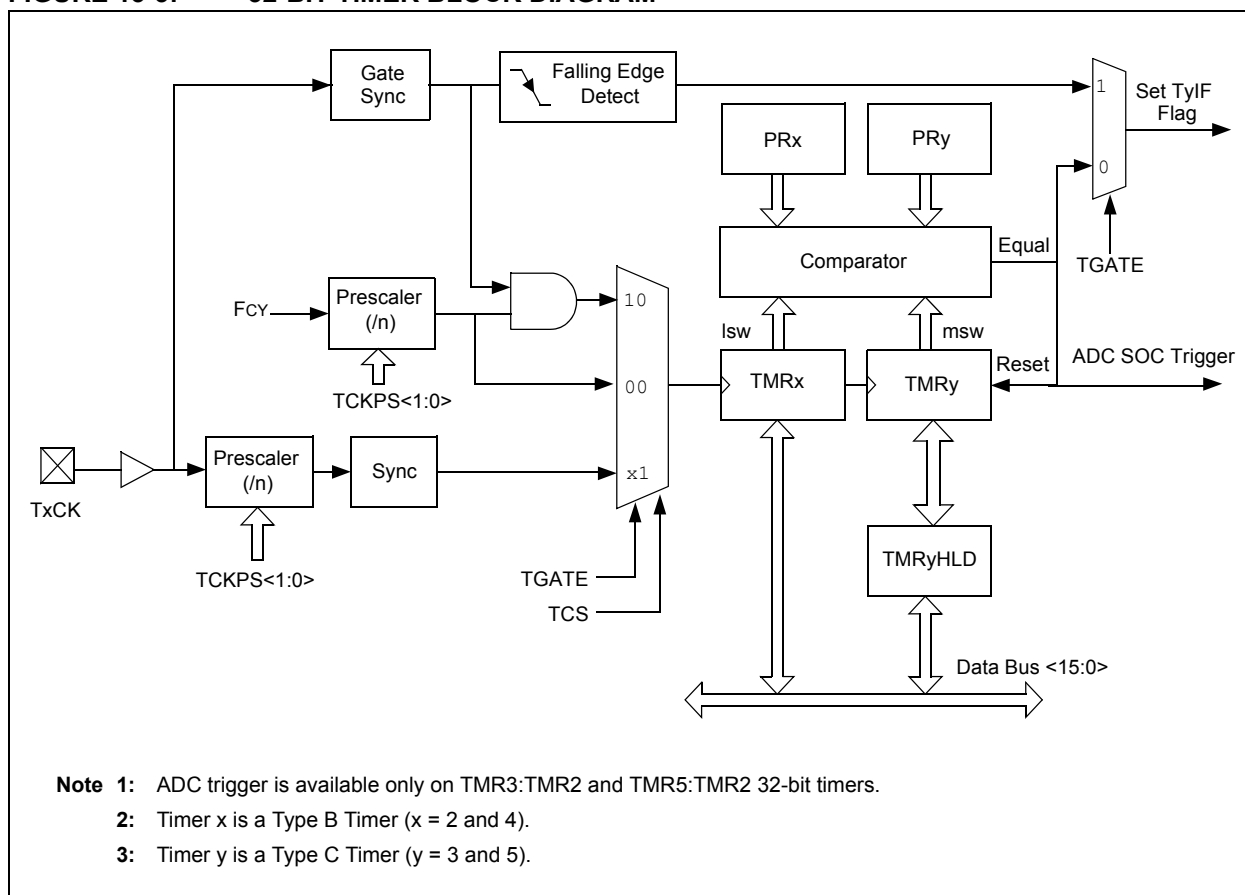
bit 12-8 **RP23R<4:0>**: Peripheral Output Function is Assigned to RP23 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP22R<4:0>**: Peripheral Output Function is Assigned to RP22 Output Pin bits (see [Table 11-2](#) for peripheral function numbers)

Note 1: This register is implemented in 44-pin devices only.

FIGURE 13-3: 32-BIT TIMER BLOCK DIAGRAM



13.3 Timer Resources

Many useful resources related to Timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315>

13.3.1 KEY RESOURCES

- **Section 11. “Timers”** (DS70205)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

16.3 Motor Control PWM Resources

Many useful resources related to Motor Control PWM are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315
--

16.3.1 KEY RESOURCES

- **Section 14. “Motor Control PWM”** (DS70187)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE

Note 1: This data sheet summarizes the features of the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Quadrature Encoder Interface (QEI)”** (DS70208) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

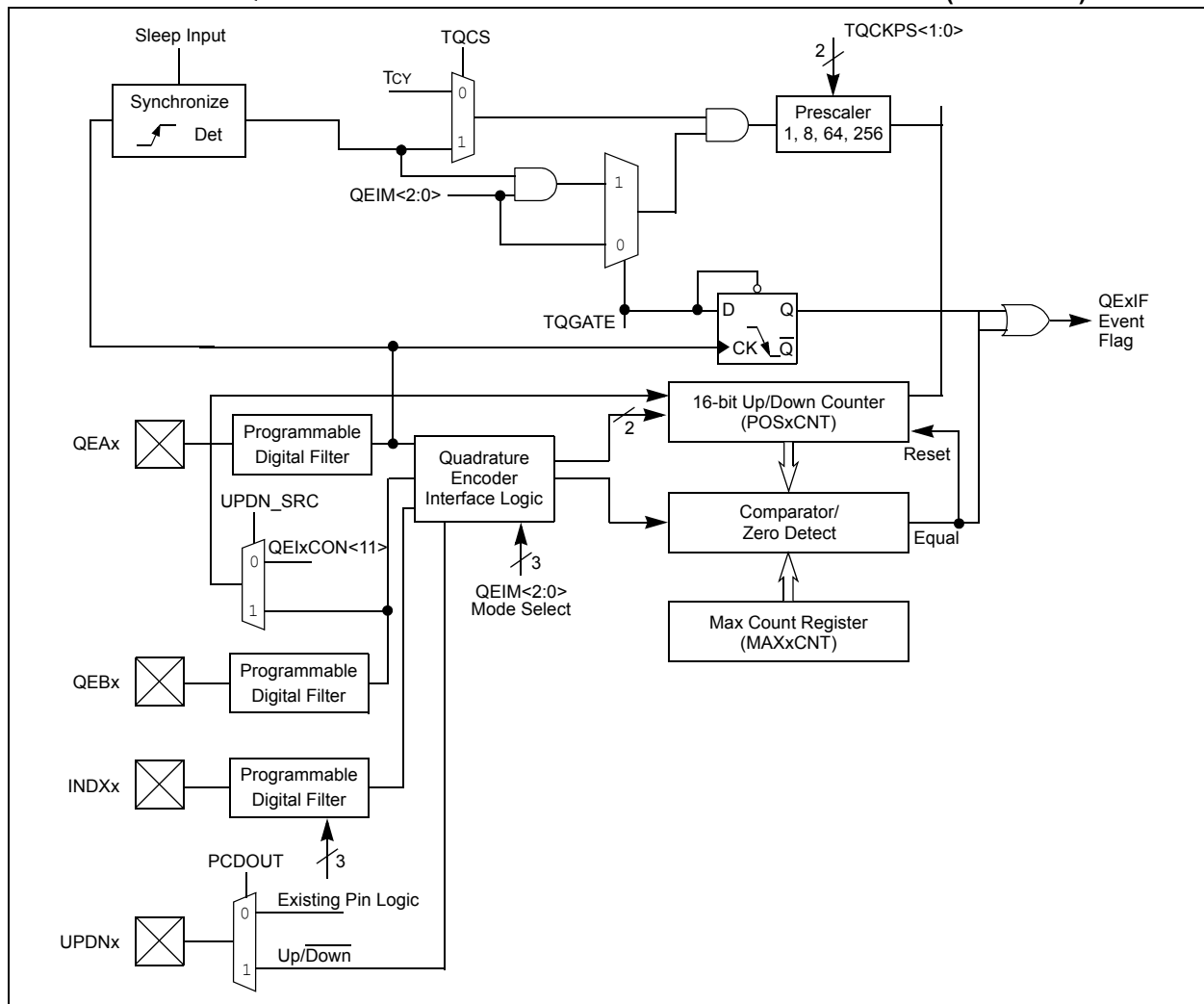
The operational features of the QEI include:

- Three input channels for two phase signals and index pulse
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode
- Quadrature Encoder Interface interrupts

These operating modes are determined by setting the appropriate bits, QEIM<2:0> bits (QEIXCON<10:8>). **Figure 17-1** depicts the Quadrature Encoder Interface block diagram.

Note: An ‘x’ used in the names of pins, control/status bits and registers denotes a particular Quadrature Encoder Interface (QEI) module number (x = 1 or 2).

FIGURE 17-1: QUADRATURE ENCODER INTERFACE BLOCK DIAGRAM (x = 1 OR 2)



REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK9	AMSK8
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSKx:** Mask for Address bit x Select bit

1 = Enable masking for bit x of incoming message address; bit match not required in this position

0 = Disable masking for bit x; bit match required in this position

24.3 Comparator Voltage Reference

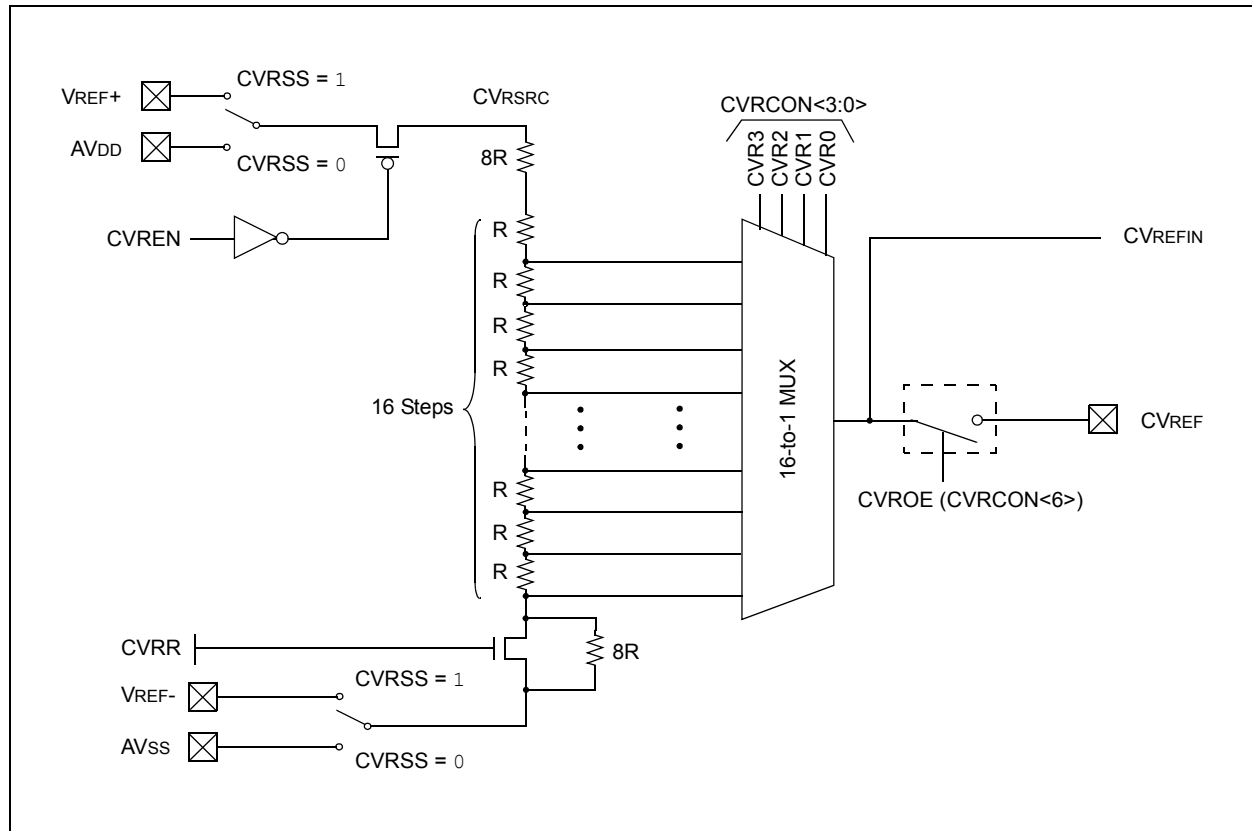
24.3.1 CONFIGURING THE COMPARATOR VOLTAGE REFERENCE

The voltage reference module is controlled through the CVRCON register ([Register 24-2](#)). The comparator voltage reference provides two ranges of output voltage, each with 16 distinct levels. The range to be used is selected by the CVRR bit (CVRCON<5>). The primary difference between the ranges is the size of the steps selected by the CVREF Selection bits (CVR3:CVR0), with one range offering finer resolution.

The comparator reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF-. The voltage source is selected by the CVRSS bit (CVRCON<4>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 24-2: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



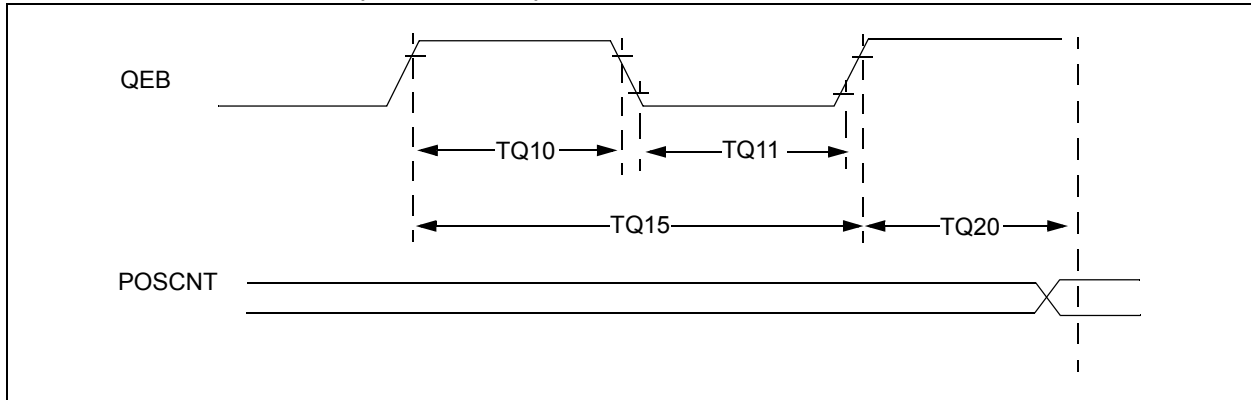
NOTES:

TABLE 28-5: CODE FLASH SECURITY SEGMENT SIZES FOR 128 KB DEVICES

CONFIG BITS	BSS<2:0> = x11 0K		BSS<2:0> = x10 1K		BSS<2:0> = x01 4K		BSS<2:0> = x00 8K	
SSS<2:0> = x11 0K	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h
			BS = 768 IW		BS = 3840 IW		BS = 7936 IW	
	GS = 43776 IW	0157FEh	GS = 43008 IW	0157FEh	GS = 39936 IW	0157FEh	GS = 35840 IW	0157FEh
SSS<2:0> = x10 4K	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00ABFEh	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00ABFEh	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00ABFEh	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00ABFEh
	SS = 3840 IW		BS = 768 IW		BS = 3840 IW		BS = 7936 IW	
			SS = 3072 IW					
	GS = 39936 IW	0157FEh	GS = 39936 IW	0157FEh	GS = 39936 IW	0157FEh	GS = 35840 IW	0157FEh
SSS<2:0> = x01 8K	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h
			BS = 768 IW		BS = 3840 IW		BS = 7936 IW	
	SS = 7936 IW		SS = 7168 IW		SS = 4096 IW			
	GS = 35840 IW	0157FEh	GS = 35840 IW	0157FEh	GS = 35840 IW	0157FEh	GS = 35840 IW	0157FEh
SSS<2:0> = x00 16K	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h	VS = 256 IW	000000h 0001FEh 000200h 0007FEh 000800h 001FFEh 002000h 003FFEh 004000h 007FFEh 008000h 00FFFEh 010000h
			BS = 768 IW		BS = 3840 IW		BS = 7936 IW	
	SS = 16128 IW		SS = 15360 IW		SS = 12288 IW		SS = 8192 IW	
	GS = 27648 IW	0157FEh	GS = 27648 IW	0157FEh	GS = 27648 IW	0157FEh	GS = 27648 IW	0157FEh

TABLE 29-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions $\in \{W4 * W4, W5 * W5, W6 * W6, W7 * W7\}$
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions $\in \{W4 * W5, W4 * W6, W4 * W7, W5 * W6, W5 * W7, W6 * W7\}$
Wn	One of 16 working registers $\in \{W0...W15\}$
Wnd	One of 16 destination working registers $\in \{W0...W15\}$
Wns	One of 16 source working registers $\in \{W0...W15\}$
WREG	W0 (working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$
Wx	X data space prefetch address register for DSP instructions $\in \{[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], \text{none}\}$
Wxd	X data space prefetch destination register for DSP instructions $\in \{W4...W7\}$
Wy	Y data space prefetch address register for DSP instructions $\in \{[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], \text{none}\}$
Wyd	Y data space prefetch destination register for DSP instructions $\in \{W4...W7\}$

FIGURE 31-6: TIMERQ (QE1 MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS**TABLE 31-25: QE1 MODULE EXTERNAL CLOCK TIMING REQUIREMENTS**

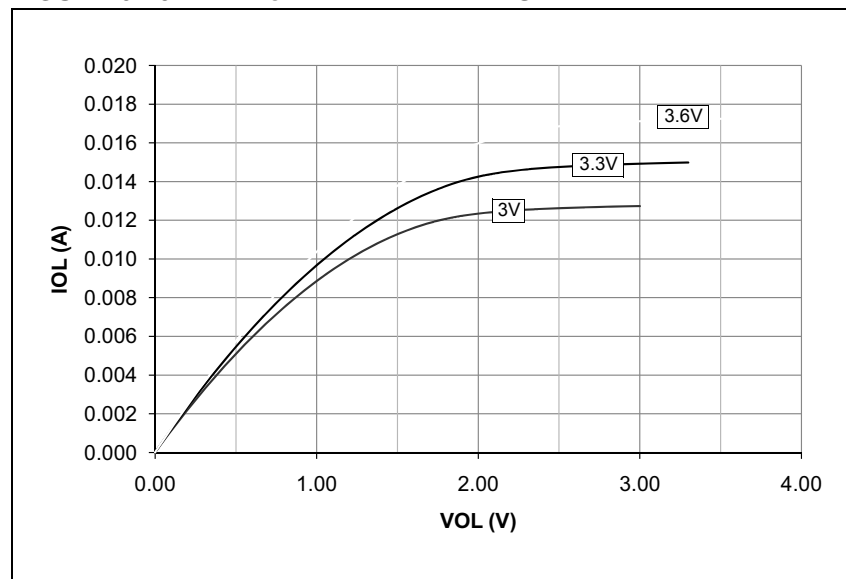
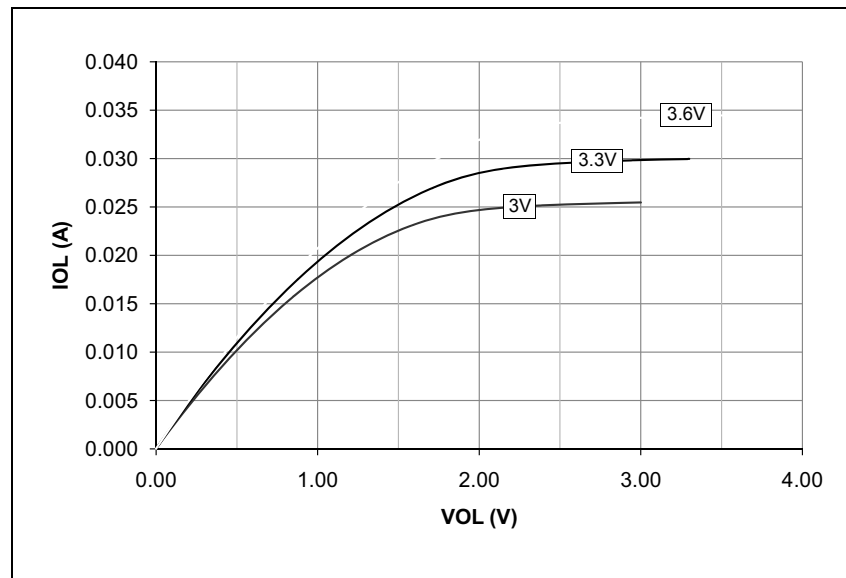
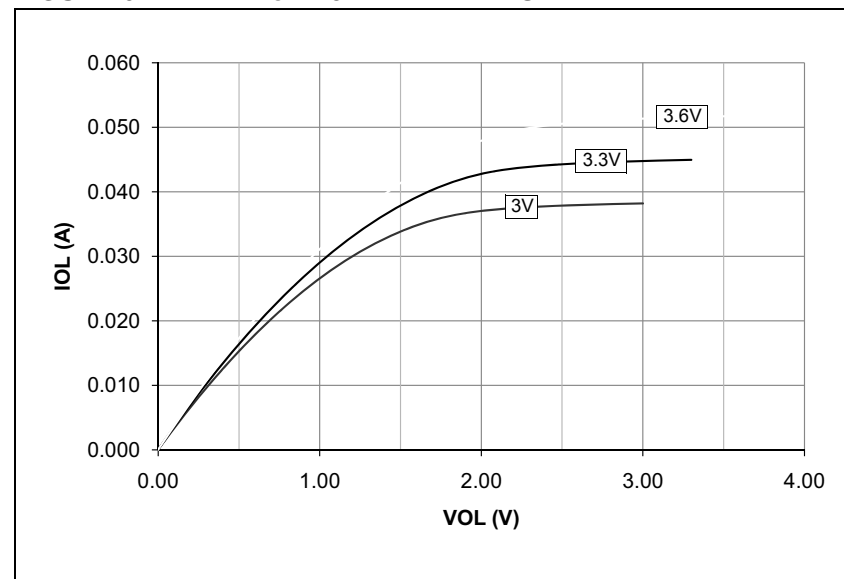
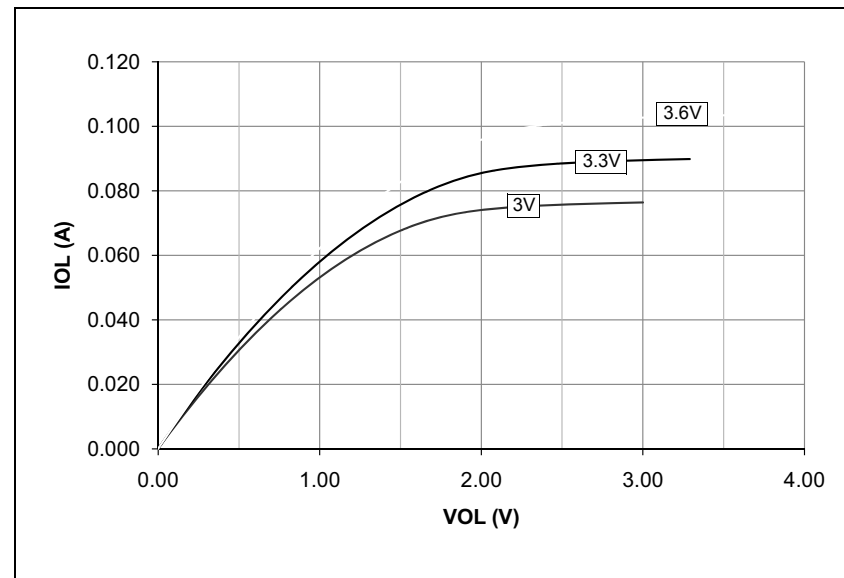
AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min	Typ	Max	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Tcy + 20		—	ns	Must also meet parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Tcy + 20		—	ns	Must also meet parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	2 * Tcy + 40		—	ns	—
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.5 Tcy		1.5 Tcy	—	—

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 32-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ for High Temperature				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	Output Low Voltage I/O Pins: 2x Sink Driver Pins - RA2, RA7-RA10, RB10, RB11, RB7, RB4, RC3-RC9	—	—	0.4	V	$I_{OL} \leq 1.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output Low Voltage I/O Pins: 4x Sink Driver Pins - RA0, RA1, RB0-RB3, RB5, RB6, RB8, RB9, RB12-RB15, RC0-RC2	—	—	0.4	V	$I_{OL} \leq 3.6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA3, RA4	—	—	0.4	V	$I_{OL} \leq 6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
DO20	VOH	Output High Voltage I/O Pins: 2x Source Driver Pins - RA2, RA7-RA10, RB4, RB7, RB10, RB11, RC3-RC9	2.4	—	—	V	$I_{OL} \geq -1.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage I/O Pins: 4x Source Driver Pins - RA0, RA1, RB0-RB3, RB5, RB6, RB8, RB9, RB12-RB15, RC0-RC2	2.4	—	—	V	$I_{OL} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage I/O Pins: 8x Source Driver Pins - RA4, RA3	2.4	—	—	V	$I_{OL} \geq -6 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
DO20A	VOH1	Output High Voltage I/O Pins: 2x Source Driver Pins - RA2, RA7-RA10, RB4, RB7, RB10, RB11, RC3-RC9	1.5	—	—	V	$I_{OH} \geq -1.9 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			2.0	—	—		$I_{OH} \geq -1.85 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			3.0	—	—		$I_{OH} \geq -1.4 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage 4x Source Driver Pins - RA0, RA1, RB0-RB3, RB5, RB6, RB8, RB9, RB12-RB15, RC0-RC2	1.5	—	—	V	$I_{OH} \geq -3.9 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			2.0	—	—		$I_{OH} \geq -3.7 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			3.0	—	—		$I_{OH} \geq -2 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
		Output High Voltage I/O Pins: 8x Source Driver Pins - RA3, RA4	1.5	—	—	V	$I_{OH} \geq -7.5 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			2.0	—	—		$I_{OH} \geq -6.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1
			3.0	—	—		$I_{OH} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ See Note 1

Note 1: Parameters are characterized, but not tested.

FIGURE 32-5: VOL – 2x DRIVER PINS**FIGURE 32-6: VOL – 4x DRIVER PINS****FIGURE 32-7: VOL – 8x DRIVER PINS****FIGURE 32-8: VOL – 16x DRIVER PINS**

Using the RCON Status Bits 87

V

Voltage Regulator (On-Chip) 339

W

Watchdog Time-out Reset (WDTR) 86

Watchdog Timer (WDT) 335, 340

 Programming Considerations 340

WWW Address..... 455

WWW, On-Line Support 9

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2007-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-62076-236-3

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.