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Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc204t-i-ml

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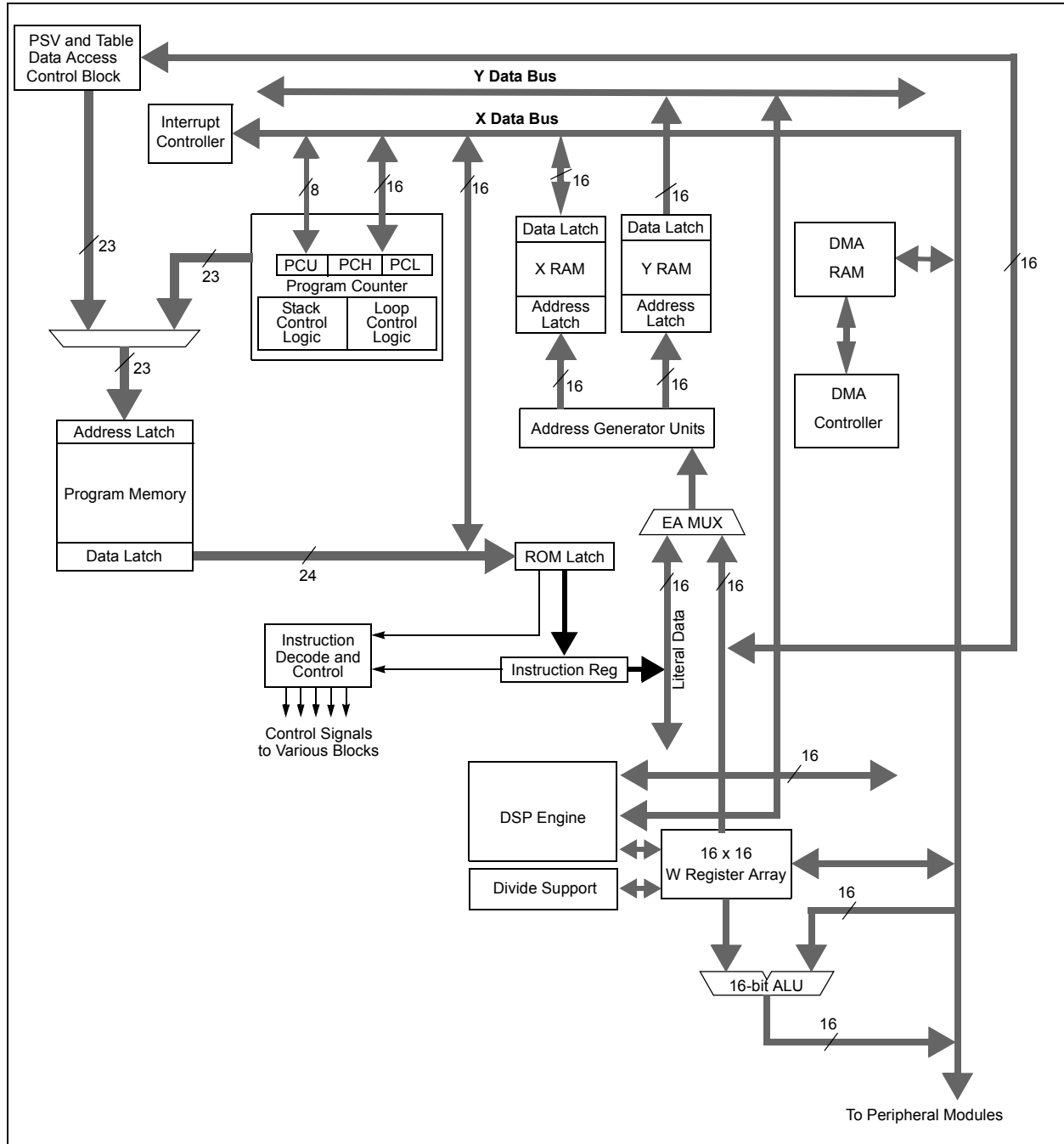To determine if an errata sheet exists for a particular device, please check with one of the following:

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FIGURE 3-1: **dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 AND dsPIC33FJ128MCX02/X04 CPU CORE BLOCK DIAGRAM**

REGISTER 3-1:   SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5   **IPL<2:0>:** CPU Interrupt Priority Level Status bits[2]

111 = CPU Interrupt Priority Level is 7 (15), user interrupts disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4   **RA:** REPEAT Loop Active bit

1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3   **N:** MCU ALU Negative bit

1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2   **OV:** MCU ALU Overflow bit

This bit is used for signed arithmetic (two's complement). It indicates an overflow of a magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1   **Z:** MCU ALU Zero bit

1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0   **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit

1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1:   This bit can be read or cleared (not set).
2:   The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
3:   The IPL<2:0> Status bits are read only when the NSTDIS bit (INTCON1<15>) = 1.
4:   This bit can be read or cleared (not set). Clearing this bit clears SA and SB.

6.9 Configuration Mismatch Reset

To maintain the integrity of the peripheral pin select control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change in any of the registers occur (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset occurs.

The Configuration Mismatch Flag bit (CM) in the Reset Control register (RCON<9>) is set to indicate the configuration mismatch Reset. Refer to **Section 11.0 "I/O Ports"** for more information on the configuration mismatch Reset.

> **Note:** The configuration mismatch feature and associated reset flag is not available on all devices.

6.10 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The Illegal Opcode or Uninitialized W Access Reset Flag bit (IOPUWR) in the Reset Control register (RCON<14>) is set to indicate the illegal condition device Reset.

6.10.0.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The illegal opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the illegal opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

6.10.0.2 UNINITIALIZED W REGISTER RESET

Any attempts to use the uninitialized W register as an address pointer will Reset the device. The W register array (with the exception of W15) is cleared during all resets and is considered uninitialized until written to.

6.10.0.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (Boot and Secure Segment), that operation will cause a security Reset.

The PFC occurs when the Program Counter is reloaded as a result of a Call, Jump, Computed Jump, Return, Return from Subroutine, or other form of branch instruction.

The VFC occurs when the Program Counter is reloaded with an Interrupt or Trap vector.

Refer to **Section 28.8 "Code Protection and CodeGuard Security"** for more information on Security Reset.

6.11 Using the RCON Status Bits

The user application can read the Reset Control register (RCON) after any device Reset to determine the cause of the reset.

> **Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 6-3 provides a summary of the Reset flag bit operation.

TABLE 6-3: RESET FLAG BIT OPERATION[1]

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR, BOR
IOPWR (RCON<14>)	Illegal opcode or uninitialized W register access or Security Reset	POR, BOR
CM (RCON<9>)	Configuration Mismatch	POR, BOR
EXTR (RCON<7>)	MCLR Reset	POR
SWR (RCON<6>)	RESET instruction	POR, BOR
WDTO (RCON<4>)	WDT time-out	PWRSAV instruction, CLRWDT instruction, POR, BOR
SLEEP (RCON<3>)	PWRSAV #SLEEP instruction	POR, BOR
IDLE (RCON<2>)	PWRSAV #IDLE instruction	POR, BOR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note 1: All Reset flag bits can be set or cleared by user software.

REGISTER 7-12: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	DMA4IE	PMPIE	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DMA3IE	C1IE[1]	C1RXIE[1]	SPI2IE	SPI2EIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DMA4IE:** DMA Channel 4 Data Transfer Complete Interrupt Enable bit

1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 13 **PMPIE:** Parallel Master Port Interrupt Enable bit

1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 12-5 **Unimplemented:** Read as '0'

bit 4 **DMA3IE:** DMA Channel 3 Data Transfer Complete Interrupt Enable bit

1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 3 **C1IE:** ECAN1 Event Interrupt Enable bit[1]

1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 2 **C1RXIE:** ECAN1 Receive Data Ready Interrupt Enable bit[1]

1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 1 **SPI2IE:** SPI2 Event Interrupt Enable bit

1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 0 **SPI2EIE:** SPI2 Error Interrupt Enable bit

1 = Interrupt request enabled
0 = Interrupt request not enabled

Note 1: Interrupts are disabled on devices without an ECAN™ module.

REGISTER 7-15:   IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T1IP<2:0>			—	OC1IP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC1IP<2:0>			—	INT0IP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **T1IP<2:0>:** Timer1 Interrupt Priority bits
                111 = Interrupt is priority 7 (highest priority interrupt)
                •
                •
                •
                001 = Interrupt is priority 1
                000 = Interrupt source is disabled

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **OC1IP<2:0>:** Output Compare Channel 1 Interrupt Priority bits
                111 = Interrupt is priority 7 (highest priority interrupt)
                •
                •
                •
                001 = Interrupt is priority 1
                000 = Interrupt source is disabled

bit 7   **Unimplemented:** Read as '0'

bit 6-4   **IC1IP<2:0>:** Input Capture Channel 1 Interrupt Priority bits
                111 = Interrupt is priority 7 (highest priority interrupt)
                •
                •
                •
                001 = Interrupt is priority 1
                000 = Interrupt source is disabled

bit 3   **Unimplemented:** Read as '0'

bit 2-0   **INT0IP<2:0>:** External Interrupt 0 Priority bits
                111 = Interrupt is priority 7 (highest priority interrupt)
                •
                •
                •
                001 = Interrupt is priority 1
                000 = Interrupt source is disabled

REGISTER 7-17: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1RXIP<2:0>			—	SPI1IP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	SPI1EIP<2:0>			—	T3IP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U1RXIP<2:0>:** UART1 Receiver Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI1IP<2:0>:** SPI1 Event Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SPI1EIP<2:0>:** SPI1 Error Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **T3IP<2:0>:** Timer3 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

The DMA controller features eight identical data transfer channels.

Each channel has its own set of control and status registers. Each DMA channel can be configured to copy data either from buffers stored in dual port DMA RAM to peripheral SFRs, or from peripheral SFRs to buffers in DMA RAM.

The DMA controller supports the following features:

• Eight DMA channels
• Register Indirect with Post-increment Addressing mode
• Register Indirect without Post-increment Addressing mode
• Peripheral Indirect Addressing mode (peripheral generates destination address)
• CPU interrupt after half or full block transfer complete

• Byte or word transfers
• Fixed priority channel arbitration
• Manual (software) or Automatic (peripheral DMA requests) transfer initiation
• One-Shot or Auto-Repeat block transfer modes
• Ping-Pong mode (automatic switch between two DPSRAM start addresses after each block transfer complete)
• DMA request for each channel can be selected from any supported interrupt source
• Debug support features

For each DMA channel, a DMA interrupt request is generated when a block transfer is complete. Alternatively, an interrupt can be generated when half of the block has been filled.

FIGURE 8-1: **TOP LEVEL SYSTEM ARCHITECTURE USING A DEDICATED TRANSACTION BUS**
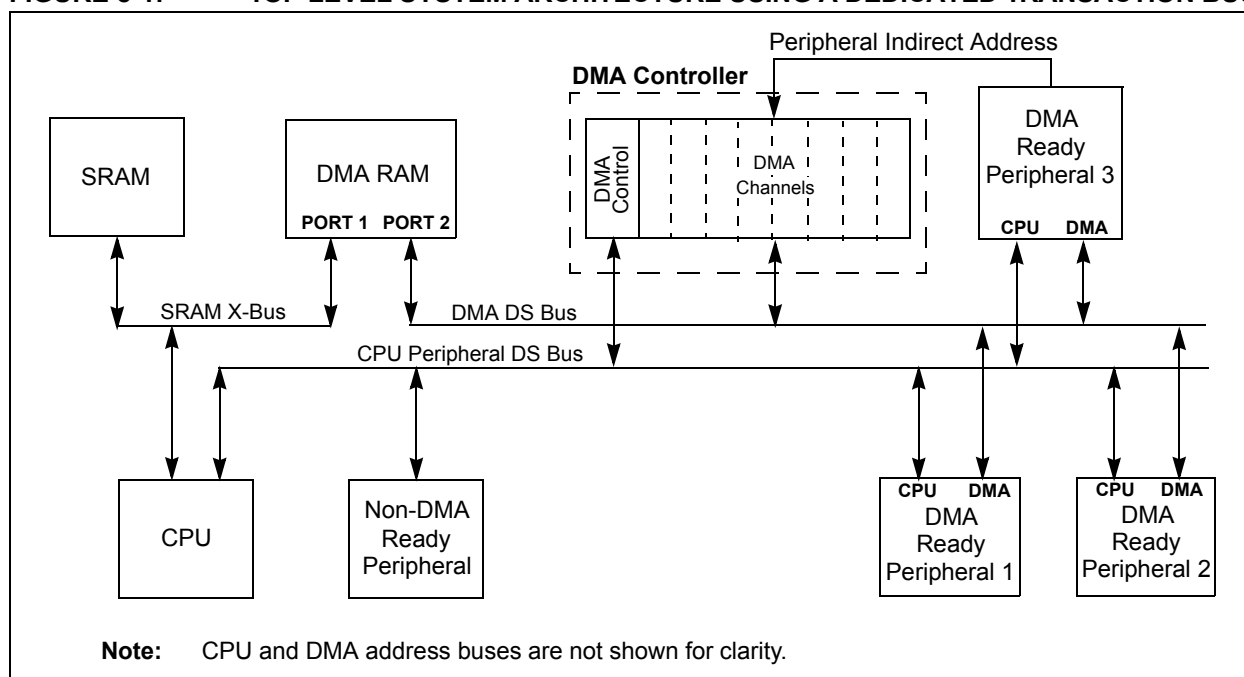
11.6.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. The dsPIC33F devices include three features to prevent alterations to the peripheral map:

• Control register lock sequence
• Continuous state monitoring
• Configuration bit pin select lock

11.6.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers;
clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) the IOLOCK bit as a single operation.

> **Note:** MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:
>
> ```
> __builtin_write_OSCCONL(value)
> __builtin_write_OSCCONH(value)
> ```
>
> See MPLAB IDE Help for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the peripheral pin selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

11.6.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset is triggered.

11.6.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY Configuration bit (FOSC<5>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the peripheral pin select registers.

REGISTER 11-10: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTERS 14

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	QEB1R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	QEA1R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13   **Unimplemented:** Read as '0'

bit 12-8   **QEB1R<4:0>:** Assign B (QEB1) to the corresponding pin

11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

bit 7-5   **Unimplemented:** Read as '0'

bit 4-0   **QEA1R<4:0>:** Assign A (QEA1) to the corresponding pin

11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

REGISTER 11-19: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SS2R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **SS2R<4:0>:** Assign SPI2 Slave Select Input ($\overline{\text{SS2}}$) to the corresponding RPn pin

11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

REGISTER 11-20: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26[1]

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	C1RXR<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **C1RXR<4:0>:** Assign ECAN1 Receive (C1RX) to the corresponding RPn pin

11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

Note 1: This register is disabled on devices without an ECAN™ module.

FIGURE 16-2: **2-CHANNEL PWM MODULE BLOCK DIAGRAM (PWM2)**
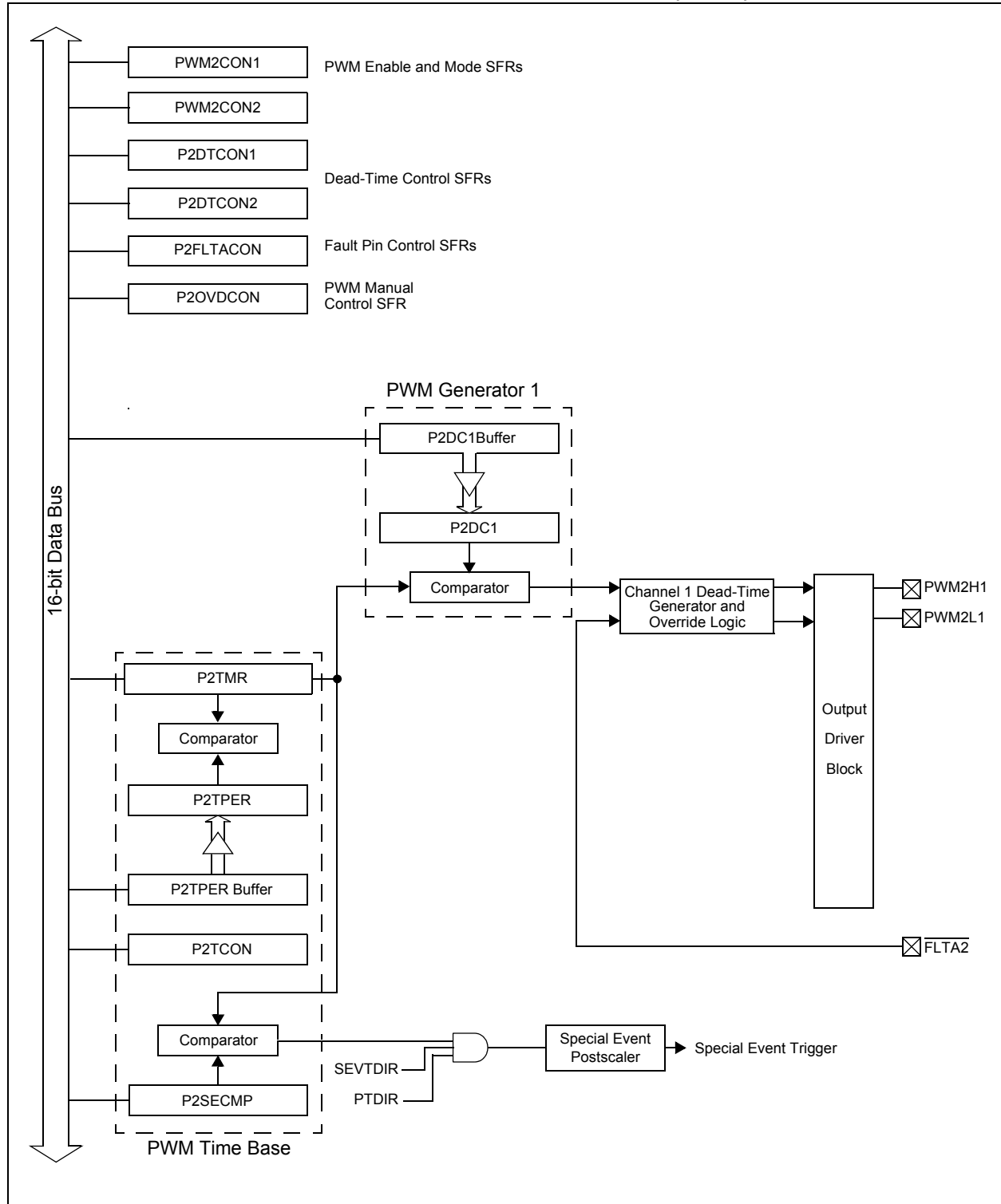
REGISTER 25-8: ALRMVAL (WHEN ALRMPTR<1:0> = 10): ALARM MONTH AND DAY VALUE REGISTER[1]

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE<3:0>			
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN<1:0>		DAYONE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13   **Unimplemented:** Read as '0'

bit 12   **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit; contains a value of 0 or 1

bit 11-8   **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit; contains a value from 0 to 9

bit 7-6   **Unimplemented:** Read as '0'

bit 5-4   **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit; contains a value from 0 to 3

bit 3-0   **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit; contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 25-9: ALRMVAL (WHEN ALRMPTR<1:0> = 01): ALARM WEEKDAY AND HOURS VALUE REGISTER[1]

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN<1:0>		HRONE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11   **Unimplemented:** Read as '0'

bit 10-8   **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit; contains a value from 0 to 6

bit 7-6   **Unimplemented:** Read as '0'

bit 5-4   **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit; contains a value from 0 to 2

bit 3-0   **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit; contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

NOTES:

27.2 PMP Control Registers

REGISTER 27-1: PMCON: PARALLEL PORT CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1[1]	ADRMUX0[1]	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP[2]	—	CS1P[2]	BEP	WRSP	RDSP
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15   **PMPEN:** Parallel Master Port Enable bit

           1 = PMP enabled
           0 = PMP disabled, no off-chip access performed

bit 14   **Unimplemented:** Read as '0'

bit 13   **PSIDL:** Stop in Idle Mode bit

           1 = Discontinue module operation when device enters Idle mode
           0 = Continue module operation in Idle mode

bit 12-11   **ADRMUX1:ADRMUX0:** Address/Data Multiplexing Selection bits[1]

           11 = Reserved
           10 = All 16 bits of address are multiplexed on PMD<7:0> pins
           01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 3 bits are multiplexed on PMA<10:8>
           00 = Address and data appear on separate pins

bit 10   **PTBEEN:** Byte Enable Port Enable bit (16-bit Master mode)

           1 = PMBE port enabled
           0 = PMBE port disabled

bit 9   **PTWREN:** Write Enable Strobe Port Enable bit

           1 = PMWR/PMENB port enabled
           0 = PMWR/PMENB port disabled

bit 8   **PTRDEN:** Read/Write Strobe Port Enable bit

           1 = PMRD/$\overline{PMWR}$ port enabled
           0 = PMRD/$\overline{PMWR}$ port disabled

bit 7-6   **CSF1:CSF0:** Chip Select Function bits

           11 = Reserved
           10 = PMCS1 functions as chip select
           0x = PMCS1 functions as address bit 14

bit 5   **ALP:** Address Latch Polarity bit[2]

           1 = Active-high (PMALL and PMALH)
           0 = Active-low (PMALL and PMALH)

bit 4   **Unimplemented:** Read as '0'

bit 3   **CS1P:** Chip Select 1 Polarity bit[2]

           1 = Active-high (PMCS1/PMCS1)
           0 = Active-low (PMCS1/PMCS1)

Note 1: 28-pin devices do not have PMA<10:2>.

      2: These bits have no effect when their corresponding pins are used as address lines.

TABLE 28-2:   dsPIC33F CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bit `11` = User program memory is not code-protected `10` = Standard security `0x` = High security
GWRP	FGS	Immediate	General Segment Write-Protect bit `1` = User program memory is not write-protected `0` = User program memory is write-protected
IESO	FOSCSEL	Immediate	Two-speed Oscillator Start-up Enable bit `1` = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready `0` = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, Immediate	Initial Oscillator Source Selection bits `111` = Internal Fast RC (FRC) oscillator with postscaler `110` = Internal Fast RC (FRC) oscillator with divide-by-16 `101` = LPRC oscillator `100` = Secondary (LP) oscillator `011` = Primary (XT, HS, EC) oscillator with PLL `010` = Primary (XT, HS, EC) oscillator `001` = Internal Fast RC (FRC) oscillator with PLL `000` = FRC oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits `1x` = Clock switching is disabled, Fail-Safe Clock Monitor is disabled `01` = Clock switching is enabled, Fail-Safe Clock Monitor is disabled `00` = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	FOSC	Immediate	Peripheral Pin Select Configuration bit `1` = Allow only one reconfiguration `0` = Allow multiple reconfigurations
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) `1` = OSC2 is clock output `0` = OSC2 is general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits `11` = Primary oscillator disabled `10` = HS Crystal Oscillator mode `01` = XT Crystal Oscillator mode `00` = EC (External Clock) mode
FWDTEN	FWDT	Immediate	Watchdog Timer Enable bit `1` = Watchdog Timer always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register has no effect.) `0` = Watchdog Timer enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	FWDT	Immediate	Watchdog Timer Window Enable bit `1` = Watchdog Timer in Non-Window mode `0` = Watchdog Timer in Window mode
WDTPRE	FWDT	Immediate	Watchdog Timer Prescaler bit `1` = 1:128 `0` = 1:32

Note 1:   This Configuration register is not available on dsPIC33FJ32MC302/304 devices.

TABLE 31-23: TIMER2 AND TIMER4 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min	Typ	Max	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or $(T_{CY} + 20)/N$	—	—	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or $(T_{CY} + 20)/N$	—	—	ns	Must also meet parameter TB15 N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or $(2 T_{CY} + 40)/N$	—	—	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		$0.75 T_{CY} + 40$	—	$1.75 T_{CY} + 40$	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 31-24: TIMER3 AND TIMER5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min	Typ	Max	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	$T_{CY} + 20$	—	—	ns	Must also meet parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	$T_{CY} + 20$	—	—	ns	Must also meet parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	$2 T_{CY} + 40$	—	—	ns	—
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		$0.75 T_{CY} + 40$	—	$1.75 T_{CY} + 40$	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

FIGURE 31-21: **SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**

Note: Refer to Figure 31-1 for load conditions.
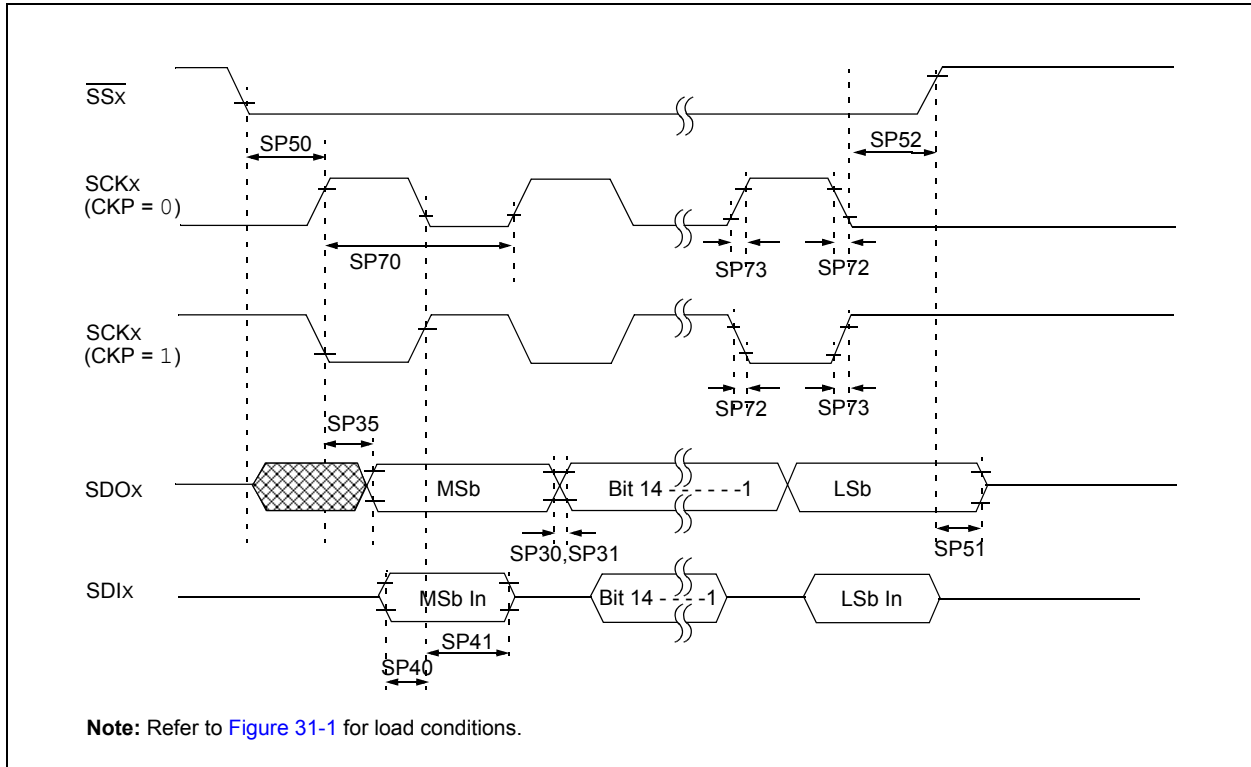
28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
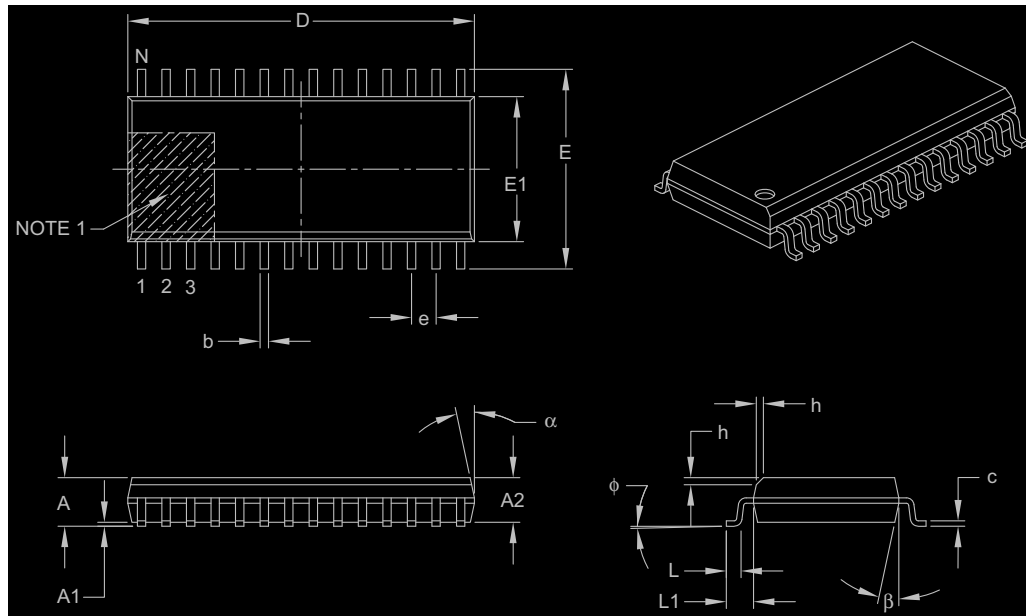
Units		MILLMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle Top	φ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B