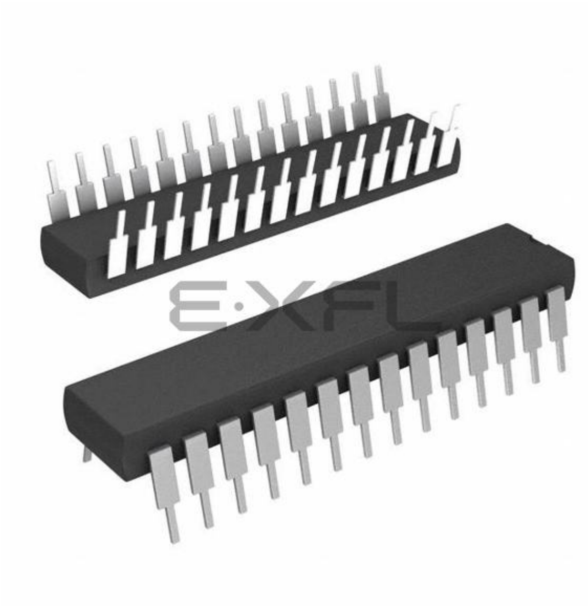
Microchip Technology - DSPIC33FJ64MC802-E/SP Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc802-e-sp

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN8	I	Analog	No	Analog input channels.
CLKI	I	ST/CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally, functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI SOSCO	I O	ST/CMOS —	No No	32.768 kHz low-power oscillator crystal input; CMOS otherwise. 32.768 kHz low-power oscillator crystal output.
CN0-CN30	I	ST	No	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1-IC2 IC7-IC8	I I	ST ST	Yes Yes	Capture inputs 1/2. Capture inputs 7/8.
OCFA OC1-OC4	I O	ST —	Yes Yes	Compare Fault A input (for Compare Channels 1, 2, 3 and 4). Compare outputs 1 through 4.
INT0 INT1 INT2	I I I	ST ST ST	No Yes Yes	External interrupt 0. External interrupt 1. External interrupt 2.
RA0-RA4 RA7-RA10	I/O I/O	ST ST	No No	PORTA is a bidirectional I/O port. PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC9	I/O	ST	No	PORTC is a bidirectional I/O port.
T1CK T2CK T3CK T4CK T5CK	I I I I I	ST ST ST ST ST	No Yes Yes Yes Yes	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input.
$\overline{\text{U1CTS}}$ $\overline{\text{U1RTS}}$ U1RX U1TX	I O I O	ST — ST —	Yes Yes Yes Yes	UART1 clear to send. UART1 ready to send. UART1 receive. UART1 transmit.
$\overline{\text{U2CTS}}$ $\overline{\text{U2RTS}}$ U2RX U2TX	I O I O	ST — ST —	Yes Yes Yes Yes	UART2 clear to send. UART2 ready to send. UART2 receive. UART2 transmit.
SCK1 SDI1 SDO1 $\overline{\text{SS1}}$	I/O I O I/O	ST ST — ST	Yes Yes Yes Yes	Synchronous serial clock input/output for SPI1. SPI1 data in. SPI1 data out. SPI1 slave synchronization or frame pulse I/O.
SCK2 SDI2 SDO2 $\overline{\text{SS2}}$	I/O I O I/O	ST ST — ST	Yes Yes Yes Yes	Synchronous serial clock input/output for SPI2. SPI2 data in. SPI2 data out. SPI2 slave synchronization or frame pulse I/O.
SCL1 SDA1 ASCL1 ASDA1	I/O I/O I/O I/O	ST ST ST ST	No No No No	Synchronous serial clock input/output for I2C1. Synchronous serial data input/output for I2C1. Alternate synchronous serial clock input/output for I2C1. Alternate synchronous serial data input/output for I2C1.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
PPS = Peripheral Pin Select
Analog = Analog input
O = Output
TTL = TTL input buffer
P = Power
I = Input

FIGURE 4-4: DATA MEMORY MAP FOR dsPIC33FJ128MC202/204 AND dsPIC33FJ64MC202/204 DEVICES WITH 8 KB RAM

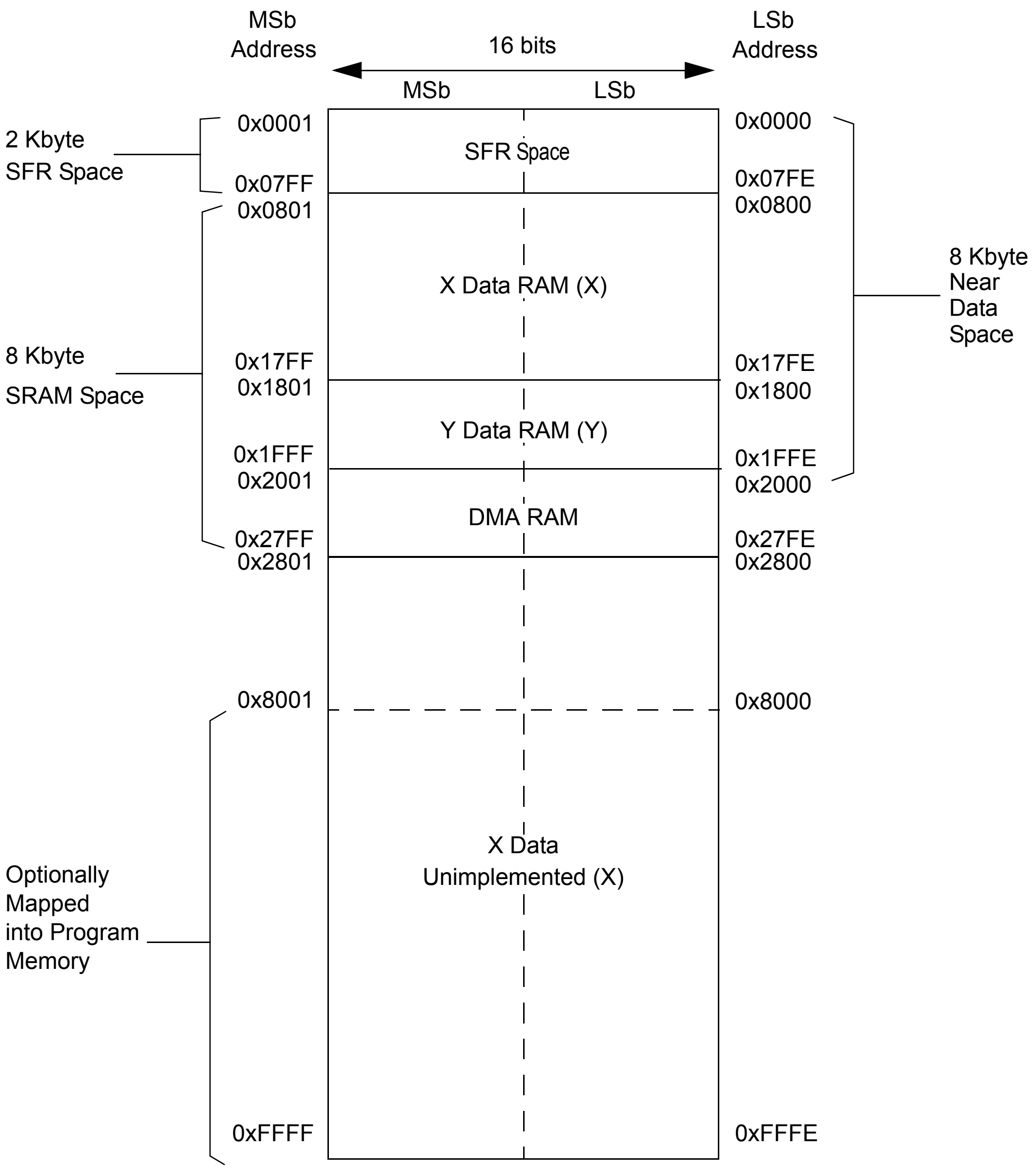


TABLE 4-1: CPU CORE REGISTERS MAP (CONTINUED)

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
MODCON	0046	XMODEN	YMODEN	—	—	BWM<3:0>				YWM<3:0>				XWM<3:0>				0000
XMODSRT	0048	XS<15:1>															0	xxxx
XMODEND	004A	XE<15:1>															1	xxxx
YMODSRT	004C	YS<15:1>															0	xxxx
YMODEND	004E	YE<15:1>															1	xxxx
XBREV	0050	BREN	XB<14:0>															xxxx
DISICNT	0052	—	—	Disable Interrupts Counter Register														xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1 (CONTINUED)

bit 2	**CMIE:** Comparator Interrupt Enable bit `1` = Interrupt request enabled `0` = Interrupt request not enabled
bit 1	**MI2C1IE:** I2C1 Master Events Interrupt Enable bit `1` = Interrupt request enabled `0` = Interrupt request not enabled
bit 0	**SI2C1IE:** I2C1 Slave Events Interrupt Enable bit `1` = Interrupt request enabled `0` = Interrupt request not enabled

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 39. "Oscillator (Part III)"** (DS70216) of the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

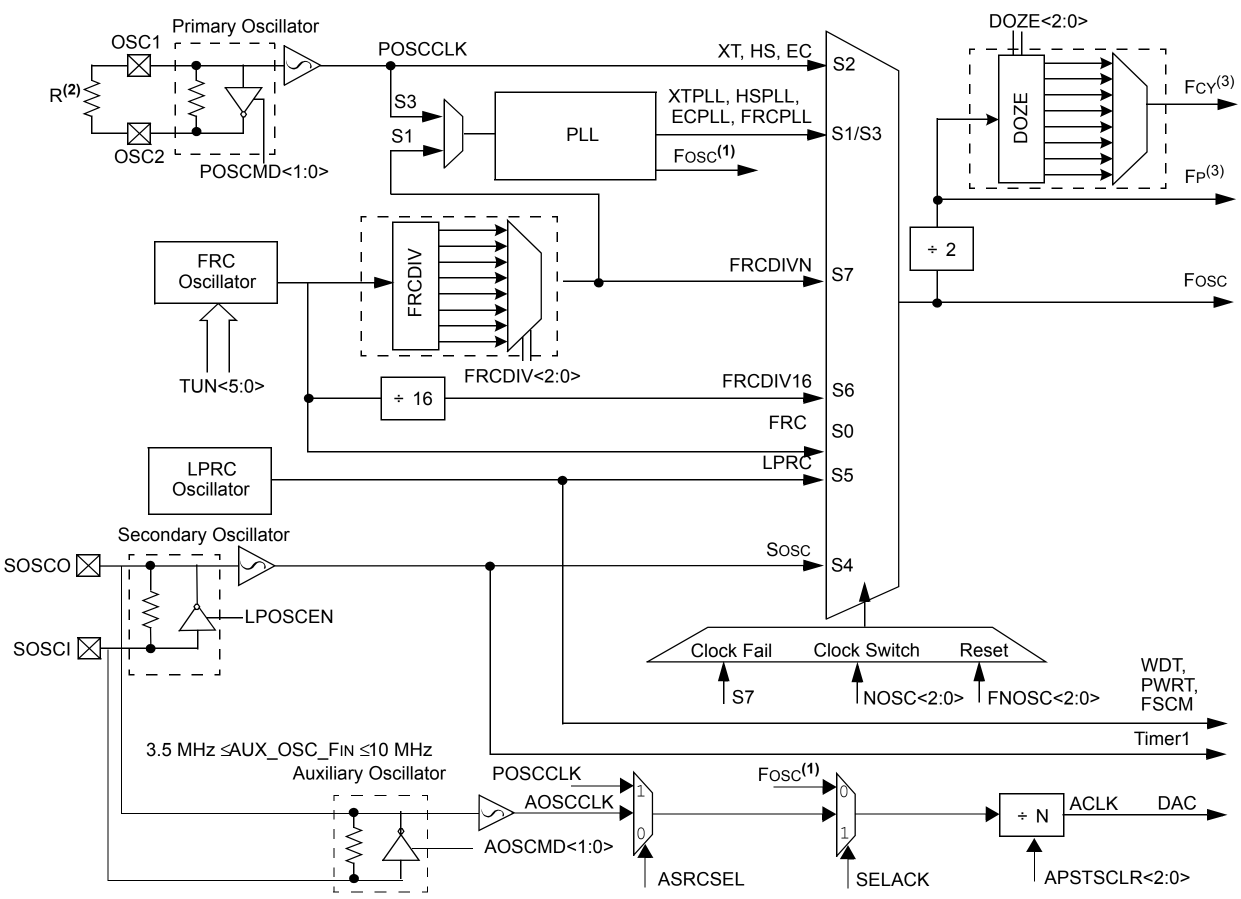
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 oscillator system provides:

- External and internal oscillator options as clock sources
- An on-chip Phase-Locked Loop (PLL) to scale the internal operating frequency to the required system clock frequency
- An internal FRC oscillator that can also be used with the PLL, thereby allowing full-speed operation without any external clock generation hardware
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- An Oscillator Control register (OSCCON)
- Non-volatile Configuration bits for main oscillator selection
- An auxiliary crystal oscillator for audio DAC

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See Figure 9-2 for PLL details.

2: If the Oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 MΩ must be connected.

3: The term FP refers to the clock source for all the peripherals, while FCY refers to the clock source for the CPU. Throughout this document FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used in any ratio other than 1:1, which is the default.

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>(2)		
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	R/W-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

Legend:	C = Clear only bit	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
111 = Fast RC (FRC) oscillator with Divide-by-n
110 = Fast RC (FRC) oscillator with Divide-by-16
101 = Low-Power RC (LPRC) oscillator
100 = Secondary Oscillator (SOSC)
011 = Primary oscillator (XT, HS, EC) with PLL
010 = Primary oscillator (XT, HS, EC)
001 = Fast RC (FRC) oscillator with divide-by-N and PLL (FRCDIVN + PLL)
000 = Fast RC (FRC) oscillator

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
111 = Fast RC (FRC) oscillator with Divide-by-n
110 = Fast RC (FRC) oscillator with Divide-by-16
101 = Low-Power RC (LPRC) oscillator
100 = Secondary Oscillator (SOSC)
011 = Primary oscillator (XT, HS, EC) with PLL
010 = Primary oscillator (XT, HS, EC)
001 = Fast RC (FRC) oscillator with divide-by-N and PLL (FRCDIVN + PLL)
000 = Fast RC (FRC) oscillator

bit 7 **CLKLOCK:** Clock Lock Enable bit
If clock switching is enabled and FSCM is disabled, (FCKSM<1:0> (FOSC<7:6>) = 0b01)
1 = Clock switching is disabled, system clock source is locked
0 = Clock switching is enabled, system clock source can be modified by clock switching

bit 6 **IOLOCK:** Peripheral Pin Select Lock bit
1 = Peripherial pin select is locked, write to peripheral pin select registers not allowed
0 = Peripherial pin select is not locked, write to peripheral pin select registers allowed

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock, or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as ‘0’

Note 1: Writes to this register require an unlock sequence. Refer to **Section 39. “Oscillator (Part III)”** (DS70216) in the *“dsPIC33F/PIC24H Family Reference Manual”* (available from the Microchip web site) for details.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

3: This register is reset only on a Power-on Reset (POR).

REGISTER 11-9: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	FLTA2R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘`0`’

bit 4-0 **FLTA2R<4:0>:** Assign PWM2 Fault ($\overline{\text{FLTA2}}$) to the corresponding RPn pin

`11111` = Input tied to Vss
`11001` = Input tied to RP25
•
•
•
`00001` = Input tied to RP1
`00000` = Input tied to RP0

REGISTER 11-19: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SS2R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘`0`’

bit 4-0 **SS2R<4:0>:** Assign SPI2 Slave Select Input ($\overline{\text{SS2}}$) to the corresponding RPn pin

`11111` = Input tied to Vss
`11001` = Input tied to RP25
•
•
•
`00001` = Input tied to RP1
`00000` = Input tied to RP0

REGISTER 11-20: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26[1]

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	C1RXR<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘`0`’

bit 4-0 **C1RXR<4:0>:** Assign ECAN1 Receive (C1RX) to the corresponding RPn pin

`11111` = Input tied to Vss
`11001` = Input tied to RP25
•
•
•
`00001` = Input tied to RP1
`00000` = Input tied to RP0

Note 1: This register is disabled on devices without an ECAN™ module.

REGISTER 16-9: PxFLTACON: FAULT A CONTROL REGISTER[1]

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
FLTAM	—	—	—	—	FAEN3	FAEN2	FAEN1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-8	**FAOVxH<3:1>:FAOVxL<3:1>:** Fault Input A PWM Override Value bits 1 = The PWM output pin is driven active on an external Fault input event 0 = The PWM output pin is driven inactive on an external Fault input event
bit 7	**FLTAM:** Fault A Mode bit 1 = The Fault A input pin functions in the Cycle-by-Cycle mode 0 = The Fault A input pin latches all control pins to the programmed states in PxFLTACON<13:8>
bit 6-3	**Unimplemented:** Read as ‘0’
bit 2	**FAEN3:** Fault Input A Enable bit 1 = PWMxH3/PWMxL3 pin pair is controlled by Fault Input A 0 = PWMxH3/PWMxL3 pin pair is not controlled by Fault Input A
bit 1	**FAEN2:** Fault Input A Enable bit 1 = PWMxH2/PWMxL2 pin pair is controlled by Fault Input A 0 = PWMxH2/PWMxL2 pin pair is not controlled by Fault Input A
bit 0	**FAEN1:** Fault Input A Enable bit 1 = PWMxH1/PWMxL1 pin pair is controlled by Fault Input A 0 = PWMxH1/PWMxL1 pin pair is not controlled by Fault Input A

Note 1: PWM2 supports only one PWM I/O pin pair.

REGISTER 21-13: CiBUFPNT2: ECAN™ FILTER 4-7 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7
`1111` = Filter hits received in RX FIFO buffer
`1110` = Filter hits received in RX Buffer 14
•
•
•
`0001` = Filter hits received in RX Buffer 1
`0000` = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 (same values as bit 15-12)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 (same values as bit 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 (same values as bit 15-12)

REGISTER 21-14: CiBUFPNT3: ECAN™ FILTER 8-11 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11
`1111` = Filter hits received in RX FIFO buffer
`1110` = Filter hits received in RX Buffer 14
•
•
•
`0001` = Filter hits received in RX Buffer 1
`0000` = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 (same values as bit 15-12)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 (same values as bit 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 (same values as bit 15-12)

BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10	**EID<5:0>:** Extended Identifier bits
bit 9	**RTR:** Remote Transmission Request bit `1` = Message will request remote transmission `0` = Normal message
bit 8	**RB1:** Reserved Bit 1 User must set this bit to ‘`0`’ per CAN protocol.
bit 7-5	**Unimplemented:** Read as ‘`0`’
bit 4	**RB0:** Reserved Bit 0 User must set this bit to ‘`0`’ per CAN protocol.
bit 3-0	**DLC<3:0>:** Data Length Code bits

BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8	**Byte 1<15:8>:** ECAN™ Message byte 0
bit 7-0	**Byte 0<7:0>:** ECAN Message byte 1

BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 7							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 6							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8	**Byte 7<15:8>:** ECAN™ Message byte 7
bit 7-0	**Byte 6<7:0>:** ECAN Message byte 6

BUFFER 21-8: ECAN™ MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	FILHIT<4:0>(1)				
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

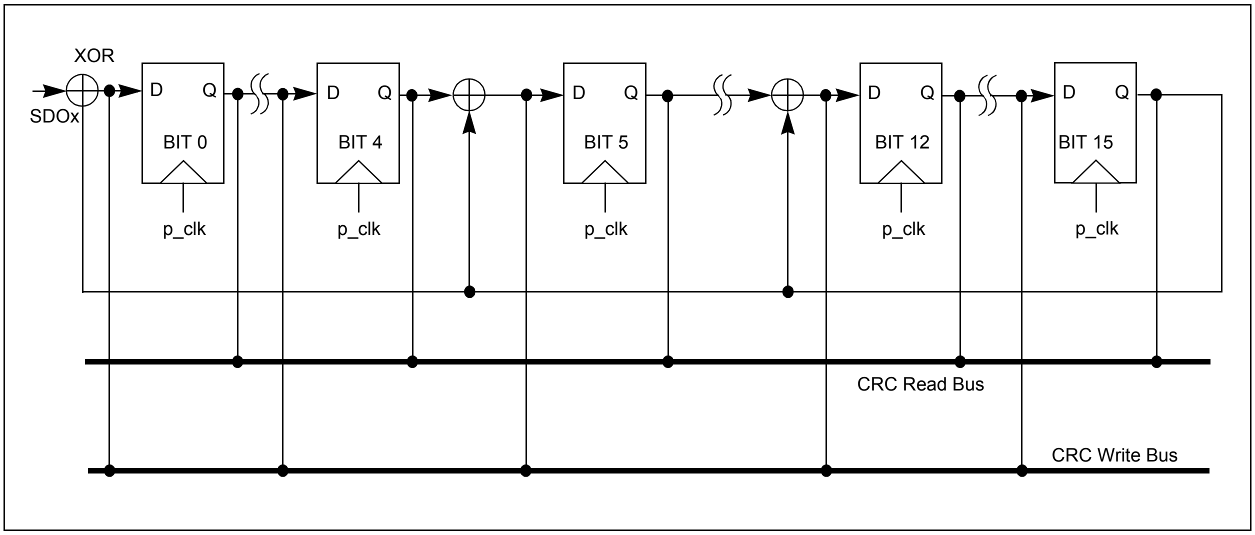
bit 15-13	**Unimplemented:** Read as ‘0’
bit 12-8	**FILHIT<4:0>:** Filter Hit Code bits(1) Encodes number of filter that resulted in writing this buffer.
bit 7-0	**Unimplemented:** Read as ‘0’

Note 1: Only written by module for receive buffers, unused for transmit buffers.

REGISTER 22-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0	**CH0SA<4:0>:** Channel 0 Positive Input Select for Sample A bits **dsPIC33FJ32MC304, dsPIC33FJ64MC204/804 and dsPIC33FJ128MC204/804 devices only:** `01000` = Channel 0 positive input is AN8 • • • `00010` = Channel 0 positive input is AN2 `00001` = Channel 0 positive input is AN1 `00000` = Channel 0 positive input is AN0 **dsPIC33FJ32MC302, dsPIC33FJ64MC202/802 and dsPIC33FJ128MC202/802 devices only:** `00101` = Channel 0 positive input is AN5 • • • `00010` = Channel 0 positive input is AN2 `00001` = Channel 0 positive input is AN1 `00000` = Channel 0 positive input is AN0

FIGURE 26-2: CRC GENERATOR RECONFIGURED FOR $x^{16} + x^{12} + x^5 + 1$



26.2 User Interface

26.2.1 DATA INTERFACE

To start serial shifting, a ‘1’ must be written to the CRCGO bit.

The module incorporates a FIFO that is 8 deep when PLEN (PLEN<3:0>) > 7, and 16 deep, otherwise. The data for which the CRC is to be calculated must first be written into the FIFO. The smallest data element that can be written into the FIFO is one byte. For example, if PLEN = 5, then the size of the data is PLEN + 1 = 6. The data must be written as follows:

```
data[5:0] = crc_input[5:0]
data[7:6] = ‘bxx
```

Once data is written into the CRCWDAT MSb (as defined by PLEN), the value of VWORD (VWORD<4:0>) increments by one. The serial shifter starts shifting data into the CRC engine when CRCGO = 1 and VWORD > 0. When the MSb is shifted out, VWORD decrements by one. The serial shifter continues shifting until the VWORD reaches 0. Therefore, for a given value of PLEN, it will take (PLEN + 1) * VWORD number of clock cycles to complete the CRC calculations.

When VWORD reaches 8 (or 16), the CRCFUL bit will be set. When VWORD reaches 0, the CRCMPT bit will be set.

To continually feed data into the CRC engine, the recommended mode of operation is to initially “prime” the FIFO with a sufficient number of words so no interrupt is generated before the next word can be written. Once that is done, start the CRC by setting the CRCGO bit to ‘1’. From that point onward, the VWORD bits should be polled. If they read less than 8 or 16, another word can be written into the FIFO.

To empty words already written into a FIFO, the CRCGO bit must be set to ‘1’ and the CRC shifter allowed to run until the CRCMPT bit is set.

Also, to get the correct CRC reading, it will be necessary to wait for the CRCMPT bit to go high before reading the CRCWDAT register.

If a word is written when the CRCFUL bit is set, the VWORD Pointer will roll over to 0. The hardware will then behave as if the FIFO is empty. However, the condition to generate an interrupt will not be met; therefore, no interrupt will be generated (See **Section 26.2.2 “Interrupt Operation”**).

At least one instruction cycle must pass after a write to CRCWDAT before a read of the VWORD bits is done.

26.2.2 INTERRUPT OPERATION

When the VWORD4:VWORD0 bits make a transition from a value of ‘1’ to ‘0’, an interrupt will be generated.

26.3 Operation in Power-Saving Modes

26.3.1 SLEEP MODE

If Sleep mode is entered while the module is operating, the module will be suspended in its current state until clock execution resumes.

26.3.2 IDLE MODE

To continue full module operation in Idle mode, the CSIDL bit must be cleared prior to entry into the mode.

If CSIDL = 1, the module will behave the same way as it does in Sleep mode; pending interrupt events will be passed on, even though the module clocks are not available.

28.2 On-Chip Voltage Regulator

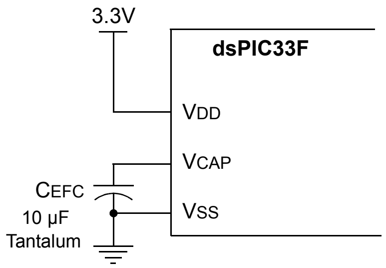
All of the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 devices power their core digital logic at a nominal 2.5V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. When the regulator is enabled, a low-ESR (less than 5 Ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 28-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 31-13 located in **Section 31.0 “Electrical Characteristics”**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

On a POR, it takes approximately 20 µs for the on-chip voltage regulator to generate an output voltage. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down.

FIGURE 28-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR(1,2,3)



Note 1: These are typical operating voltages. Refer to Table 31-13 located in **Section 31.1 “DC Characteristics”** for the full operating ranges of VDD and VCAP.

2: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

3: Typical VCAP pin voltage = 2.5V when VDD ≥ VDDMIN.

28.3 Brown-Out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is ‘`1`’.

Concurrently, the PWRT time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = `0` and a crystal oscillator is being used, then a nominal delay of TFSCM = 100 is applied. The total delay in this case is TFSCM.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit, if enabled, continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

TABLE 31-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

<table>
<tr><td colspan="3">DC CHARACTERISTICS</td><td colspan="5">Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 85°C for Industrial
-40°C ≤ TA ≤ +125°C for Extended</td></tr>
<tr><th>Param No.</th><th>Symbol</th><th>Characteristic</th><th>Min</th><th>Typ(1)</th><th>Max</th><th>Units</th><th>Conditions</th></tr>
<tr><td colspan="8">Operating Voltage</td></tr>
<tr><td rowspan="2">DC10</td><td colspan="7">Supply Voltage</td></tr>
<tr><td>VDD</td><td></td><td>3.0</td><td>—</td><td>3.6</td><td>V</td><td>Industrial and Extended</td></tr>
<tr><td>DC12</td><td>VDR</td><td>RAM Data Retention Voltage(2)</td><td>1.8</td><td>—</td><td>—</td><td>V</td><td>—</td></tr>
<tr><td>DC16</td><td>VPOR</td><td>VDD Start Voltage
to ensure internal Power-on Reset signal</td><td>—</td><td>—</td><td>VSS</td><td>V</td><td>—</td></tr>
<tr><td>DC17</td><td>SVDD</td><td>VDD Rise Rate
to ensure internal Power-on Reset signal</td><td>0.03</td><td>—</td><td>—</td><td>V/ms</td><td>0-3.0V in 0.1s</td></tr>
</table>

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

TABLE 31-38: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP70	TscP	Maximum SCK Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{\text{SSx}}$ ↓to SCKx ↑ or SCKx Input	120	—	—	ns	—
SP51	TssH2doZ	$\overline{\text{SSx}}$ ↑ to SDOx Output High-Impedance(4)	10	—	50	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{\text{SSx}}$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCK clock generated by the Master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 31-47: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	76	—	—	ns	—
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	—
Conversion Rate							
AD55	tCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate	—	—	1.1	Msps	—
AD57	TSAMP	Sample Time	2 TAD	—	—	—	—
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(1)	2 TAD	—	3 TAD	—	Auto-Convert Trigger not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(1)	2 TAD	—	3 TAD	—	—
AD62	tCSS	Conversion Completion to Sample Start (ASAM = `1`)(1)	—	0.5 TAD	—	—	—
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(1)	—	—	20	µs	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

3: The tDPU is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (AD1CON1<ADON>='1'). During this time, the ADC result is indeterminate.

TABLE 31-48: AUDIO DAC MODULE SPECIFICATIONS

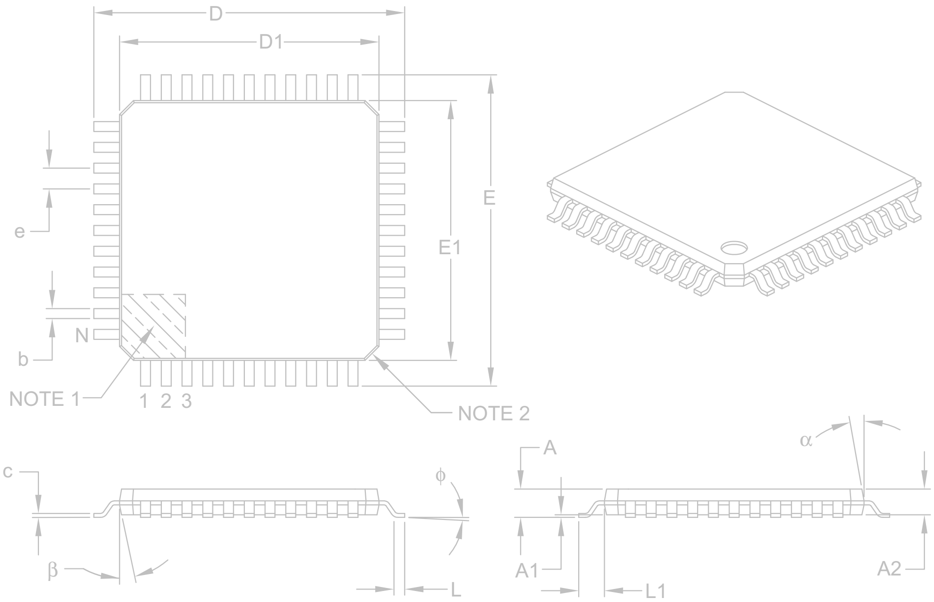
AC/DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Clock Parameters							
DA01	VOD+	Positive Output Differential Voltage	1	1.15	2	V	VOD+ = VDACH - VDACL See **Note 1,2**
DA02	VOD-	Negative Output Differential Voltage	-2	-1.15	-1	V	VOD- = VDACL - VDACH See **Note 1,2**
DA03	VRES	Resolution	—	16	—	bits	—
DA04	GERR	Gain Error	—	3.1	—	%	—
DA08	FDAC	Clock frequency	—	—	25.6	MHz	—
DA09	FSAMP	Sample Rate	0	—	100	kHz	—
DA10	FINPUT	Input data frequency	0	—	45	kHz	Sampling frequency = 100 kHz
DA11	TINIT	Initialization period	1024	—	—	Clks	Time before first sample
DA12	SNR	Signal-to-Noise Ratio	—	61		dB	Sampling frequency = 96 kHz

Note 1: Measured VDACH and VDACL output with respect to VSS, with 15 µA load and FORM bit (DACxCON<8>) = `0`.

2: This parameter is tested at -40°C ≤ TA ≤ +85°C only.

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

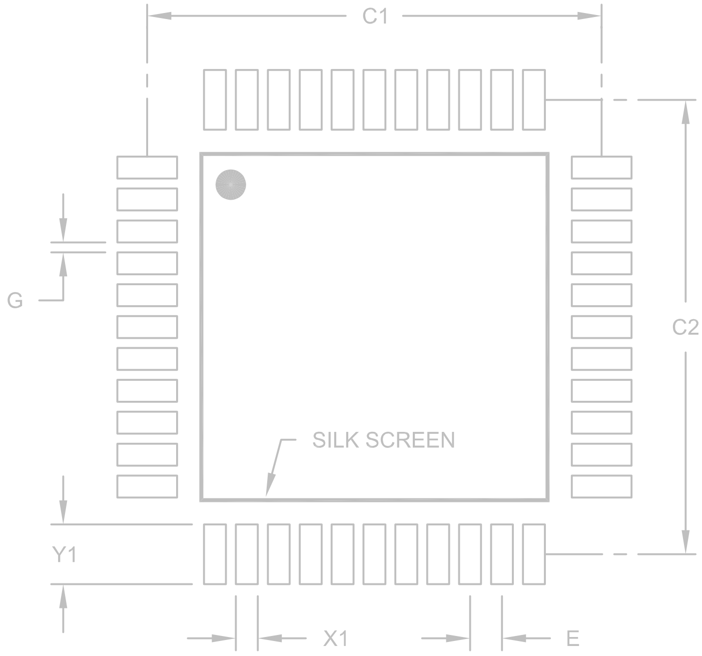
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076A