



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

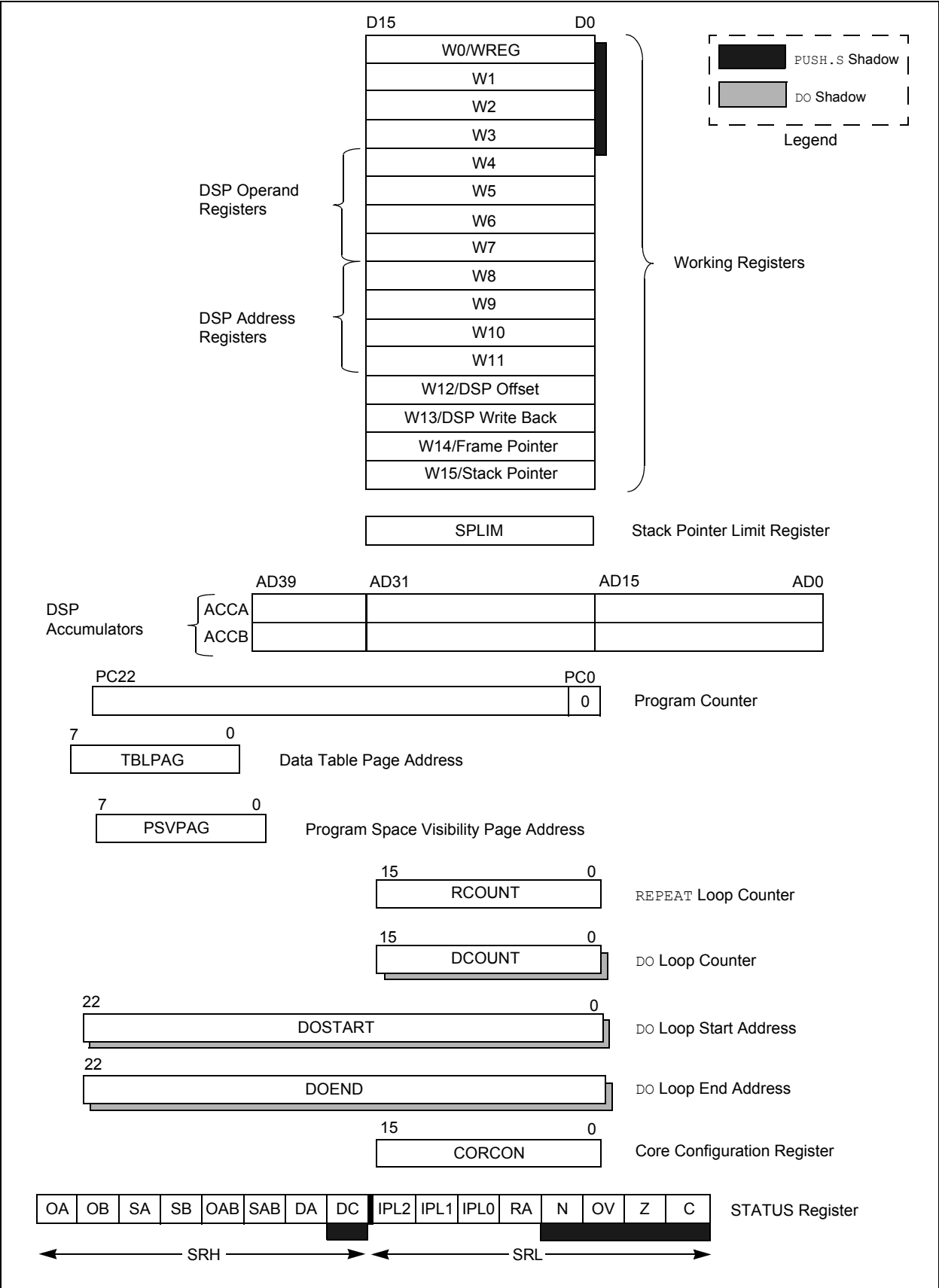
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc802-i-so

FIGURE 3-2: dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 AND dsPIC33FJ128MCX02/X04 PROGRAMMER'S MODEL



4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTERS MAP

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
WREG0	0000	Working Register 0																0000	
WREG1	0002	Working Register 1																0000	
WREG2	0004	Working Register 2																0000	
WREG3	0006	Working Register 3																0000	
WREG4	0008	Working Register 4																0000	
WREG5	000A	Working Register 5																0000	
WREG6	000C	Working Register 6																0000	
WREG7	000E	Working Register 7																0000	
WREG8	0010	Working Register 8																0000	
WREG9	0012	Working Register 9																0000	
WREG10	0014	Working Register 10																0000	
WREG11	0016	Working Register 11																0000	
WREG12	0018	Working Register 12																0000	
WREG13	001A	Working Register 13																0000	
WREG14	001C	Working Register 14																0000	
WREG15	001E	Working Register 15																0800	
SPLIM	0020	Stack Pointer Limit Register																xxxx	
ACCAL	0022	ACCAL																xxxx	
ACCAH	0024	ACCAH																xxxx	
ACCAU	0026	ACCA<39>									ACCAU							xxxx	
ACCBL	0028	ACCBL																xxxx	
ACCBH	002A	ACCBH																xxxx	
ACCBU	002C	ACCB<39>									ACCBU							xxxx	
PCL	002E	Program Counter Low Word Register																xxxx	
PCH	0030	—	—	—	—	—	—	—	—	Program Counter High Byte Register									0000
TBLPAG	0032	—	—	—	—	—	—	—	—	Table Page Address Pointer Register									0000
PSVPAG	0034	—	—	—	—	—	—	—	—	Program Memory Visibility Page Address Pointer Register									0000
RCOUNT	0036	Repeat Loop Counter Register																xxxx	
DCOUNT	0038	DCOUNT<15:0>																xxxx	
DOSTARTL	003A	DOSTARTL<15:1>															0	xxxx	
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						00xx	
DOENDL	003E	DOENDL<15:1>															0	xxxx	
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>						00xx	
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	—	—	—	US	EDT	DL<2:0>			SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF	0020	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.8.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access to stored constant data from the data space without the need to use special instructions (such as `TBLRDH`).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and program space visibility is enabled by setting the PSV bit in the Core Control register (`CORCON<2>`). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (`PSVPAG`). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, `PSVPAG` functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add a cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address 0x8000 and higher maps directly into a corresponding program memory address (see [Figure 4-11](#)), only the lower 16 bits of the

24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '1111 1111' or '0000 0000' to force a `NOB`. This prevents possible issues should the area of code ever be accidentally executed.

Note: PSV access is temporarily disabled during table reads/writes.

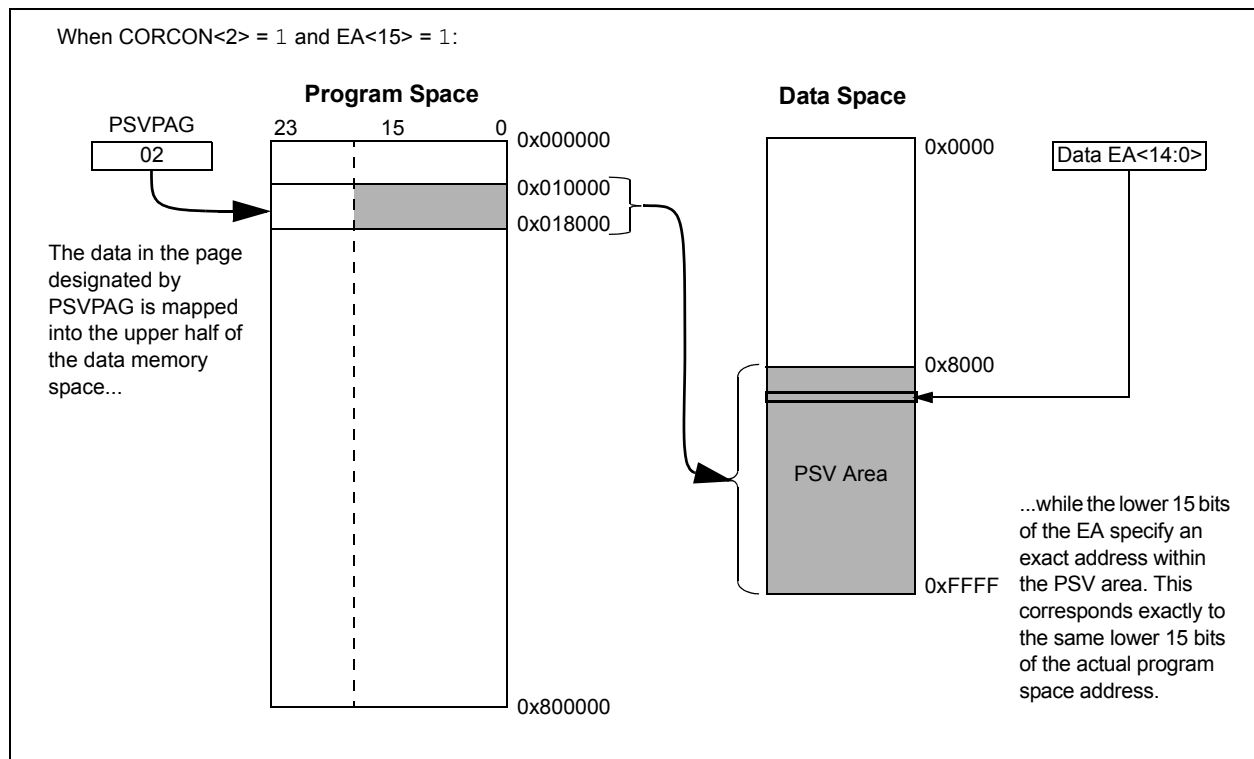
For operations that use PSV and are executed outside a `REPEAT` loop, the `MOV` and `MOV.D` instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV, and are executed inside a `REPEAT` loop, these instances require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the `REPEAT` loop allows the instruction using PSV to access data, to execute in a single cycle.

FIGURE 4-11: PROGRAM SPACE VISIBILITY OPERATION



5.2 RTSP Operation

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (512 instructions) at a time, and to program one row or one word at a time. Table 31-12 shows typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

The program memory implements holding buffers that can contain 64 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 64 TBLWTL and TBLWTH instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 31-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time, and Word Write Cycle Time parameters (see Table 31-12).

EQUATION 5-1: PROGRAMMING TIME

$$T = \frac{11064 \text{ Cycles}}{7.37 \text{ MHz} \times (\text{FRC Accuracy})\% \times (\text{FRC Tuning})\%}$$

For example, if the device is operating at +125°C, the FRC accuracy will be ±5%. If the TUN<5:0> bits (see Register 9-4) are set to 'b111111, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \text{ Cycles}}{7.37 \text{ MHz} \times (1 + 0.05) \times (1 - 0.00375)} = 1.435 \text{ ms}$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064 \text{ Cycles}}{7.37 \text{ MHz} \times (1 - 0.05) \times (1 - 0.00375)} = 1.586 \text{ ms}$$

Setting the WR bit (NVMCON<15>) starts the operation, and the WR bit is automatically cleared when the operation is finished.

5.4 Control Registers

Two SFRs are used to read and write the program Flash memory:

- NVMCON: The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.
- NVMKEY: NVMKEY (Register 5-2) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to Section 5.3 “Programming Operations” for further details.

5.5 Flash Programming Resources

Many useful resources related to Flash programming are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315>

5.5.1 KEY RESOURCES

- Section 5. “Flash Programming” (DS70191)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

7.3 Interrupt Control and Status Registers

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 devices implement a total of 30 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFSx
- IECx
- IPCx
- INTTREG

7.3.1 INTCON1 AND INTCON2

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS) as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table (AIVT).

7.3.2 IFSx

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.3.3 IECx

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.3.4 IPCx

The IPC registers are used to set the interrupt priority level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.3.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU interrupt priority level, which are latched into vector number bits (VECNUM<6:0>) and Interrupt level bits (ILR<3:0>) in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in [Table 7-1](#). For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0>, and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

7.3.6 STATUS/CONTROL REGISTERS

Although they are not specifically part of the interrupt control hardware, two of the CPU control registers contain bits that control interrupt functionality.

- The CPU Status register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU interrupt priority level. The user software can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU priority level. The IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in [Register 7-1](#) through [Register 7-32](#).

7.4 Interrupts Resources

Many useful resources related to Interrupts are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](#), contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315>

7.4.1 KEY RESOURCES

- **Section 32. “Interrupts (Part III)”** (DS70214)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

REGISTER 7-8: IFS3: INTERRUPT FLAG STATUS REGISTER 3

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0
FLTA1IF	RTCIF	DMA5IF	—	—	QE11IF	PWM1IF	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **FLTA1IF:** PWM1 Fault A Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 14 **RTCIF:** Real-Time Clock and Calendar Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 13 **DMA5IF:** DMA Channel 5 Data Transfer Complete Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10 **QE11IF:** QE11 Event Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 9 **PWM1IF:** PWM1 Event Interrupt Flag Status bit
 1 = Interrupt request has occurred
 0 = Interrupt request has not occurred
- bit 8-0 **Unimplemented:** Read as '0'

8.0 DIRECT MEMORY ACCESS (DMA)

Note 1: This data sheet summarizes the features of the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 38. “Direct Memory Access (DMA) (Part III)”** (DS70215) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

Direct Memory Access (DMA) is a very efficient mechanism of copying data between peripheral SFRs (e.g., UART Receive register, Input Capture 1 buffer), and buffers or variables stored in RAM, with minimal CPU intervention. The DMA controller can automatically copy entire blocks of data without requiring the user software to read or write the peripheral Special Function Registers (SFRs) every time a peripheral interrupt occurs. The DMA controller uses a dedicated bus for data transfers and therefore, does not steal cycles from the code execution flow of the CPU. To exploit the DMA capability, the corresponding user buffers or variables must be located in DMA RAM.

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 peripherals that can utilize DMA are listed in [Table 8-1](#).

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<6:0> Bits	DMAxPAD Register Values to Read From Peripheral	DMAxPAD Register Values to Write to Peripheral
INT0 – External Interrupt 0	0000000	—	—
IC1 – Input Capture 1	0000001	0x0140 (IC1BUF)	—
OC1 – Output Compare 1 Data	0000010	—	0x0182 (OC1R)
OC1 – Output Compare 1 Secondary Data	0000010	—	0x0180 (OC1RS)
IC2 – Input Capture 2	0000101	0x0144 (IC2BUF)	—
OC2 – Output Compare 2 Data	0000110	—	0x0188 (OC2R)
OC2 – Output Compare 2 Secondary Data	0000110	—	0x0186 (OC2RS)
TMR2 – Timer2	0000111	—	—
TMR3 – Timer3	0001000	—	—
SPI1 – Transfer Done	0001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
UART1RX – UART1 Receiver	0001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	0001100	—	0x0224 (U1TXREG)
ADC1 – ADC1 Convert Done	0001101	0x0300 (ADC1BUF0)	—
UART2RX – UART2 Receiver	0011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	0011111	—	0x0234 (U2TXREG)
SPI2 – Transfer Done	0100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
ECAN1 – RX Data Ready	0100010	0x0440 (C1RXD)	—
PMP - Master Data Transfer	0101101	0x0608 (PMDIN1)	0x0608 (PMDIN1)
ECAN1 – TX Data Request	1000110	—	0x0442 (C1TXD)
DAC1 - Right Data Output	1001110	—	0x3F6 (DAC1RDAT)
DAC2 - Left Data Output	1001111	—	0x03F8 (DAC1LDAT)

12.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. “Timers”** (DS70205) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the real-time clock, or operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated from the low power 32 kHz crystal oscillator available on the device.
- Can be operated in Asynchronous Counter mode from an external clock source.
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler.

The unique features of Timer1 allow it to be used for Real-Time Clock (RTC) applications. A block diagram of Timer1 is shown in [Figure 12-1](#).

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

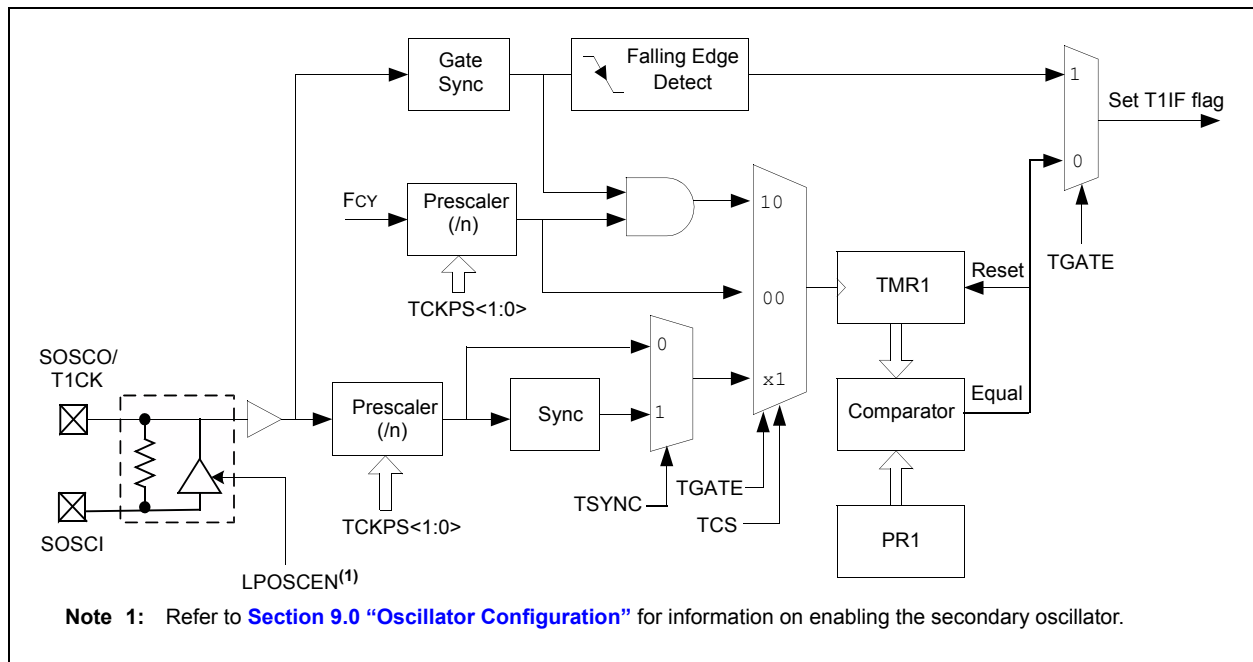
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the [Table 12-1](#).

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



REGISTER 13-2: TyCON: TIMER CONTROL REGISTER (y = 3 or 5)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽²⁾	—	TSIDL ⁽¹⁾	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE ⁽²⁾	TCKPS<1:0> ⁽²⁾		—	—	TCS ⁽²⁾	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TON:** Timery On bit⁽²⁾

1 = Starts 16-bit Timerx

0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit⁽¹⁾

1 = Discontinue timer operation when device enters Idle mode

0 = Continue timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit⁽²⁾

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation enabled

0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits⁽²⁾

11 = 1:256 prescale value

10 = 1:64 prescale value

01 = 1:8 prescale value

00 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit⁽²⁾

1 = External clock from TxCK pin

0 = Internal clock (Fosc/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

2: When the 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), these bits have no effect.

15.2 Output Compare Resources

Many useful resources related to Output Compare are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this [link](http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315), contains the latest updates and additional information.

<p>Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en532315</p>
--

15.2.1 KEY RESOURCES

- **Section 13. “Output Compare”** (DS70209)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

NOTES:

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

Legend:	C = Clear only bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HS = Set in hardware	HSC = Hardware set/cleared
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.
- bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.
- bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.
- bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.
- bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

REGISTER 21-11: CIfEN1: ECAN™ ACCEPTANCE FILTER ENABLE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **FLTENN**: Enable Filter n to Accept Messages bits

1 = Enable Filter n

0 = Disable Filter n

REGISTER 21-12: CIBUFPNT1: ECAN™ FILTER 0-3 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F3BP<3:0>**: RX Buffer mask for Filter 3
 1111 = Filter hits received in RX FIFO buffer
 1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>**: RX Buffer mask for Filter 2 (same values as bit 15-12)

bit 7-4 **F1BP<3:0>**: RX Buffer mask for Filter 1 (same values as bit 15-12)

bit 3-0 **F0BP<3:0>**: RX Buffer mask for Filter 0 (same values as bit 15-12)

REGISTER 22-3: AD1CON3: ADC1 CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC<4:0> ⁽¹⁾				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS<7:0> ⁽²⁾							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADRC:** ADC Conversion Clock Source bit

1 = ADC internal RC clock

0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto Sample Time bits⁽¹⁾

11111 = 31 TAD

•

•

•

00001 = 1 TAD

00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits⁽²⁾

11111111 = Reserved

•

•

•

•

01000000 = Reserved

00111111 = $T_{CY} \cdot (ADCS<7:0> + 1) = 64 \cdot T_{CY} = T_{AD}$

•

•

•

00000010 = $T_{CY} \cdot (ADCS<7:0> + 1) = 3 \cdot T_{CY} = T_{AD}$

00000001 = $T_{CY} \cdot (ADCS<7:0> + 1) = 2 \cdot T_{CY} = T_{AD}$

00000000 = $T_{CY} \cdot (ADCS<7:0> + 1) = 1 \cdot T_{CY} = T_{AD}$

Note 1: These bits are only used if AD1CON1<7:5> (SSRC<2:0>) = 111.

2: This bit is not used if AD1CON3<15> (ADRC) = 1.

REGISTER 24-2: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR	CVRSS	CVR<3:0>			
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit

1 = CVREF circuit powered on

0 = CVREF circuit powered down

bit 6 **CVROE:** Comparator VREF Output Enable bit

1 = CVREF voltage level is output on CVREF pin

0 = CVREF voltage level is disconnected from CVREF pin

bit 5 **CVRR:** Comparator VREF Range Selection bit

1 = CVRSRC range should be 0 to 0.625 CVRSRC with CVRSRC/24 step size

0 = CVRSRC range should be 0.25 to 0.719 CVRSRC with CVRSRC/32 step size

bit 4 **CVRSS:** Comparator VREF Source Selection bit

1 = Comparator reference source CVRSRC = VREF+ – VREF-

0 = Comparator reference source CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>:** Comparator VREF Value Selection $0 \leq \text{CVR<3:0>} \leq 15$ bits

When CVRR = 1:

$$CV_{REF} = (\text{CVR<3:0>} / 24) \cdot (CV_{RSRC})$$

When CVRR = 0:

$$CV_{REF} = 1/4 \cdot (CV_{RSRC}) + (\text{CVR<3:0>} / 32) \cdot (CV_{RSRC})$$

FIGURE 31-6: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS

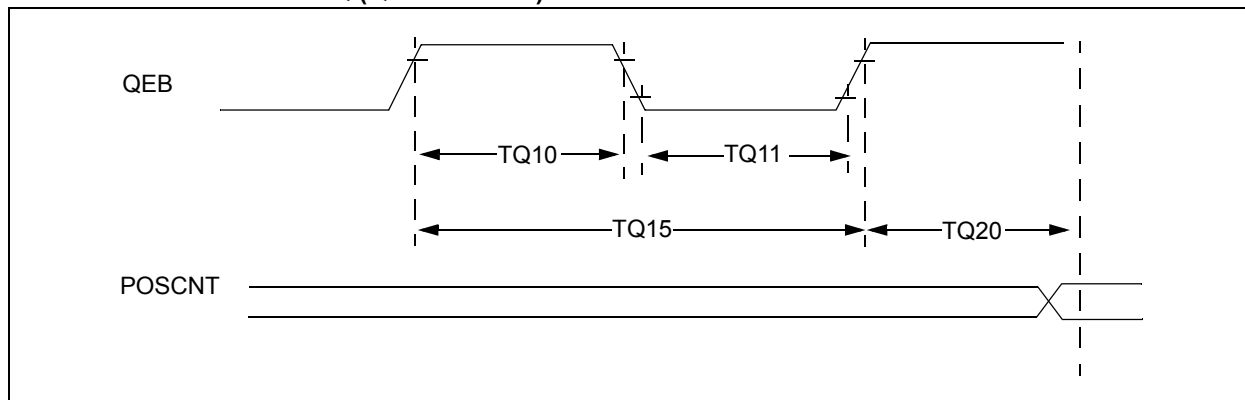


TABLE 31-25: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min	Typ	Max	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Tcy + 20		—	ns	Must also meet parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Tcy + 20		—	ns	Must also meet parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	2 * Tcy + 40		—	ns	—
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.5 Tcy		1.5 Tcy	—	—

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 31-19: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

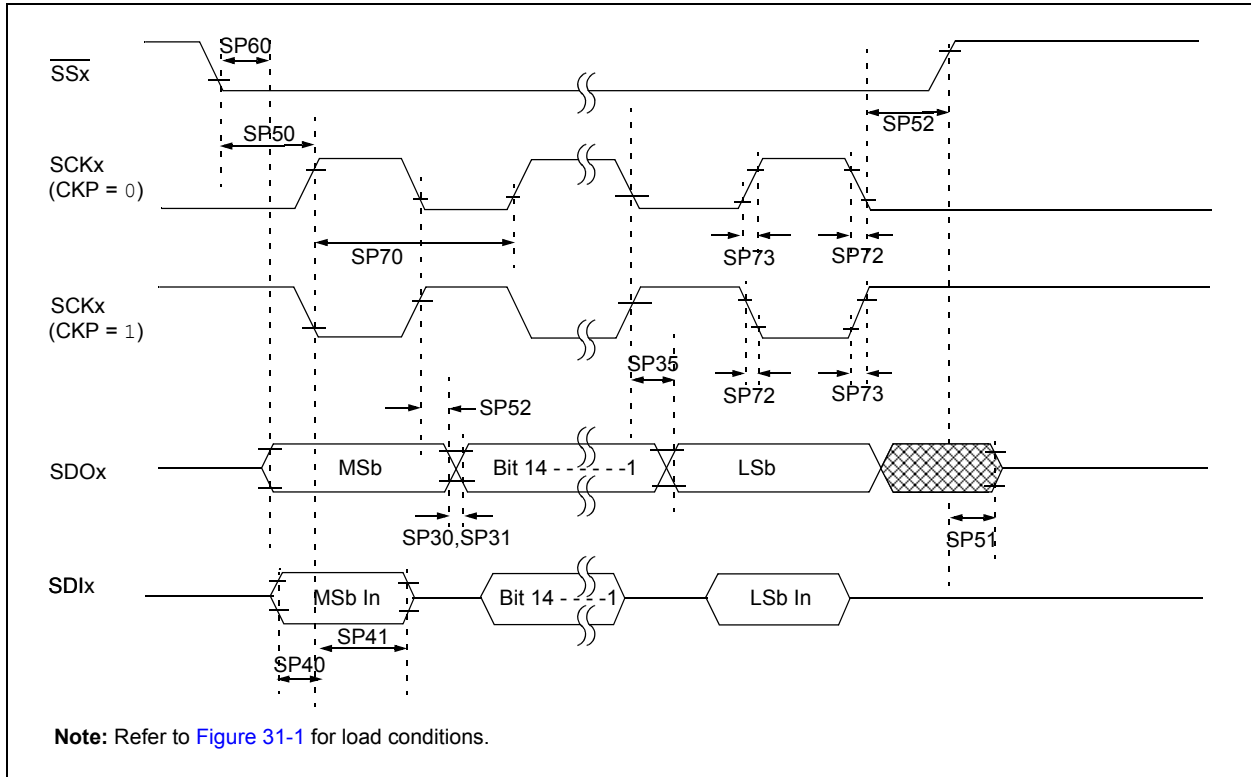


FIGURE 31-26: ECAN MODULE I/O TIMING CHARACTERISTICS

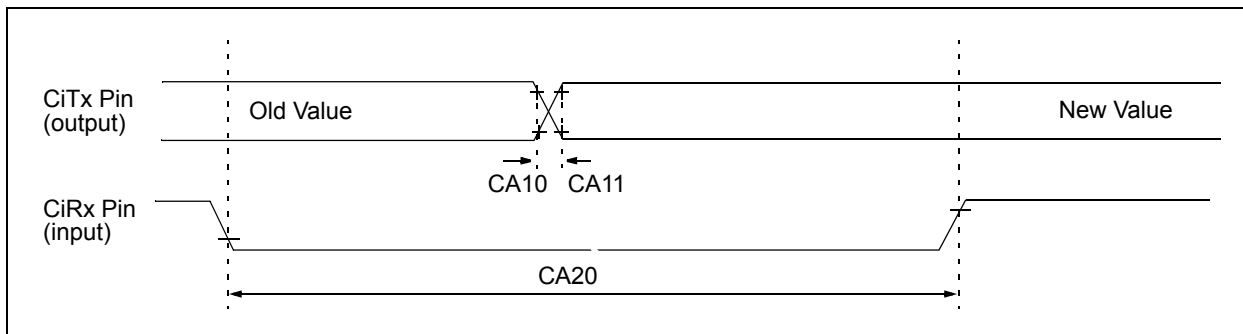


TABLE 31-42: ECAN MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter D032
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter D031
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	120	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

NOTES:

Operation Example	65	AD1CON1 (ADC1 Control 1)	286
Start and End Address	65	AD1CON2 (ADC1 Control 2)	288
W Address Register Selection	65	AD1CON3 (ADC1 Control 3)	289
Motor Control PWM	213	AD1CON4 (ADC1 Control 4)	290
Motor Control PWM Module		AD1CSSL (ADC1 Input Scan Select Low)	295
2-Output Register Map	48	AD1PCFGL (ADC1 Port Configuration Low)	295
6-Output Register Map	47	CIUFNT1 (ECAN Filter 0-3 Buffer Pointer)	267
MPLAB ASM30 Assembler, Linker, Librarian	354	CIUFNT2 (ECAN Filter 4-7 Buffer Pointer)	268
MPLAB Integrated Development Environment Software	353	CIUFNT3 (ECAN Filter 8-11 Buffer Pointer)	268
MPLAB PM3 Device Programmer	356	CIUFNT4 (ECAN Filter 12-15 Buffer Pointer)	269
MPLAB REAL ICE In-Circuit Emulator System	355	CIUFG1 (ECAN Baud Rate Configuration 1)	265
MPLINK Object Linker/MPLIB Object Librarian	354	CIUFG2 (ECAN Baud Rate Configuration 2)	266
N		CICTRL1 (ECAN Control 1)	258
NVM Module		CICTRL2 (ECAN Control 2)	259
Register Map	62	CIIEC (ECAN Transmit/Receive Error Count)	265
O		CIUFCR (ECAN FIFO Control)	261
Open-Drain Configuration	164	CIUFEN1 (ECAN Acceptance Filter Enable)	267
Output Compare	209	CIUFIFO (ECAN FIFO Status)	262
P		CIUFMSKSEL1 (ECAN Filter 7-0 Mask Selection)	271, 272
Packaging	429	CIINTE (ECAN Interrupt Enable)	264
Details	430	CIINTF (ECAN Interrupt Flag)	263
Marking	429	CIURFnEID (ECAN Acceptance Filter n Extended Identifier)	271
Peripheral Module Disable (PMD)	156	CIURFnSID (ECAN Acceptance Filter n Standard Identifier)	270
Pinout I/O Descriptions (table)	13	CIURFUL1 (ECAN Receive Buffer Full 1)	274
PMD Module		CIURFUL2 (ECAN Receive Buffer Full 2)	274
Register Map	62	CIURMnEID (ECAN Acceptance Filter Mask n Extended Identifier)	273
PORTA		CIURMnSID (ECAN Acceptance Filter Mask n Standard Identifier)	273
Register Map	60, 61	CIURXOVF1 (ECAN Receive Buffer Overflow 1)	275
PORTB		CIURXOVF2 (ECAN Receive Buffer Overflow 2)	275
Register Map	61	CIURBnSID (ECAN Buffer n Standard Identifier)	277, 278, 280
Power-on Reset (POR)	85	CIURmCON (ECAN TX/RX Buffer m Control)	276
Power-Saving Features	155	CIUEC (ECAN Interrupt Code)	260
Clock Frequency and Switching	155	CLKDIV (Clock Divisor)	149
Program Address Space	35	CORCON (Core Control)	28, 94
Construction	68	DFLTCON (QEI Control)	231
Data Access from Program Memory Using Program Space Visibility	71	DMACS0 (DMA Controller Status 0)	138
Data Access from Program Memory Using Table Instructions	70	DMACS1 (DMA Controller Status 1)	140
Data Access from, Address Generation	69	DMAxCNT (DMA Channel x Transfer Count)	137
Memory Map	35	DMAxCON (DMA Channel x Control)	134
Table Read Instructions		DMAxPAD (DMA Channel x Peripheral Address)	137
TBLRDH	70	DMAxREQ (DMA Channel x IRQ Select)	135
TBLRDL	70	DMAxSTA (DMA Channel x RAM Start Address A) .	136
Visibility Operation	71	DMAxSTB (DMA Channel x RAM Start Address B) .	136
Program Memory		DSADR (Most Recent DMA RAM Address)	141
Interrupt Vector	36	I2CxCON (I2Cx Control)	242
Organization	36	I2CxMSK (I2Cx Slave Mode Address Mask)	246
Reset Vector	36	I2CxSTAT (I2Cx Status)	244
Q		IFS0 (Interrupt Flag Status 0)	98, 105
Quadrature Encoder Interface (QEI)	227	IFS1 (Interrupt Flag Status 1)	100, 107
Quadrature Encoder Interface (QEI) Module		IFS2 (Interrupt Flag Status 2)	102, 109
Register Map	48	IFS3 (Interrupt Flag Status 3)	103, 110
R		IFS4 (Interrupt Flag Status 4)	104, 111
Reader Response	456	INTCON1 (Interrupt Control 1)	95
Register Map		INTCON2 (Interrupt Control 2)	97
CRC	60	INTREG Interrupt Control and Status Register	129
Dual Comparator	60	IPC0 (Interrupt Priority Control 0)	112
Parallel Master/Slave Port	59	IPC1 (Interrupt Priority Control 1)	113
Real-Time Clock and Calendar	60	IPC11 (Interrupt Priority Control 11)	122
Registers		IPC14 (Interrupt Priority Control 14)	123
AD1CHS0 (ADC1 Input Channel 0 Select)	293	IPC15 (Interrupt Priority Control 15)	124
AD1CHS123 (ADC1 Input Channel 1, 2, 3 Select) ...	291	IPC16 (Interrupt Priority Control 16)	125
		IPC17 (Interrupt Priority Control 17)	126