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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V3
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	16
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-FQFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5307ai66b

- DMA controller
  - — Four fully programmable channels: two support external requests
  - — Dual-address and single-address transfer support with 8-, 16-, and 32-bit data capability
  - — Source/destination address pointers that can increment or remain constant
  - — 24-bit transfer counter per channel
  - — Operand packing and unpacking supported
  - — Auto-alignment transfers supported for efficient block movement
  - — Bursting and cycle steal support
  - — Two-bus-clock internal access
  - — Automatic DMA transfers from on-chip UARTs using internal interrupts
- DRAM controller
  - — Synchronous DRAM (SDRAM), extended-data-out (EDO) DRAM, and fast page mode support
  - — Up to 512 Mbytes of DRAM
  - — Programmable timer provides CAS-before-RAS refresh for asynchronous DRAMs
  - — Support for two separate memory blocks
- Two UARTs
  - — Full-duplex operation
  - — Programmable clock
  - — Modem control signals available ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$)
  - — Processor-interrupt capability
- Dual 16-bit general-purpose multiple-mode timers
  - — 8-bit prescaler
  - — Timer input and output pins
  - — Processor-interrupt capability
  - — Up to 22-nS resolution at 45 MHz
- I^2C module
  - — Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - — Fully compatible with industry-standard I^2C bus
  - — Master or slave modes support multiple masters
  - — Automatic interrupt generation with programmable level
- System interface module (SIM)
  - — Chip selects provide direct interface to 8-, 16-, and 32-bit SRAM, ROM,

1.4.2 User Registers

The user programming model is shown in Figure 1-4 and summarized in Table 1-1.

Table 1-1. User-Level Registers

Register	Description
Data registers (D0–D7)	These 32-bit registers are for bit, byte, word, and longword operands. They can also be used as index registers.
Address registers (A0–A7)	These 32-bit registers serve as software stack pointers, index registers, or base address registers. The base address registers can be used for word and longword operations. A7 functions as a hardware stack pointer during stacking for subroutine calls and exception handling.
Program counter (PC)	Contains the address of the instruction currently being executed by the MCF5307 processor
Condition code register (CCR)	The CCR is the lower byte of the SR. It contains indicator flags that reflect the result of a previous operation and are used for conditional instruction execution.
MAC status register (MACSR)	Defines the operating configuration of the MAC unit and contains indicator flags from the results of MAC instructions.
Accumulator (ACC)	General-purpose register used to accumulate the results of MAC operations
Mask register (MASK)	General-purpose register provides an optional address mask for MAC instructions that fetch operands from memory. It is useful in the implementation of circular queues in operand memory.

1.4.3 Supervisor Registers

Table 1-2 summarizes the MCF5307 supervisor-level registers.

Table 1-2. Supervisor-Level Registers

Register	Description
Status register (SR)	The upper byte of the SR provides interrupt information in addition to a variety of mode indicators signaling the operating state of the ColdFire processor. The lower byte of the SR is the CCR, as shown in Figure 1-4.
Vector base register (VBR)	Defines the upper 12 bits of the base address of the exception vector table used during exception processing. The low-order 20 bits are forced to zero, locating the vector table on 0-modulo-1 Mbyte address.
Cache configuration register (CACR)	Defines the operating modes of the Version 4 cache memories. Control fields configuring the instruction, data, and branch cache are provided by this register, along with the default attributes for the 4-Gbyte address space.
Access control registers (ACR0/1)	Define address ranges and attributes associated with various memory regions within the 4-Gbyte address space. Each ACR defines the location of a given memory region and assigns attributes such as write-protection and cache mode (copyback, write-through, cacheability). Additionally, CACR fields assign default attributes to the instruction and data memory spaces.
RAM base address register (RAMBAR)	Provide the logical base address for the 4-Kbyte SRAM module and define attributes and access types allowed for the SRAM.
Module base address register (MBAR)	Defines the logical base address for the memory-mapped space containing the control registers for the on-chip peripherals.

Table I-i. Acronyms and Abbreviated Terms (Continued)

Term	Meaning
MAC	Multiple accumulate unit
MBAR	Memory base address register
MSB	Most-significant byte
msb	Most-significant bit
Mux	Multiplex
NOP	No operation
OEP	Operand execution pipeline
PC	Program counter
PCLK	Processor clock
PLL	Phase-locked loop
PLRU	Pseudo least recently used
POR	Power-on reset
PQFP	Plastic quad flat pack
RISC	Reduced instruction set computing
Rx	Receive
SIM	System integration module
SOF	Start of frame
TAP	Test access port
TTL	Transistor-to-transistor logic
Tx	Transmit
UART	Universal asynchronous/synchronous receiver transmitter

Table 2-15. Miscellaneous Instruction Execution Times (Continued)

Opcode	Í	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An)	(d8,An,Xi*SF)	(xxx).wl	#<xxx>
nop		3(0/0)	—	—	—	—	—	—	—
pea	Í	—	2(0/1)	—	—	2(0/1) [3]	3(0/1)[4]	2(0/1)	—
pulse		1(0/0)	—	—	—	—	—	—	—
stop	#imm	—	—	—	—	—	—	—	3(0/0)[5]
trap	#imm	—	—	—	—	—	—	—	18(1/2)
trapf		1(0/0)	—	—	—	—	—	—	—
trapf.w		1(0/0)	—	—	—	—	—	—	—
trapf.l		1(0/0)	—	—	—	—	—	—	—
unlk	Ax	3(1/0)	—	—	—	—	—	—	—
wddata.l	Í	—	7(1/0)	7(1/0)	7(1/0)	7(1/0)	8(1/0)	7(1/0)	—
wdebug.l	Í	—	10(2/0)	—	—	10(2/0)	—	—	—

1 If a MOVE.W #imm,SR instruction is executed and #imm[13] = 1, the execution time is 1(0/0).

2 n is the number of registers moved by the MOVEM opcode.

3 PEA execution times are the same for (d16,PC).

4 PEA execution times are the same for (d8,PC,Xi*SF).

5 The execution time for STOP is the time required until the processor begins sampling continuously for interrupts.

2.7.5 Branch Instruction Execution Times

Table 2-16 shows general branch instruction timing.

Table 2-16. General Branch Instruction Execution Times

Opcode	Í	Effective Address							
		Rn	(An)	(An)+	-(An)	(d16,An)	(d8,An,Xi*SF)	(xxx).wl	#<xxx>
bra		—	—	—	—	1(0/1)[1]	—	—	—
bsr		—	—	—	—	1(0/1)[1]	—	—	—
jmp	Í	—	5(0/0)	—	—	5(0/0) [1]	6(0/0)	1(0/0)[1]	—
jsr	Í	—	5(0/1)	—	—	5(0/1)	6(0/1)	1(0/1) [1]	—
rte		—	—	14(2/0)	—	—	—	—	—
rts		—	—	8(1/0)	—	—	—	—	—

1 Assumes branch acceleration. Depending on the pipeline status, execution times may vary from 1 to 3 cycles.

For the conditional branch opcodes (bcc), a static algorithm is used to determine the prediction state of the branch. This algorithm is:

```
if bcc is a forward branch && CCR[7] == 0
        then the bcc is predicted as not-taken
```

Table 5-14. TDR Field Descriptions (Continued)

Bits	Name	Description	
28–22 12–6	EDx	Setting an EDx bit enables the corresponding data breakpoint condition based on the size and placement on the processor's local data bus. Clearing all EDx bits disables data breakpoints.	
28/12		EDLW	Data longword. Entire processor's local data bus.
27/11		EDWL	Lower data word.
26/10		EDWU	Upper data word.
25/9		EDLL	Lower lower data byte. Low-order byte of the low-order word.
24/8		EDLM	Lower middle data byte. High-order byte of the low-order word.
23/7		EDUM	Upper middle data byte. Low-order byte of the high-order word.
22/6		EDUU	Upper upper data byte. High-order byte of the high-order word.
21/5	DI	Data breakpoint invert. Provides a way to invert the logical sense of all the data breakpoint comparators. This can develop a trigger based on the occurrence of a data value other than the DBR contents.	
20–18/ 4–2	EAx	Enable address bits. Setting an EA bit enables the corresponding address breakpoint. Clearing all three bits disables the breakpoint.	
20/4		EAI	Enable address breakpoint inverted. Breakpoint is based outside the range between ABLR and ABHR.
19/3		EAR	Enable address breakpoint range. The breakpoint is based on the inclusive range defined by ABLR and ABHR.
18/2		EAL	Enable address breakpoint low. The breakpoint is based on the address in the ABLR.
17/1	EPC	Enable PC breakpoint. If set, this bit enables the PC breakpoint.	
16/0	PCI	Breakpoint invert. If set, this bit allows execution outside a given region as defined by PBR and PBMR to enable a trigger. If cleared, the PC breakpoint is defined within the region defined by PBR and PBMR.	

5.5 Background Debug Mode (BDM)

The ColdFire Family implements a low-level system debugger in the microprocessor hardware. Communication with the development system is handled through a dedicated, high-speed serial command interface. The ColdFire architecture implements the BDM controller in a dedicated hardware module. Although some BDM operations, such as CPU register accesses, require the CPU to be halted, other BDM commands, such as memory accesses, can be executed while the processor is running.

5.5.1 CPU Halt

Although many BDM operations can occur in parallel with CPU operations, unrestricted BDM operation requires the CPU to be halted. The sources that can cause the CPU to halt are listed below in order of priority:

1. A catastrophic fault-on-fault condition automatically halts the processor.

The following is a list of the key SIM features:

- Module base address register (MBAR)
  - — Base address location of all internal peripherals and SIM resources
  - — Address space masking to internal peripherals and SIM resources
- Phase-locked loop (PLL) clock control register (PLLCR) for CPU STOP instruction
  - — Control for turning off clocks to core and interrupt levels that turn clocks back on

  Chapter 7, “Phase-Locked Loop (PLL).”
- Interrupt controller
  - — Programmable interrupt level (1–7) for internal peripheral interrupts
  - — Programmable priority level (0–3) within each interrupt level
  - — Four external interrupts; one set to interrupt level 7; three others programmable to two interrupt levels

  See Chapter 9, “Interrupt Controller.”
- Chip select module
  - — Eight independent, user-programmable chip-select signals ($\overline{CS}$[7:0]) that can interface with SRAM, PROM, EPROM, EEPROM, Flash, and peripherals
  - — Address masking for 64-Kbyte to 4-Gbyte memory block sizes
  - — Programmable wait states and port sizes
  - — External master access to chip selects

  See Chapter 10, “Chip-Select Module.”
- System protection and reset status
  - — Reset status indicating the cause of last reset
  - — Software watchdog timer with programmable secondary bus monitor

  See Section 6.2.4, “Software Watchdog Timer.”
- Pin assignment register (PAR) configures the parallel port. See Section 6.2.9, “Pin Assignment Register (PAR).”
- Bus arbitration
  - — Default bus master park register (MPARK) controls internal and external bus arbitration and enables display of internal accesses on the external bus for debugging
  - — Supports several arbitration algorithms

  See Section 6.2.10, “Bus Arbitration Control.”

Table 6-3 describes RSR fields.

Table 6-3. RSR Field Descriptions

Bits	Name	Description
7	HRST	Hardware or system reset 1 An external device driving $\overline{\text{RSTI}}$ caused the last reset. Assertion of reset by an external device causes the core processor to take a reset exception. All registers in internal peripherals and the SIM are reset.
6	—	Reserved, should be cleared.
5	SWTR	Software watchdog timer reset 1 The last reset was caused by the software watchdog timer. If SYPCR[SWRI] = 1 and the software watchdog timer times out, a hardware reset occurs.
4–0	—	Reserved, should be cleared.

6.2.4 Software Watchdog Timer

The software watchdog timer prevents system lockup should the software become trapped in loops with no controlled exit. The software watchdog timer can be enabled or disabled through SYPCR[SWE]. If enabled, the watchdog timer requires the periodic execution of a software watchdog servicing sequence. If this periodic servicing action does not occur, the timer times out, resulting in a watchdog timer $\overline{\text{IRQ}}$ or hardware reset with $\overline{\text{RSTO}}$ driven low, as programmed by SYPCR[SWRI].

If the timer times out and the software watchdog transfer acknowledge enable bit (SYPCR[SWTA]) is set, a watchdog timer $\overline{\text{IRQ}}$ is asserted. Note that the software watchdog timer IACK cycle cannot be autovectored.

If a software watchdog timer IACK cycle has not occurred after another timeout, SWT $\overline{\text{TA}}$ is asserted in an attempt to terminate the bus cycle and allow the IACK cycle to proceed. The setting of SYPCR[SWTAVAL] indicates that the watchdog timer $\overline{\text{TA}}$ was asserted. Figure 6-4 shows termination of a locked bus.

Table 7-2. PLL Module Input SIgnals

SIgnal	Description
FREQ[1:0]	Input bus indicating the CLKIN frequency range. FREQ[1:0] are multiplexed with D[3:2] and are sampled while $\overline{\text{RSTI}}$ is asserted. FREQ[1:0] must be correctly set for proper operation. These signals do not affect CLKIN frequency but are required to set up the analog PLL to handle the input clock frequency. 00 16.6—27.999 MHz 01 28—38.999 MHz 10 39—45 MHz 11 Not used
DIVIDE[1:0]	The MCF5307 samples clock ratio encodings on the lower data bits of the bus to determine the CLKIN-to-processor clock ratio. D[1:0]/DIVIDE[1:0] support the divide-ratio combinations. 00 1/4 01 Not used 10 1/2 11 1/3

Table 7-3 describes PLL module outputs.

Table 7-3. PLL Module Output Signals

Output	Description
BCLKO	This bus clock output provides a divided version of the processor clock frequency, determined by DIVIDE[1:0].
PSTCLK	Provides a buffered processor status clock at 2X the CLKIN frequency. PSTCLK is a delayed version of PCLK. See Section 7.4.1, “PCLK, PSTCLK, and BCLKO,” and Figure 7-1.
$\overline{\text{RSTO}}$	This output provides an external reset for peripheral devices.

7.4 Timing Relationships

The MCF5307 uses CLKIN and BCLKO, which is generated by the PLL and may be used as the bus timing reference for external devices. The MCF5307 BCLKO frequency can be 1/2, 1/3, or 1/4 the processor clock. In this document, bus timings are referenced from BCLKO. Furthermore, depending on the user configuration, the BCLKO-to-processor clock ratio may differ from the CLKIN-to-processor clock ratio.

7.4.1 PCLK, PSTCLK, and BCLKO

Figure 7-3 shows the frequency relationships between PCLK, PSTCLK,CLKIN, and the three possible versions of BCLKO. This figure does not show the skew between CLKIN and PCLK, PSTCLK, and BCLKO. PSTCLK is equal to frequency of PCLK. Similarly, the skew between PCLK and BCLKO is unspecified.

11.3.3.5 Refresh Operation

The DRAM controller supports $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operations that are not synchronized to bus activity. A special $\overline{\text{DRAMW}}$ pin is provided so refresh can occur regardless of the state of the processor bus.

When the refresh counter rolls over, it sets an internal flag to indicate that a refresh is pending. If that happens during a continuous page-mode access, the page is closed ($\overline{\text{RAS}}$ precharged) when the data transfer completes to allow the refresh to occur. The flag is cleared when the refresh cycle is run. Both memory blocks are simultaneously refreshed as determined by the DCR. DRAM accesses are delayed during refresh. Only an active bus access to a DRAM block can delay refresh.

Figure 11-12 shows a bus cycle delayed by a refresh operation. Notice that $\overline{\text{DRAMW}}$ is forced high during refresh. The row address is held until the pending DRAM access.

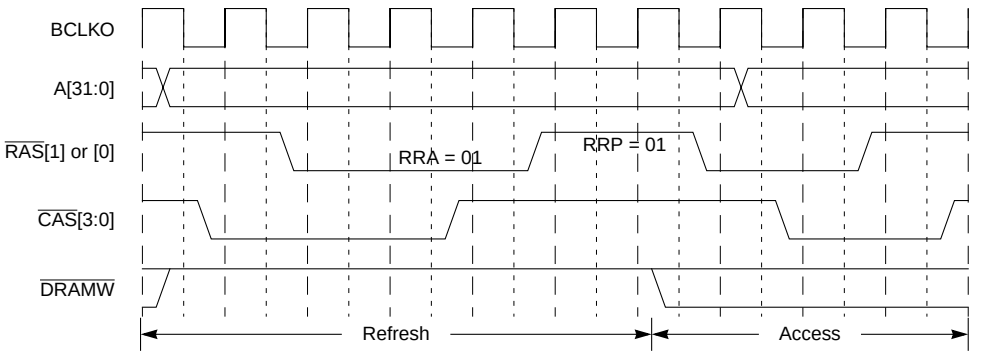

Figure 11-12. DRAM Access Delayed by Refresh

11.4 Synchronous Operation

By running synchronously with the system clock instead of responding to asynchronous control signals, SDRAM can (after an initial latency period) be accessed on every clock; 5-1-1-1 is a typical MCF5307 burst rate to SDRAM.

Note that because the MCF5307 cannot have more than one page open at a time, it does not support interleaving.

SDRAM controllers are more sophisticated than asynchronous DRAM controllers. Not only must they manage addresses and data, but they must send special commands for such functions as precharge, read, write, burst, auto-refresh, and various combinations of these functions. Table 11-10 lists common SDRAM commands.

tables, find the one that corresponds to the number of column address lines on the SDRAM and to the port size as seen by the MCF5307, which is not necessarily the SDRAM port size. For example, if two 1M x 16-bit SDRAMs together form a 2M x 32-bit memory, the port size is 32 bits. Most SDRAMs likely have fewer address lines than are shown in the tables, so follow only the connections shown until all SDRAM address lines are connected.

Table 11-15. MCF5307 to SDRAM Interface (8-Bit Port, 9-Column Address Lines)

MCF5307 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8														
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22

Table 11-16. MCF5307 to SDRAM Interface (8-Bit Port,10-Column Address Lines)

MCF5307 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8	18												
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21

Table 11-17. MCF5307 to SDRAM Interface (8-Bit Port,11-Column Address Lines)

MCF5307 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	19	21	22	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8	18	20										
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20

Table 11-18. MCF5307 to SDRAM Interface (8-Bit Port,12-Column Address Lines)

MCF5307 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A21	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	19	21	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8	18	20	22								
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19

- Because of the nature of the internal CPU pipeline this condition does not occur often; however, the use of continuous page mode is recommended because it can provide a slight performance increase.

Figure 11-20 shows two read accesses in continuous page mode. Note that there is no precharge between the two accesses. Also notice that the second cycle begins with a read operation with no ACTV command.

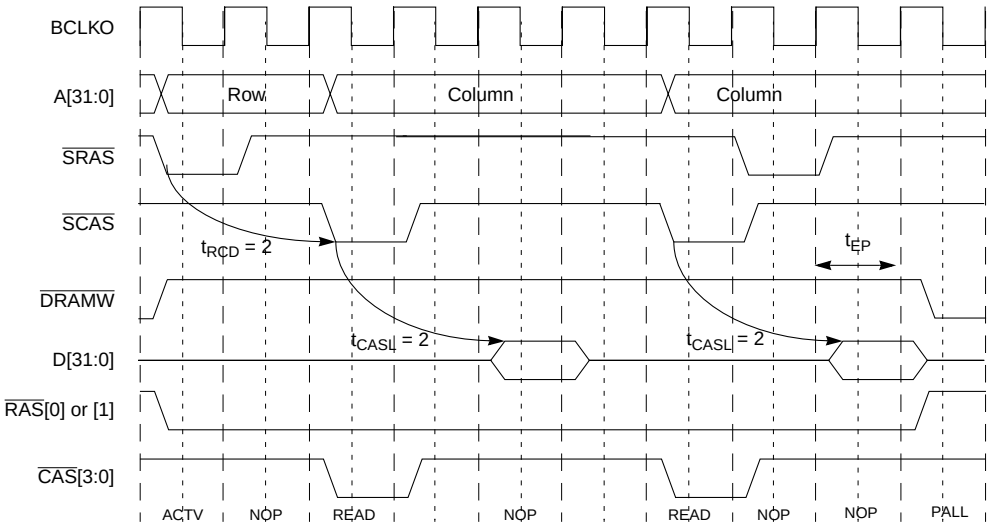

Figure 11-20. Synchronous, Continuous Page-Mode Access—Consecutive Reads

Figure 11-21 shows a write followed by a read in continuous page mode. Because the bus cycle is terminated with a WRITE command, the second cycle begins sooner after the write than after the read. A read requires data to be returned before the bus cycle can terminate. Note that in continuous page mode, secondary accesses output the column address only.

Chapter 12
DMA Controller Module

This chapter describes the MCF5307 DMA controller module. It provides an overview of the module and describes in detail its signals and registers. The latter sections of this chapter describe operations, features, and supported data transfer modes in detail.

12.1 Overview

The direct memory access (DMA) controller module provides an efficient way to move blocks of data with minimal processor interaction. The DMA module, shown in Figure 12-1, provides four channels that allow byte, word, or longword operand transfers. Each channel has a dedicated set of registers that define the source and destination addresses (SAR*n* and DAR*n*), byte count (BCR*n*), and control and status (DCR*n* and DSR*n*). Transfers can be dual or single address to off-chip devices or dual address to on-chip devices, such as UART, SDRAM controller, and parallel port.

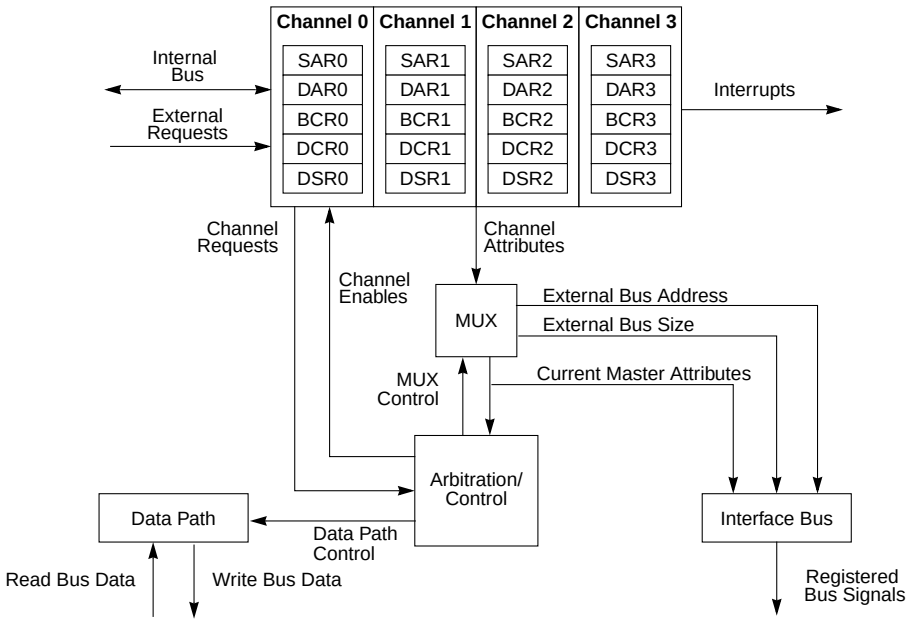

Figure 12-1. DMA Signal Diagram

Table 13-5. Calculated Time-out Values (90-MHz Processor Clock) (Continued)

TMR[PS]		TMR[CLK] = 10 (System Bus Clock/16)			TMR[CLK] = 01 (System Bus Clock/1)		
Decimal	Hex	45 MHz	30 MHz	22.5 MHz	45 MHz	30 MHz	22.5 MHz
126	7E	2.95931	4.43897	5.91863	0.18496	0.27744	0.36991
127	7F	2.98262	4.47392	5.96523	0.18641	0.27962	0.37283
128	80	3.00592	4.50888	6.01184	0.18787	0.2818	0.37574
129	81	3.02922	4.54383	6.05844	0.18933	0.28399	0.37865
130	82	3.05252	4.57878	6.10504	0.19078	0.28617	0.38157
131	83	3.07582	4.61373	6.15165	0.19224	0.28836	0.38448
132	84	3.09912	4.64869	6.19825	0.1937	0.29054	0.38739
133	85	3.12243	4.68364	6.24485	0.19515	0.29273	0.3903
134	86	3.14573	4.71859	6.29146	0.19661	0.29491	0.39322
135	87	3.16903	4.75354	6.33806	0.19806	0.2971	0.39613
136	88	3.19233	4.7885	6.38466	0.19952	0.29928	0.39904
137	89	3.21563	4.82345	6.43127	0.20098	0.30147	0.40195
138	8A	3.23893	4.8584	6.47787	0.20243	0.30365	0.40487
139	8B	3.26224	4.89335	6.52447	0.20389	0.30583	0.40778
140	8C	3.28554	4.92831	6.57108	0.20535	0.30802	0.41069
141	8D	3.30884	4.96326	6.61768	0.2068	0.3102	0.4136
142	8E	3.33214	4.99821	6.66428	0.20826	0.31239	0.41652
143	8F	3.35544	5.03316	6.71089	0.20972	0.31457	0.41943
144	90	3.37874	5.06812	6.75749	0.21117	0.31676	0.42234
145	91	3.40205	5.10307	6.80409	0.21263	0.31894	0.42526
146	92	3.42535	5.13802	6.8507	0.21408	0.32113	0.42817
147	93	3.44865	5.17297	6.8973	0.21554	0.32331	0.43108
148	94	3.47195	5.20793	6.9439	0.217	0.3255	0.43399
149	95	3.49525	5.24288	6.99051	0.21845	0.32768	0.43691
150	96	3.51856	5.27783	7.03711	0.21991	0.32986	0.43982
151	97	3.54186	5.31279	7.08371	0.22137	0.33205	0.44273
152	98	3.56516	5.34774	7.13032	0.22282	0.33423	0.44564
153	99	3.58846	5.38269	7.17692	0.22428	0.33642	0.44856
154	9A	3.61176	5.41764	7.22352	0.22574	0.3386	0.45147
155	9B	3.63506	5.4526	7.27013	0.22719	0.34079	0.45438
156	9C	3.65837	5.48755	7.31673	0.22865	0.34297	0.4573
157	9D	3.68167	5.5225	7.36333	0.2301	0.34516	0.46021
158	9E	3.70497	5.55745	7.40994	0.23156	0.34734	0.46312
159	9F	3.72827	5.59241	7.45654	0.23302	0.34953	0.46603
160	A0	3.75157	5.62736	7.50314	0.23447	0.35171	0.46895
161	A1	3.77487	5.66231	7.54975	0.23593	0.35389	0.47186
162	A2	3.79818	5.69726	7.59635	0.23739	0.35608	0.47477
163	A3	3.82148	5.73222	7.64295	0.23884	0.35826	0.47768
164	A4	3.84478	5.76717	7.68956	0.2403	0.36045	0.4806
165	A5	3.86808	5.80212	7.73616	0.24176	0.36263	0.48351

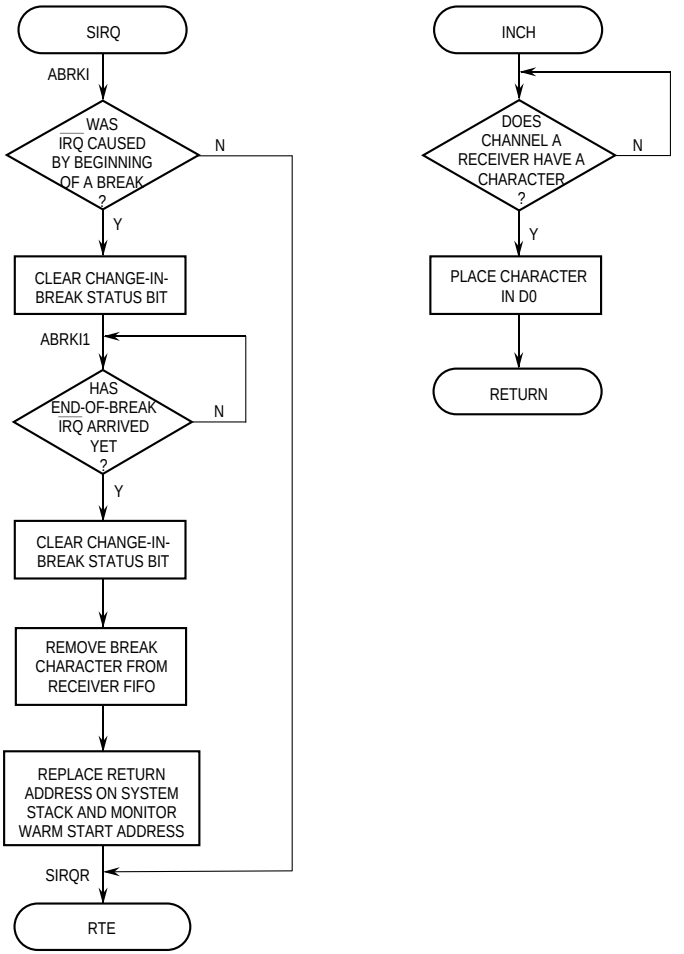

Figure 14-27. UART Mode Programming Flowchart (Sheet 4 of 5)

17.8.1 DMA Request ($\overline{\text{DREQ}}$[1:0]/PP[6:5])

The DMA request pins ($\overline{\text{DREQ}}$[1:0]/PP[6:5]) can serve as the DMA request inputs or as two bits of the parallel port, as determined by individually programmable bits in the PAR.

These inputs are asserted by a peripheral device to request an operand transfer between that peripheral and memory by either channel 0 or 1 of the on-chip DMA.

Note that DMA acknowledge indication is displayed on TM[2:0], during DMA transfers of channel 0 and 1.

17.9 Serial Module Signals

The signals in the following sections are used to transfer serial data between the two UART modules and external peripherals.

17.9.1 Transmitter Serial Data Output (TxD)

TxD is held high (mark condition) when the transmitter is disabled, idle, or operating in the local loop-back mode. Data is shifted out least-significant bit (lsb) first on TxD on the falling edge of the clock source.

17.9.2 Receiver Serial Data Input (RxD)

Data received on RxD is sampled on the rising edge of the clock source, with the lsb received first.

17.9.3 Clear to Send ($\overline{\text{CTS}}$)

This input can generate an interrupt on a change of state.

17.9.4 Request to Send ($\overline{\text{RTS}}$)

This output can be programmed to be negated or asserted automatically by either the receiver or the transmitter. When connected to a transmitter's $\overline{\text{CTS}}$, $\overline{\text{RTS}}$ can control serial data flow.

17.10 Timer Module Signals

The signals in the following sections are external interfaces to the two general-purpose MCF5307 timers. These 16-bit timers can capture timer values, trigger external events or internal interrupts, or count external events.

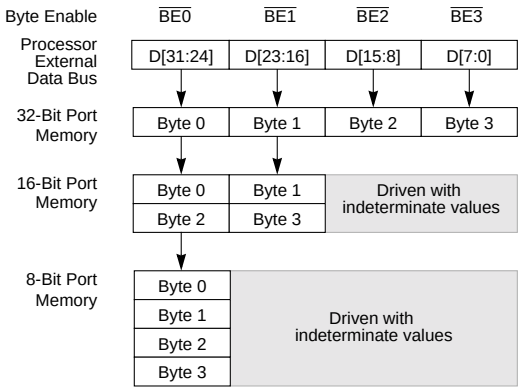

Figure 18-2. Connections for External Memory Port Sizes

The timing relationships between BCLKOchip select ($\overline{CS}$[7:0]), byte enable/byte write enables ($\overline{BE}$/$\overline{BWE}$[3:0]), and output enable ($\overline{OE}$) are similar to their relationships with address strobe ($\overline{AS}$) in that all transitions occur during the low phase of BCLKO. However, as shown in Figure 18-3, differences in on-chip signal routing and external loading may prevent signals from asserting simultaneously.

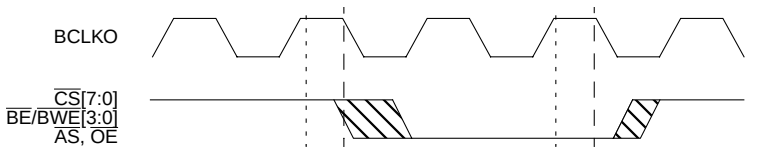

Figure 18-3. Chip-Select Module Output Timing Diagram

18.4.1 Bus Cycle Execution

When a bus cycle is initiated, the MCF5307 first compares its address with the base address and mask configurations programmed for chip selects 0–7 (CSCR0–CSCR7) and for DRAM blocks 0 and 1 address and control registers (DACR0 and DACR1). If the driven address matches a programmed chip select or DRAM block, the appropriate chip select is asserted or the DRAM block is selected using the specifications programmed in the respective configuration register. Otherwise, the following occurs:

- If the address and attributes do not match in CSCR or DACR, the MCF5307 runs an external burst-inhibited bus cycle with a default of external termination on a 32-bit port.
- If an address and attribute match in multiple CSCRs, the matching chip-select signals are driven; however, the MCF5307 runs an external burst-inhibited bus cycle with external termination on a 32-bit port.
- If an address and attribute match both DACRs or a DACR and a CSCR, the operation is undefined.

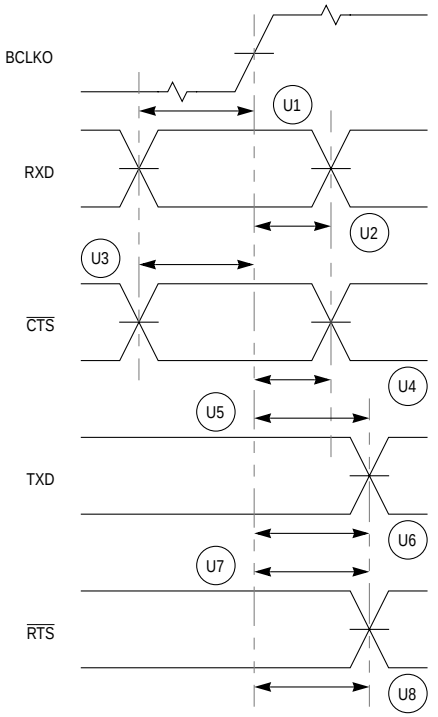

Figure 20-16. UART0/1 Module AC Timing—UART Mode

System memory. The physical memory available to a processor.

T

Tenure. A tenure consists of three phases: arbitration, transfer, termination. There can be separate address bus tenures and data bus tenures.

Throughput. The measure of the number of instructions that are processed per clock cycle.

Transfer termination. The successful or unsuccessful conclusion of a data transfer.

U

Underflow. A condition that occurs during arithmetic operations when the result cannot be represented accurately in the destination register.

User mode. The operating state of a processor used typically by application software. In user mode, software can access only certain control registers and can access only user memory space. No privileged operations can be performed.

W

Word. A 16-bit data element.

Write-through. A cache memory update policy in which all processor write cycles are written to both the cache and memory.

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