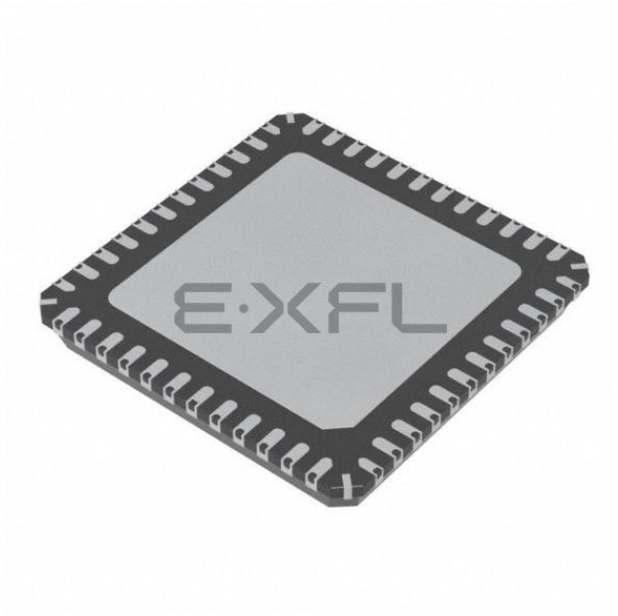

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (52kB)
Controller Series	-
RAM Size	4K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	3V ~ 28V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle98432qxxuma1

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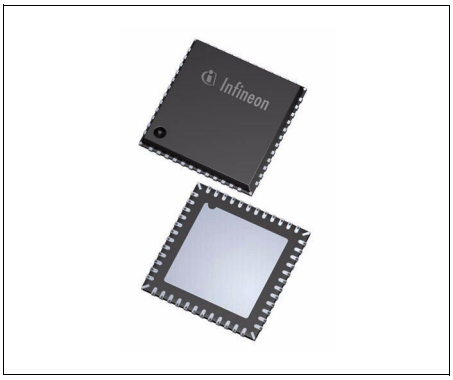
1 Overview



VQFN-48-31

Summary of Features

- 32-bit ARM Cortex-M0 Core
  - up to 40 MHz clock frequency
  - one clock per machine cycle architecture
  - single cycle multiplier
- On-chip memory
  - 52 KB Flash (including EEPROM)
  - 4 KB EEPROM (emulated in Flash)
  - 768 bytes 100 Time Programmable Memory (100TP)
  - 4 KB RAM
  - Boot ROM for startup firmware and Flash routines
- On-chip OSC
- 2 Low-Side Switches incl. PWM functionality, can be used e.g. as relay driver
- 2 High-Side Switches with cyclic sense option and PWM functionality, e.g. for supplying LEDs or switch panels (min. 150 mA)
- 5 High Voltage Monitor Input pins for wake-up and with cyclic sense with analog measurement option
- 10 General-purpose I/O Ports (GPIO)
- 6 Analog input Ports
- 10-Bit A/D Converter with 6 analog inputs + VBAT_SENSE + VS + 5 high voltage monitoring inputs
- 8-Bit A/D Converter with 7 inputs for voltage and temperature supervision
- Measurement unit with 12 channels together with the onboard 10-Bit A/D converter and data post processing
- 16-Bit timers - GPT12, Timer 2 and Timer 21
- Capture/compare unit for PWM signal generation (CCU6)
- 2 full duplex serial interfaces (UART1, UART2), UART1 with LIN support
- 2 synchronous serial channels (SSC1, SSC2)
- On-chip debug support via 2-wire SWD
- LIN Bootstrap loader to program the Flash via LIN (LIN BSL)
- 1 LIN 2.2 transceiver
- Single power supply from 3.0 V to 28 V
- Low-dropout voltage regulators (LDO)
- 5 V voltage supply VDDEXT for external loads (e.g. Hall-sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes:
  - Micro Controller Unit slow-down mode

Type	Package	Marking
TLE9843-2QX	VQFN-48-31	TLE9843-2QX

6 System Control Unit - Digital Modules (SCU-DM)

6.1 Features

- Flexible clock configuration features
- Reset management of all system resets
- System modes control for all power modes (active, power down, sleep)
- Interrupt enabling for many system peripherals
- General purpose input output control
- Debug mode control of system peripherals

6.2 Introduction

The System Control Unit (SCU) supports all central control tasks in the TLE9843-2QX. The SCU is made up of the following sub-modules:

- Clock System and Control (CGU)
- Reset Control (RCU)
- Power Management (PCU)
- Interrupt Management (ICU)
- General Port Control
- Flexible Peripheral Management
- Module Suspend Control
- Error Detection and Correction in Data Memory
- Miscellaneous Control
- Register Mapping

  - Reset_Type_4; Peripheral reset (without SOFT)
- Baudrate generator:
  - f_{BR}; Baudrate clock for UART
- Port Control:
  - P0_POCONy.PDMx; driver strength control
  - P1_POCONy.PDMx; driver strength control
- MISC:
  - MODPISELx; Mode selection registers for UART (source selection) and Timer (trigger or count selection)

The on-chip memory modules available in the TLE9843-2QX are:

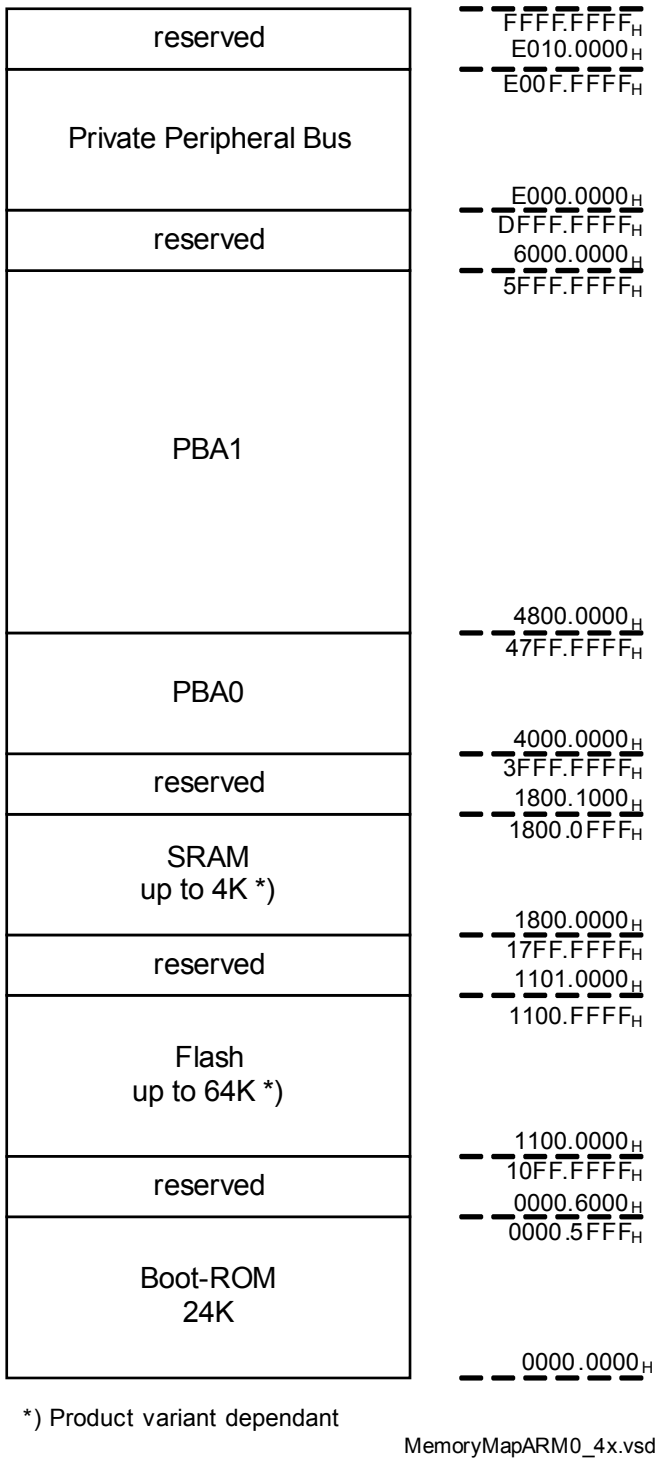


Figure 17 TLE9843-2QX Memory Map

11 NVM Module (Flash Memory)

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-System Programming via LIN (Flash mode) and SWD
- Error Correction Code (ECC) for detection of single Bit and double Bit errors and dynamic correction of single Bit errors on Data Block (Double words, 64 bits).
- Interrupt and signaling of double bit error by NMI, address of double bit error readable by FW API user routine.
- Possibility of checking single bit error occurrence by ROM routines
- Program width of 128 Byte (page)
- Minimum erase width of 128 Byte (page)
- Integrated hardware support for EEPROM emulation
- 8 Byte read access
- Physical read access time: typ. 75 ns
- Code read access acceleration integrated; read buffer
- Page program time: typ. 3 ms
- Programming time for 64KB via Debug Interface: < 1800 ms (typ.)
- Page erase (128 bytes) and sector erase (4K bytes) time: typ. 4ms
- 3 separate keys for data area, program area and BSL area
- Password protection for three configurable program flash areas, three separate keys for data, program and BSL
- Security option to protect read out via debug interface in application run mode. NVM protection mode available, which can be enabled/disabled with password
- Write/erase access to 100TP (e.g. option bytes) is possible via the debug interface

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency f_{sys}. Integrated firmware routines are provided to ease NVM, and other operations including EEPROM emulation.

The TLE9843-2QX NVM module provides physical implementation of the memory module as well as needed complementary features and interface towards the core.

The module provides proper access to the memory through 2 AHB-Lite interfaces: a 8-bit data interface for NVM internal register access and a 32-bit data interface for code/data access both multiplexed on Cortex-M0 system bus.

The TLE9843-2QX NVM module consists of the memory cell array and all the control circuits and registers needed to access the array itself. The 64 Kbyte data module is mapped in the Cortex-M0 code address range 11000000H - 1100FFFFH while the dedicated SFRs are mapped in the Cortex-M0 system address range .

Access of NVM module is granted through the AMBA matrix block that forwards to the memory modules AHB-Lite interfaces the requests generated by the masters according to the defined priority policy.

14.2.1 Port 0 and Port 1

Figure 21 shows the block diagram of an TLE9843-2QX bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin.

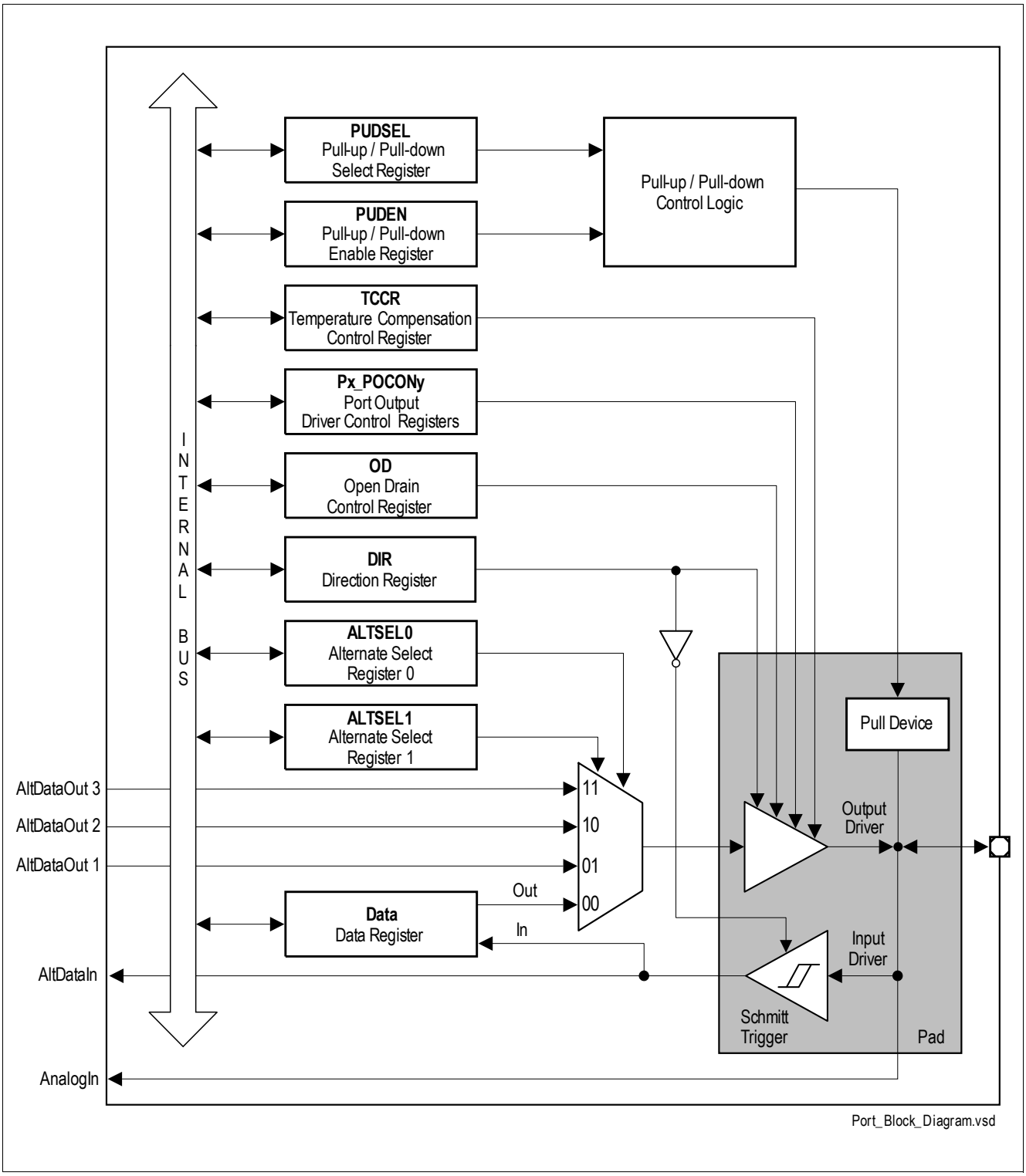


Figure 21 General Structure of Bidirectional Port

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Port 1alternate function mapping according Table 9

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12
		INP2	CC61_0	CCU6
		INP3	SSC2_S_SCK	SSC2
		INP4	T4EUDB	GPT12
	Output	GPO	P1_DATA.P0	
		ALT1	SSC2_M_SCK	SSC2
		ALT2	CC61_0	CCU6
		ALT3	UART2_TXD	UART2
P1.1	Input	GPI	P1_DATA.P1	
		INP1	T6EUDA	GPT12
		INP2	T5INB	GPT12
		INP3	T3EUDC	GPT12
		INP4	SSC2_S_MTSR	SSC2
		INP5	T21EX_3	Timer 21
		INP6	UART2_RXD	UART2
	Output	GPO	P1_DATA.P1	
		ALT1	SSC2_M_MTSR	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	EXF21_1	Timer 21
P1.2	Input	GPI	P1_DATA.P2	
		INP1	EXINT0_1	SCU
		INP2	T21_1	Timer 21
		INP3	T2INA	GPT12
		INP4	SSC2_M_MRST	SSC2
		INP5	CCPOS2_2	CCU6
	Output	GPO	P1_DATA.P2	
		ALT1	SSC2_S_MRST	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT_1	GPT12

Table 9 Port 1 Input / Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.4	Input	GPI	P1_DATA.P4	
		INP1	EXINT2_1	SCU
		INP2	T21EX_1	Timer 21
		INP3	T2INB	GPT12
		INP4	T5EUDA	GPT12
		INP5	SSC12_S_MTSR	SSC1/2
		INP6	CCPOS1_2	CCU6
	Output	GPO	P1_DATA.P4	
		ALT1	CLKOUT_1	SCU
		ALT2	COUT62_0	CCU6
		ALT3	SSC12_M_MTSR	SSC1/2

Table 10 Port 2 Input Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.5	Input / Output	GPI	P2_DATA.P5	
		INP1	T3EUDB	GPT12
		INP2	T4EUDC	GPT12
		INP3	T2_1	Timer 2
		INP4	LIN_TXD	LIN
		INP5	CCPOS1_3	CCU6
		OUT	XTAL (out)[1)]	XTAL
P2.6	Input	GPI	P2_DATA.P6	
		INP1	T4EUDD	GPT12
		INP2	T2EX_3	Timer 2
		INP3	CCPOS2_3	CCU6
		INP4	T13HR_2	CCU6
		ANALOG	AN6	ADC
P2.7	Input	GPI	P2_DATA.P7	
		INP1	CCPOS2_0	CCU6
		INP2	EXINT2_0	SCU
		INP3	T13HR_1	CCU6
		INP4	CC62_1	CCU6
		ANALOG	AN7	ADC

1) configurable by user

15.2.1 Block Diagram GPT1

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

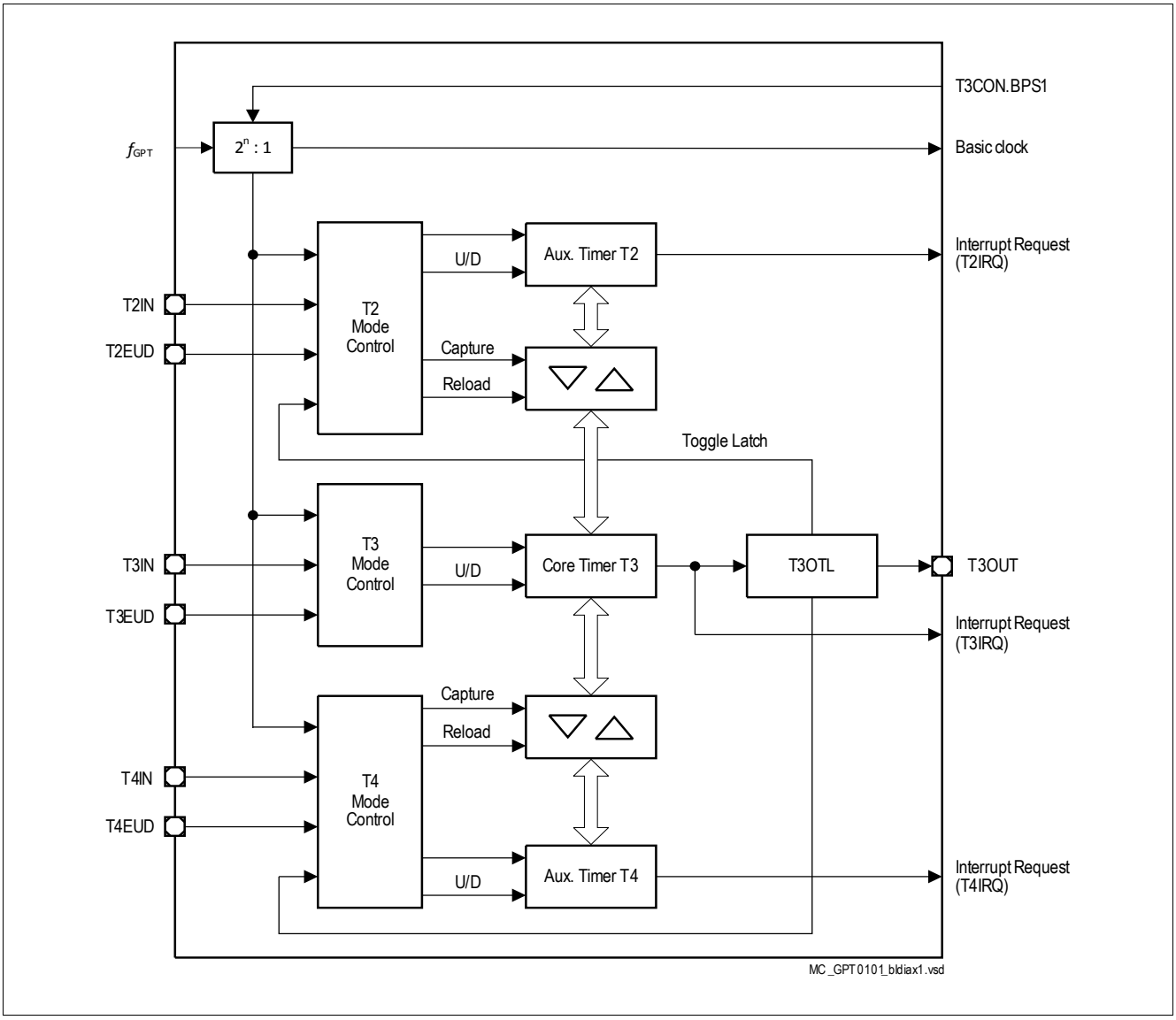


Figure 23 GPT1 Block Diagram (n = 2 … 5)

15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

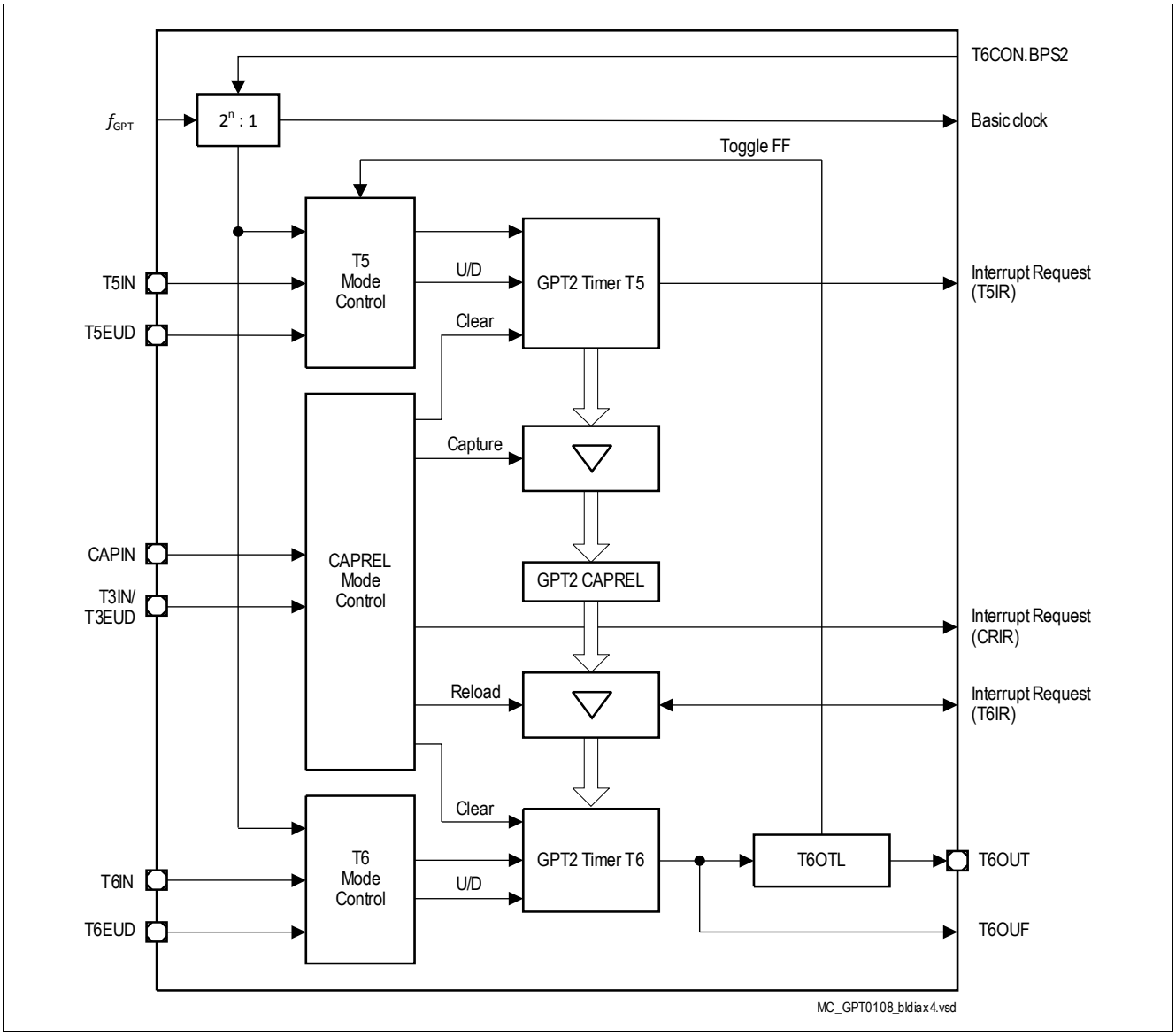


Figure 24 GPT2 Block Diagram (n = 1 … 4)

18 UART1/UART2

18.1 Features

- Full-duplex asynchronous modes
  - 8-Bit or 9-Bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered (1 Byte)
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates, e.g. 9.6kBaud, 19.2kBaud, 115.2kBaud, 125kBaud, 250kBaud, 500kBaud
- Hardware logic for break and sync byte detection
- for UART1: LIN support: connected to timer channel for synchronization to LIN baud rate

In all modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in the modes by the incoming start bit if REN = 1.

The serial interface also provides interrupt requests when transmission or reception of the frames has been completed. The corresponding interrupt request flags are TI or RI, respectively. If the serial interrupt is not used (i.e., serial interrupt not enabled), TI and RI can also be used for polling the serial interface.

18.2 Introduction

The UART1/UART2 provide a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. They are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the previous byte will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

20.2.1 Block Diagram

Figure 28 shows all functional relevant interfaces associated with the SSC Kernel.

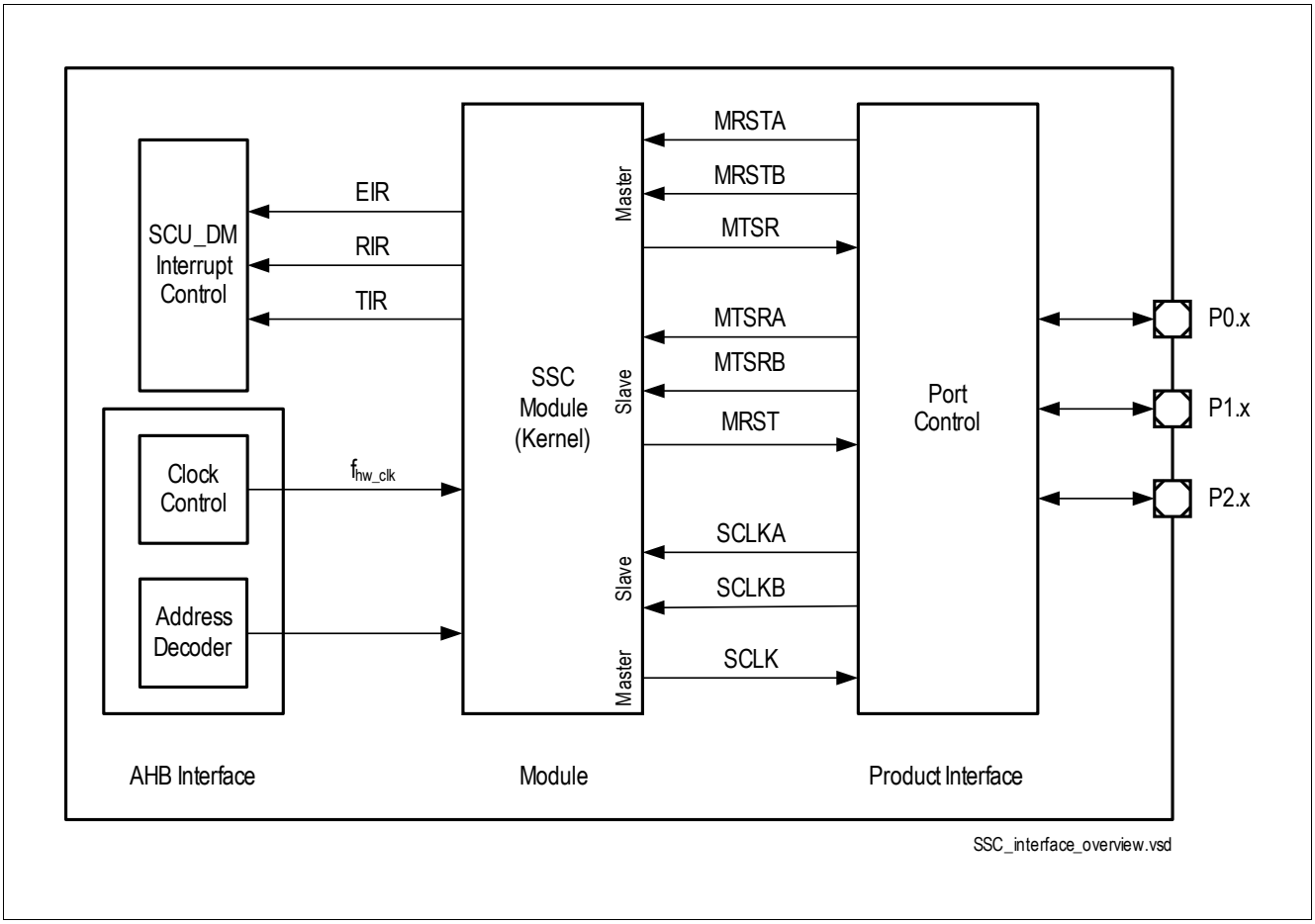


Figure 28 SSC Interface Diagram

25 High-Side Switch

25.1 Features

The high-side switch is optimized for driving resistive loads. Only small line inductance are allowed. Typical applications are single or multiple LEDs of a dashboard, switch illumination or other loads that require a high-side switch.

A cyclic switch activation during Sleep Mode or Stop Mode of the system is also available.

Functional Features

- Multi-purpose high-side switch for resistive load connections (only small line inductances are allowed)
- Overcurrent limitation
- Overcurrent detection with thresholds: 25 mA, 50 mA, 100 mA, 150 mA and automatic shutdown
- Overtemperature detection and automatic shutdown
- Open load detection in on mode with open load current of max. 1.5 mA.
- Interrupt signalling of overcurrent, overtemperature and open load condition
- Cyclic switch activation in Sleep Mode and Stop Mode with cyclic sense support and reduced driver capability: max. 40 mA
- PWM capability up to 25 kHz
- Internal connection to System-PWM Generator (CCU6)
- Slew rate control for low EMI characteristic

Applications hints

- The voltage at HSx must not exceed the supply voltage by more than 0.3V to prevent a reverse current from HSx to VS.

27 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

27.1 Relay Window Lift Application diagram

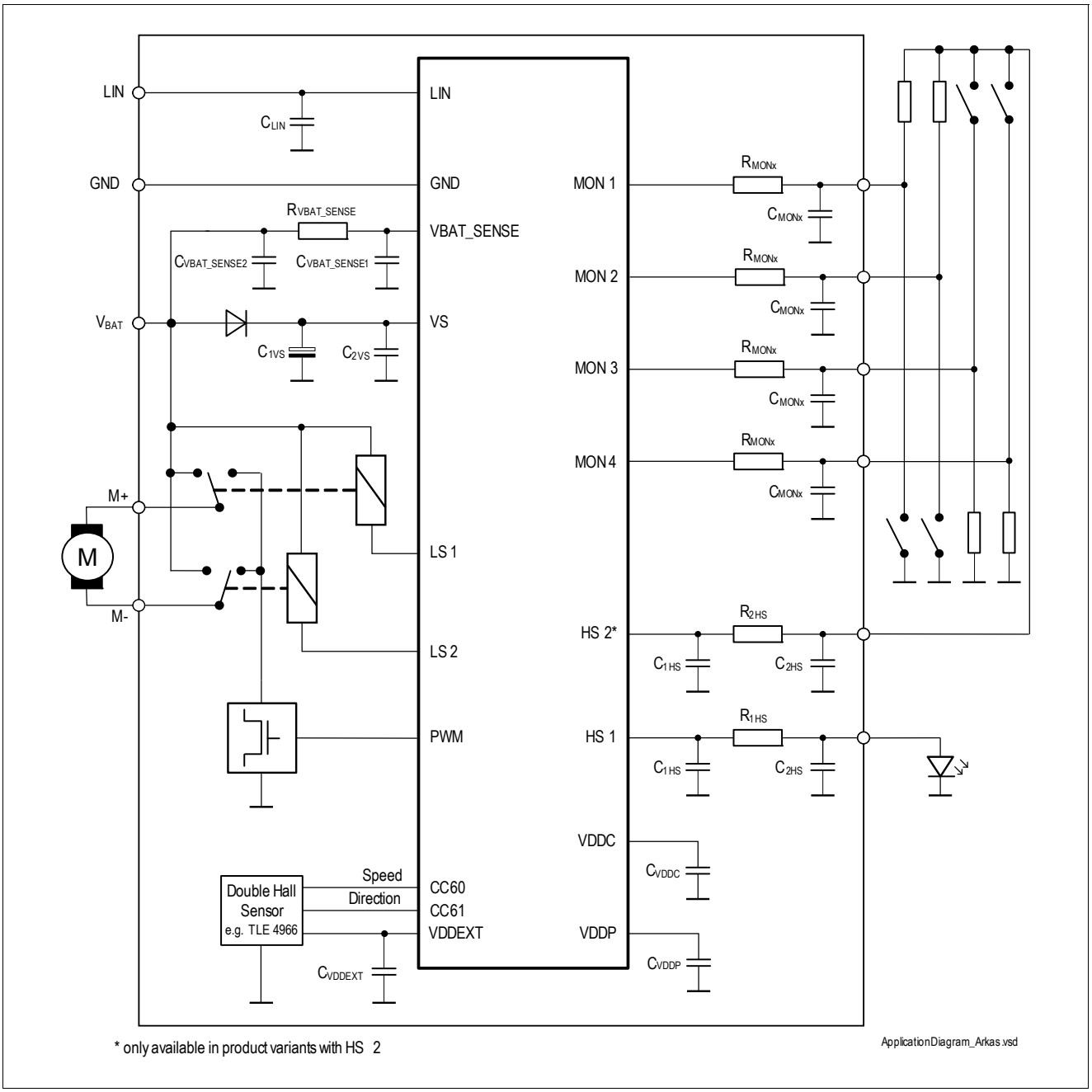


Figure 35 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

Table 16 Recommendation for connecting unused pins

type	pin number	recommendation 1 (if unused)	recommendation 2 (if unused)
MON	5, 6, 7, 8, 9	GND	open + configure internal PU/PD
LS1, LS2	11, 12	GNDLS	open
GPIO	14, 15, 16, 17, 20, 22, 23, 24, 25, 26, 33, 34, 35, 36, 37, 39	GND	external PU/PD or open + configure internal PU/PD
TMS	18	GND	
Reset	21	open	
P2/XTAL out	31	open	
P2/XTAL in	32	GND	
VDDEXT	45	open	
VBAT_SENSE	48	VS	

27.4 Connection of P0.2 for SWD debug mode

To enter the SWD debug mode, P0.2 needs to be 0 at the rising edge of the reset signal.

P0.2 has an internal pulldown, so it just needs to be ensured that there is no external 1 at P0.2 when the debug mode is entered.

27.5 Connection of TMS

For the debug mode, the TMS pin needs to be 1 at the rising edge of the reset signal. This is controlled by the debugger. The TMS pin has an internal PD.

To avoid the device entering the debug mode unintendedly in the final application, adding an external pull-down additionally is recommended.

27.6 ESD Immunity According to IEC61000-4-2

*Note: Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) were performed. The results and test condition are available in a test report. The achieved values for the test are listed in **Table 17** below.*

Table 17 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin LIN, versus GND	≥6	kV	[1)]positive pulse
ESD at pin LIN, versus GND	≤ -6	kV	[1)]negative pulse
ESD at pin VS, VBAT_SENSE, MONx, HS, versus GND	≥6	kV	[1)]positive pulse
ESD at pin VS, VBAT_SENSE, MONx, HS, versus GND	≤ -6	kV	[1)]negative pulse

28.5 Parallel Ports (GPIO)

28.5.1 Description of Keep and Force Current

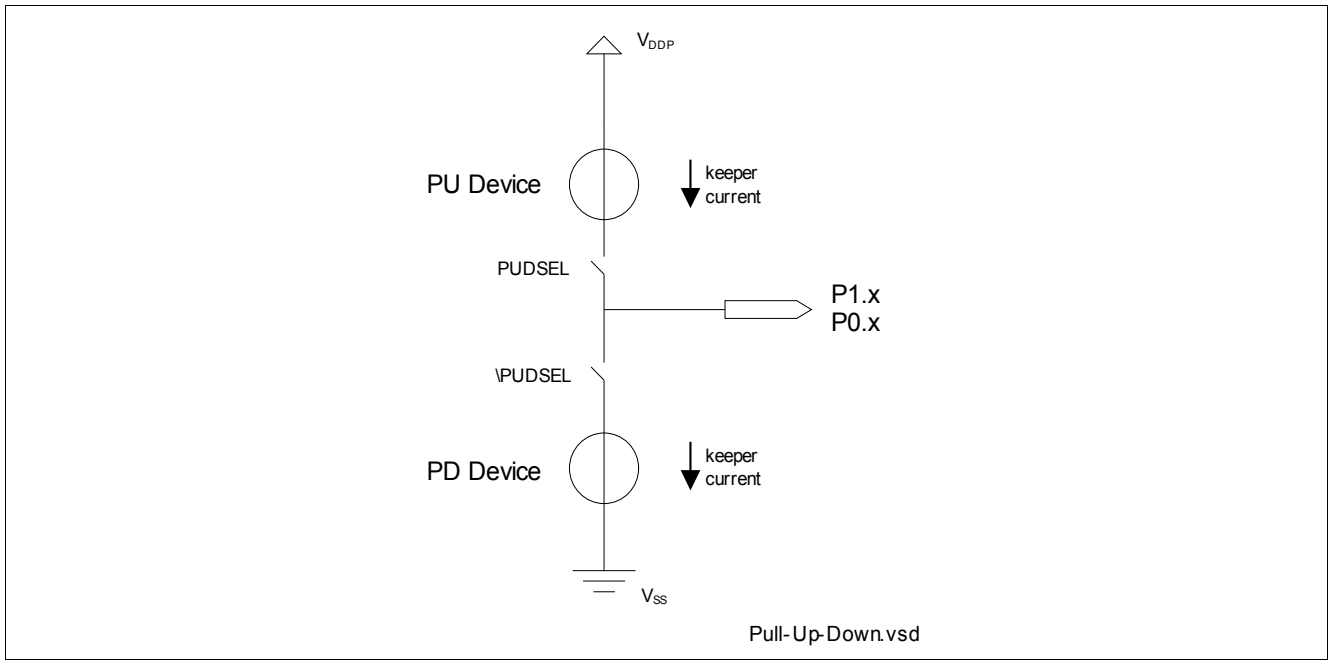


Figure 37 Pull-Up/Down Device

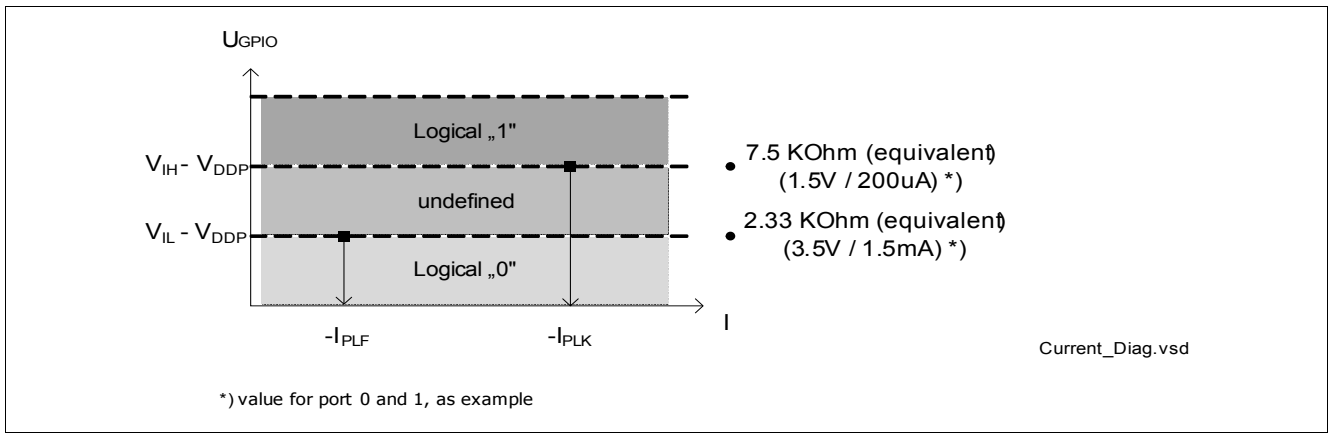


Figure 38 Pull-Up Keep and Forced Current

28.7 High-Speed Synchronous Serial Interface

28.7.1 SSC Timing

The table below provides the SSC timing in the TLE9843-2QX.

Table 37 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) 2 * T_{SSC}	–	–		2) V_{DDP} > 2.7 V	P_7.1.1
MTSR delay from SCLK	t_1	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.2
MRST setup to SCLK	t_2	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.3
MRST hold from SCLK	t_3	15	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. If f_{CPU} = 20 MHz, t_0 = 100 ns. T_{CPU} is the CPU clock period.
2) Not subject to production test, specified by design.

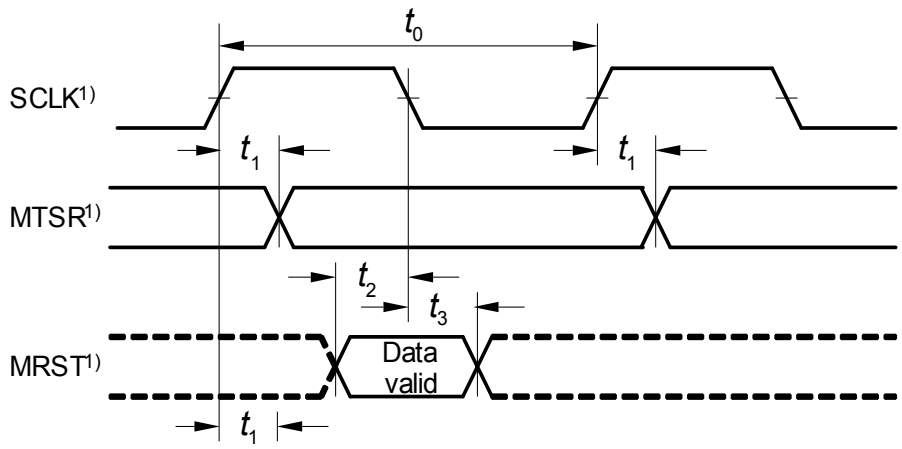


Figure 40 SSC Master Mode Timing

Table 41 A/D Converter Characteristics (cont'd)

V_S = 5.5 V to 28 V, , T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input referred noise	V_{Noise_LSB}	–	–	1.5	LSB rms	4) T_j = 25°C; this value is determined out of 4 consecutive measurements which are averaged.	P_9.2.34
Cross-coupling Attenuation between LV Channels	EA_{CCOUP}	–	±1	± 2	LSB	4) –	P_9.2.12
Input capacitance of a HV analog input	C_{AINT_HVI}	–	–	200	fF	4)	P_9.2.13
Input capacitance of a LV analog input	C_{AINT_LVI}	–	–	200	fF	4)	P_9.2.19

1) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
2) this parameter is measured with disabled hardware calibration
3) this Gain error is calibrated by IFX end of line
4) Not subject to production test