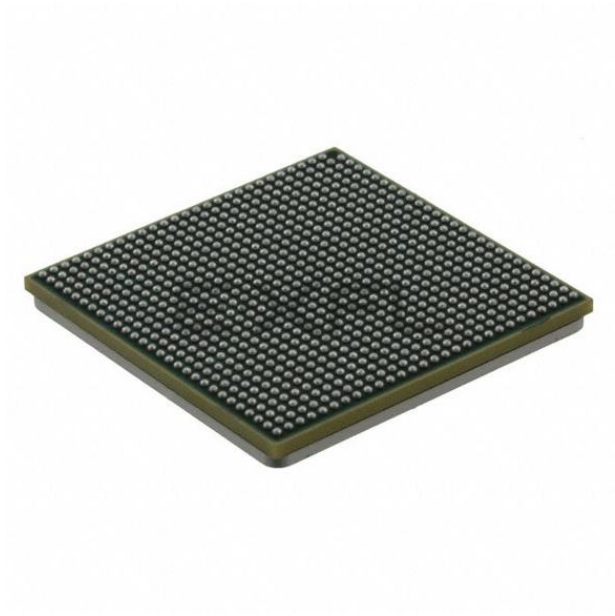

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	6.375MB
Voltage - I/O	1.0V, 1.5V, 2.5V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8157sag1000a

NOTE

See Figure 31 as a reference for correct ball grid layout.

2.2 Signal Lists

Table 1 presents the signal list sorted by ball number. Table 2 presents the signal list by signal name. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

NOTE

The information in Table 1 distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

Table 1. Signal List by Ball Number

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
A2	VSS	Ground	N/A
A3	MDQ57	I/O	GVDD
A4	GVDD	Power	N/A
A5	VSS	Ground	N/A
A6	MDQ63	I/O	GVDD
A7	GVDD	Power	N/A
A8	NC	Non-user	N/A
A9	NC	Non-user	N/A
A10	NC	Non-user	N/A
A11	NC	Non-user	N/A
A12	NC	Non-user	N/A
A13	CLKOUT	O	QVDD
A14	EE0	I	QVDD
A15	VSS	Ground	N/A
A16	MCLKIN (optional)	I	QVDD
A17	VSS	Ground	N/A
A18	CLKIN	I	QVDD
A19	VSS	Ground	N/A
A20	GPIO29/UART_TXD/CP_LOS2	I/O	NVDD
A21	GPIO31/I2C_SDA	I/O	NVDD
A22	GE1_TX_CTL	O	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
F19	GE2_RD2/CP_LOS1	I	NVDD
F20	GE2_RX_CTL	I	NVDD
F21	GE2_RD0/CP_LOS6	I	NVDD
F22	GE2_RX_CLK	I	NVDD
F23	GE2_RD1	I	NVDD
F24	GPIO26/TMR3	I/O	NVDD
F25	GPIO6/$\overline{\text{IRQ6}}$/RC6/CP_SYNC5	I/O	NVDD
F26	GPIO22	I/O	NVDD
F27	GPIO23/TMR0/$\overline{\text{BOOT\_SPI\_SL}}$	I/O	NVDD
F28	GPIO8/$\overline{\text{IRQ8}}$/RC8	I/O	NVDD
G1	VSS	Ground	N/A
G2	GVDD	Power	N/A
G3	MDM5	O	GVDD
G4	VSS	Ground	N/A
G5	GVDD	Power	N/A
G6	MDQ46	I/O	GVDD
G7	VDD	Power	N/A
G8	VSS	Ground	N/A
G9	VDD	Power	N/A
G10	VSS	Ground	N/A
G11	NC	Non-user	N/A
G12	NC	Non-user	N/A
G13	NC	Non-user	N/A
G14	NC	Non-user	N/A
G15	QVDD	Power	N/A
G16	STOP_BS	I	QVDD
G17	$\overline{\text{TRST}}$	I	QVDD
G18	VSS	Ground	N/A
G19	GPIO28/UART_RXD/CP_LOS1	I/O	NVDD
G20	GE1_RD3	I	NVDD
G21	GE1_RD2	I	NVDD
G22	GE1_RX_CLK	I	NVDD
G23	VSS	Ground	N/A
G24	GE1_RX_CTL	I	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
J3	MDQ35	I/O	GVDD
J4	GVDD	Power	N/A
J5	MDQ33	I/O	GVDD
J6	MDQ36	I/O	GVDD
J7	VDD	Power	N/A
J8	VSS	Ground	N/A
J9	VDD	Power	N/A
J10	VSS	Ground	N/A
J11	VDD	Power	N/A
J12	VSS	Ground	N/A
J13	VDD	Power	N/A
J14	VSS	Ground	N/A
J15	VDD	Power	N/A
J16	VSS	Ground	N/A
J17	VDD	Power	N/A
J18	VSS	Ground	N/A
J19	VDD	Power	N/A
J20	VSS	Ground	N/A
J21	NVDD	Power	N/A
J22	GPIO24/TMR1/RCW_SRC2	I/O	NVDD
J23	GPIO9/$\overline{\text{IRQ9}}$/RC9	I/O	NVDD
J24	$\overline{\text{RCW\_LSEL0}}$/RC17	I/O	NVDD
J25	$\overline{\text{RCW\_LSEL3}}$/RC20	I/O	NVDD
J26	$\overline{\text{RCW\_LSEL2}}$/RC19	I/O	NVDD
J27	RC21	I	NVDD
J28	GPIO3/DRQ1/$\overline{\text{IRQ3}}$/RC3	I/O	NVDD
K1	$\overline{\text{MCAS}}$	O	GVDD
K2	$\overline{\text{MCS0}}$	O	GVDD
K3	$\overline{\text{MCS1}}$	O	GVDD
K4	MDQ39	I/O	GVDD
K5	MDQ32	I/O	GVDD
K6	MDQ34	I/O	GVDD
K7	VSS	Ground	N/A
K8	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
T11	VSS	Ground	N/A
T12	VDD	Power	N/A
T13	VSS	Ground	N/A
T14	VDD	Power	N/A
T15	VSS	Ground	N/A
T16	VDD	Power	N/A
T17	VSS	Ground	N/A
T18	VDD	Power	N/A
T19	VSS	Ground	N/A
T20	VDD	Power	N/A
T21	NC	NC	N/A
T22	NC	Non-user	N/A
T23	NC	Non-user	N/A
T24	NC	NC	N/A
T25	SXPVDD	Power	N/A
T26	SXPVSS	Ground	N/A
T27	$\overline{\text{SD\_C\_RX}}$	I	SXCVDD
T28	SD_C_RX	I	SXCVDD
U1	MAVDD	Power	N/A
U2	VSS	Ground	N/A
U3	MCK1	O	GVDD
U4	GVDD	Power	N/A
U5	VSS	Ground	N/A
U6	MBA1	O	GVDD
U7	GVDD	Power	N/A
U8	VSS	Ground	N/A
U9	VDD	Power	N/A
U10	VSS	Ground	N/A
U11	VDD	Power	N/A
U12	VSS	Ground	N/A
U13	VDD	Power	N/A
U14	VSS	Ground	N/A
U15	VDD	Power	N/A
U16	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
V23	NC	NC	N/A
V24	NC	NC	N/A
V25	NC	NC	N/A
V26	NC	NC	N/A
V27	$\overline{\text{SD\_D\_RX}}$	I	SXCVDD
V28	SD_D_RX	I	SXCVDD
W1	VSS	Ground	N/A
W2	VSS	Ground	N/A
W3	MA5	O	GVDD
W4	VSS	Ground	N/A
W5	GVDD	Power	N/A
W6	MMDIC1	I/O	GVDD
W7	GVDD	Power	N/A
W8	VSS	Ground	N/A
W9	VDD	Power	N/A
W10	VSS	Ground	N/A
W11	M3VDD	Power	N/A
W12	VSS	Ground	N/A
W13	M3VDD	Power	N/A
W14	VSS	Ground	N/A
W15	M3VDD	Power	N/A
W16	VSS	Ground	N/A
W17	CPRIVDD	Power	N/A
W18	VSS	Ground	N/A
W19	VDD	Power	N/A
W20	VSS	Ground	N/A
W21	NC	NC	N/A
W22	NC	NC	N/A
W23	NC	NC	N/A
W24	SD_PLL1_AVDD	Power	N/A
W25	SD_PLL1_AGND	Ground	N/A
W26	NC	NC	N/A
W27	SXCVSS	Ground	N/A
W28	SXCVDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AC19	NC	NC	N/A
AC20	NC	Non-user	N/A
AC21	NC	NC	N/A
AC22	NC	NC	N/A
AC23	NC	NC	N/A
AC24	NC	NC	N/A
AC25	SD_F_TX	O	SXPVDD
AC26	$\overline{\text{SD\_F\_TX}}$	O	SXPVDD
AC27	SXCVSS	Ground	N/A
AC28	SXCVDD	Power	N/A
AD1	MECC7	I/O	GVDD
AD2	MECC6	I/O	GVDD
AD3	MECC0	I/O	GVDD
AD4	MECC5	I/O	GVDD
AD5	MECC3	I/O	GVDD
AD6	MDQ24	I/O	GVDD
AD7	MDM0	O	GVDD
AD8	$\overline{\text{MDQS0}}$	I/O	GVDD
AD9	MDQS0	I/O	GVDD
AD10	MDQ4	I/O	GVDD
AD11	MDQ6	I/O	GVDD
AD12	VSS	Non-user	N/A
AD13	VSS	Non-user	N/A
AD14	VSS	Non-user	N/A
AD15	VSS	Ground	N/A
AD16	VSS	Ground	N/A
AD17	NC	NC	N/A
AD18	SD_PLL2_AVDD	Power	N/A
AD19	NC	NC	N/A
AD20	NC	NC	N/A
AD21	NC	NC	N/A
AD22	NC	NC	N/A
AD23	NC	NC	N/A
AD24	NC	NC	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
Y18	CPRIVDD	Power	N/A
N11	CRPEVDD	Power	N/A
N7	CRPEVDD	Power	N/A
N9	CRPEVDD	Power	N/A
P10	CRPEVDD	Power	N/A
P8	CRPEVDD	Power	N/A
R11	CRPEVDD	Power	N/A
C16	DFT_TEST	I	QVDD
A14	EE0	I	QVDD
C14	EE1	O	QVDD
B26	GE_MDC	O	NVDD
C27	GE_MDIO	I/O	NVDD
A23	GE1_GTX_CLK	O	NVDD
H22	GE1_RD0	I	NVDD
H24	GE1_RD1	I	NVDD
G21	GE1_RD2	I	NVDD
G20	GE1_RD3	I	NVDD
G22	GE1_RX_CLK	I	NVDD
G24	GE1_RX_CTL	I	NVDD
A24	GE1_TD0	O	NVDD
A27	GE1_TD1	O	NVDD
A26	GE1_TD2	O	NVDD
A28	GE1_TD3	O	NVDD
A25	GE1_TX_CLK	I	NVDD
A22	GE1_TX_CTL	O	NVDD
C21	GE2_GTX_CLK/CP_LOS4	I/O	NVDD
F21	GE2_RD0/CP_LOS6	I	NVDD
F23	GE2_RD1	I	NVDD
F19	GE2_RD2/CP_LOS1	I	NVDD
E20	GE2_RD3/CP_LOS2	I	NVDD
F22	GE2_RX_CLK	I	NVDD
F20	GE2_RX_CTL	I	NVDD
C24	GE2_TD0	O	NVDD
C23	GE2_TD1	O	NVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
E19	NVDD	Power	N/A
E23	NVDD	Power	N/A
G25	NVDD	Power	N/A
H20	NVDD	Power	N/A
H23	NVDD	Power	N/A
H27	NVDD	Power	N/A
J21	NVDD	Power	N/A
K25	NVDD	Power	N/A
L21	NVDD	Power	N/A
AH14	PLL0_AVDD	Power	N/A
AH15	PLL1_AVDD	Power	N/A
AH16	PLL2_AVDD	Power	N/A
C17	$\overline{\text{PORESET}}$	I	QVDD
G15	QVDD	Power	N/A
H14	QVDD	Power	N/A
J27	RC21	I	NVDD
J24	$\overline{\text{RCW\_LSEL0}}$/RC17	I/O	NVDD
K24	$\overline{\text{RCW\_LSEL1}}$/RC18	I/O	NVDD
J26	$\overline{\text{RCW\_LSEL2}}$/RC19	I/O	NVDD
J25	$\overline{\text{RCW\_LSEL3}}$/RC20	I/O	NVDD
M27	$\overline{\text{SD\_A\_RX}}$	I	SXCVDD
M28	SD_A_RX	I	SXCVDD
M23	SD_A_TX	O	SXPVDD
M24	$\overline{\text{SD\_A\_TX}}$	O	SXPVDD
P27	$\overline{\text{SD\_B\_RX}}$	I	SXCVDD
P28	SD_B_RX	I	SXCVDD
N25	SD_B_TX	O	SXPVDD
N26	$\overline{\text{SD\_B\_TX}}$	O	SXPVDD
T27	$\overline{\text{SD\_C\_RX}}$	I	SXCVDD
T28	SD_C_RX	I	SXCVDD
R25	SD_C_TX	O	SXPVDD
R26	$\overline{\text{SD\_C\_TX}}$	O	SXPVDD
V27	$\overline{\text{SD\_D\_RX}}$	I	SXCVDD
V28	SD_D_RX	I	SXCVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
J9	VDD	Power	N/A
K10	VDD	Power	N/A
K12	VDD	Power	N/A
K14	VDD	Power	N/A
K16	VDD	Power	N/A
K18	VDD	Power	N/A
K20	VDD	Power	N/A
K8	VDD	Power	N/A
L11	VDD	Power	N/A
L13	VDD	Power	N/A
L15	VDD	Power	N/A
L17	VDD	Power	N/A
L19	VDD	Power	N/A
L7	VDD	Power	N/A
L9	VDD	Power	N/A
M10	VDD	Power	N/A
M12	VDD	Power	N/A
M14	VDD	Power	N/A
M16	VDD	Power	N/A
M18	VDD	Power	N/A
M20	VDD	Power	N/A
M8	VDD	Power	N/A
N13	VDD	Power	N/A
N15	VDD	Power	N/A
N17	VDD	Power	N/A
N19	VDD	Power	N/A
P12	VDD	Power	N/A
P14	VDD	Power	N/A
P16	VDD	Power	N/A
P18	VDD	Power	N/A
P20	VDD	Power	N/A
R13	VDD	Power	N/A
R15	VDD	Power	N/A
R17	VDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AA2	VSS	Ground	N/A
AA5	VSS	Ground	N/A
AA8	VSS	Ground	N/A
AB11	VSS	Ground	N/A
AB13	VSS	Ground	N/A
AB15	VSS	Ground	N/A
AB17	VSS	Ground	N/A
AC1	VSS	Ground	N/A
AC10	VSS	Ground	N/A
AC12	VSS	Ground	N/A
AC14	VSS	Ground	N/A
AC16	VSS	Ground	N/A
AC4	VSS	Ground	N/A
AC7	VSS	Ground	N/A
AD12	VSS	Non-user	N/A
AD13	VSS	Non-user	N/A
AD14	VSS	Non-user	N/A
AD15	VSS	Ground	N/A
AD16	VSS	Ground	N/A
AE11	VSS	Ground	N/A
AE13	VSS	Non-user	N/A
AE14	VSS	Ground	N/A
AE15	VSS	Ground	N/A
AE16	VSS	Ground	N/A
AE2	VSS	Ground	N/A
AE5	VSS	Ground	N/A
AE8	VSS	Ground	N/A
AF13	VSS	Non-user	N/A
AF14	VSS	Ground	N/A
AF15	VSS	Ground	N/A
AF16	VSS	Ground	N/A
AG1	VSS	Ground	N/A
AG10	VSS	Ground	N/A
AG13	VSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AG14	VSS	Ground	N/A
AG15	VSS	Ground	N/A
AG16	VSS	Ground	N/A
AG4	VSS	Ground	N/A
AG7	VSS	Ground	N/A
AH13	VSS	Ground	N/A
B11	VSS	Ground	N/A
B13	VSS	Ground	N/A
B16	VSS	Ground	N/A
B17	VSS	Ground	N/A
B18	VSS	Ground	N/A
B19	VSS	Ground	N/A
B21	VSS	Ground	N/A
B22	VSS	Non-user	N/A
B23	VSS	Ground	N/A
B25	VSS	Ground	N/A
B27	VSS	Ground	N/A
B9	VSS	Ground	N/A
C1	VSS	Ground	N/A
C18	VSS	Ground	N/A
C4	VSS	Ground	N/A
C7	VSS	Ground	N/A
D11	VSS	Ground	N/A
D13	VSS	Ground	N/A
D16	VSS	Ground	N/A
D18	VSS	Ground	N/A
D19	VSS	Non-user	N/A
D23	VSS	Ground	N/A
D9	VSS	Ground	N/A
E18	VSS	Ground	N/A
E2	VSS	Ground	N/A
E21	VSS	Ground	N/A
E22	VSS	Non-user	N/A
E25	VSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
E5	VSS	Ground	N/A
E8	VSS	Ground	N/A
F13	VSS	Ground	N/A
F16	VSS	Ground	N/A
F18	VSS	Ground	N/A
F9	VSS	Ground	N/A
G1	VSS	Ground	N/A
G10	VSS	Ground	N/A
G18	VSS	Ground	N/A
G23	VSS	Ground	N/A
G27	VSS	Ground	N/A
G4	VSS	Ground	N/A
G8	VSS	Ground	N/A
H11	VSS	Ground	N/A
H12	VSS	Non-user	N/A
H15	VSS	Ground	N/A
H17	VSS	Ground	N/A
H19	VSS	Ground	N/A
H21	VSS	Ground	N/A
H25	VSS	Ground	N/A
H7	VSS	Ground	N/A
H9	VSS	Ground	N/A
J10	VSS	Ground	N/A
J12	VSS	Ground	N/A
J14	VSS	Ground	N/A
J16	VSS	Ground	N/A
J18	VSS	Ground	N/A
J2	VSS	Ground	N/A
J20	VSS	Ground	N/A
J8	VSS	Ground	N/A
K11	VSS	Ground	N/A
K13	VSS	Ground	N/A
K15	VSS	Ground	N/A
K17	VSS	Ground	N/A

Table 17. Serial RapidIO Transmitter DC Specifications for Short Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	400	—	750	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b001101
Differential resistance	T_Rd	80	100	120	Ω	—

Table 18. Serial RapidIO Receiver DC Specifications for Short Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units
Input differential voltage	R_Vdiff	125	—	1200	mV
Differential resistance	R_Rdin	80	—	120	Ω

Table 19. Serial RapidIO Transmitter DC Specifications for Long Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Conditions
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	800	—	1200	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b000000 (with de-emphasis disabled)
De-emphasized differential output voltage	$T\_V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3	3.5	4	dB	• p(n)_(y)_tx_eq_type[1:0] = 01 • p(n)_(y)_tx_ratio_post1q[3:0] = 1110
Tx De-emphasized level	$T\_V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6	6.5	dB	• p(n)_(y)_tx_eq_type[1:0] = 01 • p(n)_(y)_tx_ratio_post1q[3:0] = 1100
Differential resistance	T_Rd	80	100	120	Ω	—

Table 20. Serial RapidIO Receiver DC Specifications for Long Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Condition
Input differential voltage	R_Vdiff	N/A	—	1200	mV	It is assumed that for the R_Vdiff min specification, that the eye can be closed at the receiver after passing the signal through a CEI/SRIO Level II LR compliant channel.
Differential resistance	R_Rdin	80	—	120	Ω	—

Figure 8 shows the DDR3 SDRAM interface input timing diagram.

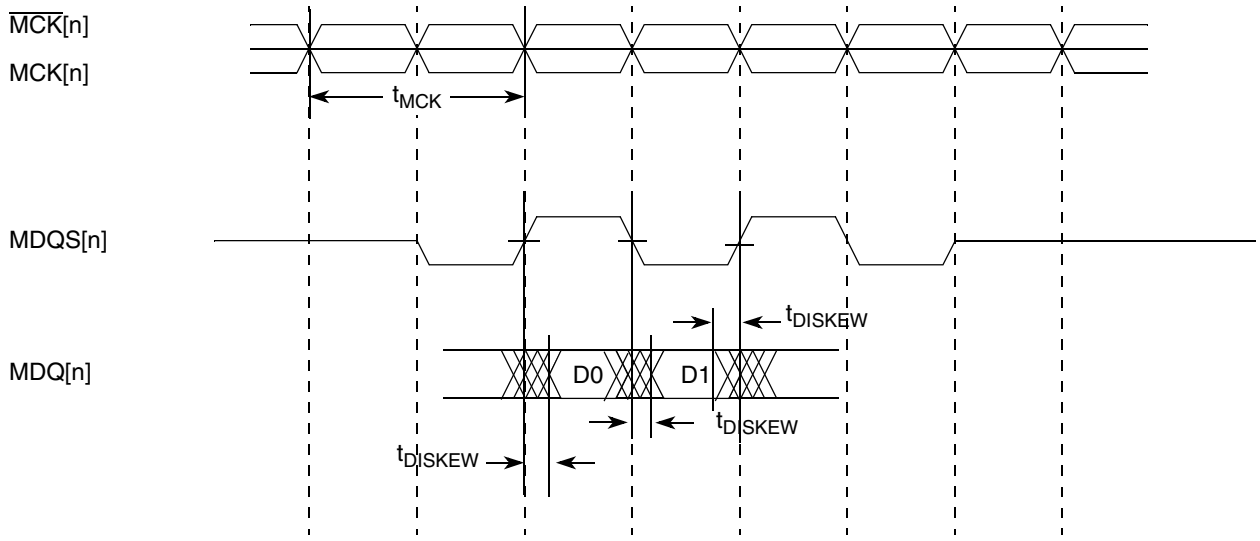

Figure 8. DDR3 SDRAM Interface Input Timing Diagram

3.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 30 provides the output AC timing specifications for the DDR SDRAM interface.

Table 30. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1.5	3	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	
$\overline{\text{MCS}}$n output setup with respect to MCK	t_{DDKHCS}				3
• 1333 MHz data rate		0.606	—	ns	
• 1200 MHz data rate		0.675	—	ns	
• 1066 MHz data rate		0.744	—	ns	
• 800 MHz data rate		0.917	—	ns	
• 667 MHz data rate		1.10	—	ns	

Table 30. DDR SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$n output hold with respect to MCK • 1333 MHz data rate • 1200 MHz data rate • 1066 MHz data rate • 800 MHz data rate • 667 MHz data rate	t_{DDKHCX}	 0.606 0.675 0.744 0.917 1.10	 — — — — —	 ns ns ns ns ns	3
MCK to MDQS Skew • > 1066 MHz data rate • 800 MHz data rate • 667 MHz data rate	t_{DDKHMH}	 –0.245 –0.375 –0.6	 0.245 0.375 0.6	 ns ns ns	4
MDQ/MECC/MDM output setup with respect to MDQS • 1333 MHz data rate • 1200 MHz data rate • 1066 MHz data rate • 800 MHz data rate • 667 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 250 275 300 375 450	 — — — — —	 ps ps ps ps ps	5, 6
MDQ/MECC/MDM output hold with respect to MDQS • 1333 MHz data rate • 1200 MHz data rate • 1066 MHz data rate • 800 MHz data rate • 667 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 250 275 300 375 450	 — — — — —	 ps ps ps ps ps	5
MDQS preamble	t_{DDKHMP}	0.9 × t_{MCK}	—	ns	—
MDQS postamble	t_{DDKHME}	0.4 × t_{MCK}	0.6 × t_{MCK}	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MSC8157 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8157.
6. At recommended operating conditions with V_{DDDDR} (1.5 V) ± 5%.

NOTE

For the ADDR/CMD setup and hold specifications in Table 30, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Table 45. CPRI Receiver AC Timing Specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps) (continued)

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	ps
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	ps
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	ps
Bit error ratio	BER	—	—	10^{-12}	—

Table 46 defines the receiver AC specifications for CPRI LV-II. The AC timing specifications do not include REF_CLK jitter.

Table 46. CPRI Receiver AC Timing Specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit
Gaussian	R_GJ	—	—	0.275	UI p-p
Uncorrelated bounded high probability jitter	R_UBHPJ	—	—	0.150	UI p-p
Correlated bounded high probability jitter	R_CBHPJ	—	—	0.525	UI p-p
Bounded high probability jitter	R_BHPJ	—	—	0.675	UI p-p
Sinusoidal jitter, maximum	R_SJ-max	—	—	5.000	UI p-p
Sinusoidal jitter, high frequency	R_SJ-hf	—	—	0.050	UI p-p
Total Jitter (does not include sinusoidal jitter).	R_TJ	—	—	0.950	UI p-p
Unit Interval: 1.2288 GBaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	µs
Unit Interval: 2.4576 GBaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	µs
Unit Interval: 3.072 GBaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	µs
Unit Interval: 4.9152 GBaud	UI	1/4915.2 – 100ppm	1/4915.2.8	1/4915.2 + 100ppm	µs
Unit Interval: 6.144 GBaud	UI	1/6144.0 – 100ppm	1/6144.0	1/6144.0 + 100ppm	µs

Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 17. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PC trace.

NOTE

The intended application is a point-to-point interface up to two connectors. The maximum allowed total loss (channel + interconnects + other loss) is 20.4 dB @ 6.144 Gbps.

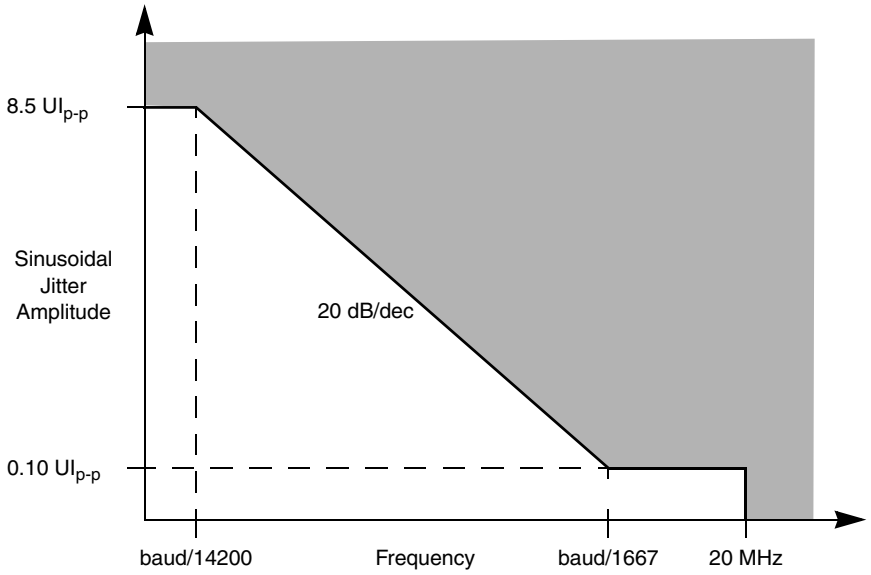

Figure 19. Single Frequency Sinusoidal Jitter Limits for Baud Rate for <3.125 Gbps

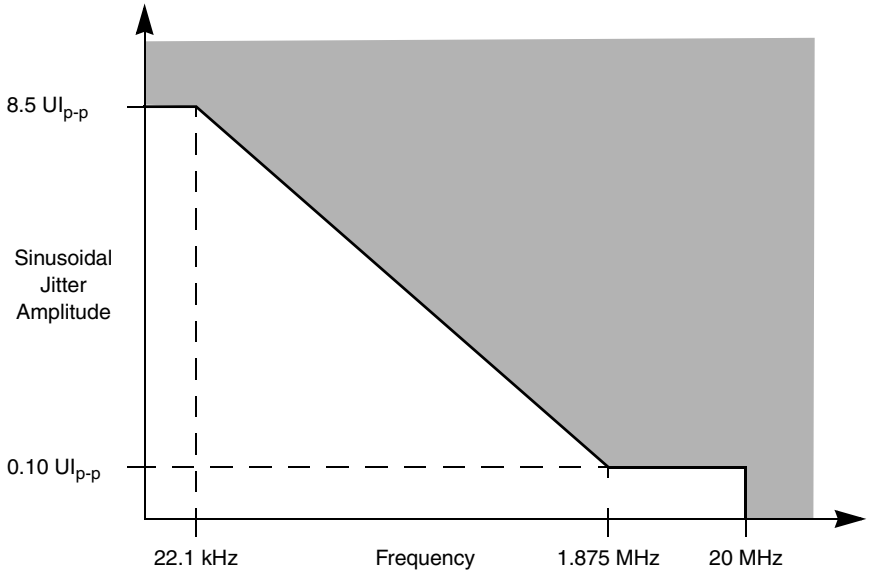

Figure 20. Single Frequency Sinusoidal Jitter Limits for Baud Rate for 3.125 Gbps

3.6.3 Timers and Timers_32b AC Timing Specifications

Table 49 lists the timer input AC timing specifications.

Table 49. Timers Input AC Timing Specifications

At recommended operating conditions (see Table 4).

Characteristics	Symbol	Minimum	Unit	Notes
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Notes:
1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 21 shows the AC test load for the timers

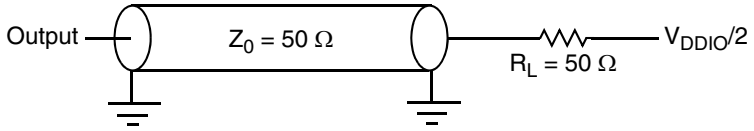

Figure 21. Timer AC Test Load

3.6.4 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are three general configuration registers used to configure the timing: GCR4, UCC1_DELAY_HR, and UCC3_DELAY_HR. These registers configure the programmable delay units (PDU) that should be programmed differently for each Interface to meet timing requirements. For additional information, see the *MSC8157 Reference Manual*.

3.6.4.1 Management Interface Timing

Table 50. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
GE_MDC frequency	f_{MDC}	—	2.5	MHz
GE_MDC period	t_{MDC}	400	—	ns
GE_MDC clock pulse width high	t_{MDC_H}	160	—	ns
GE_MDC clock pulse width low	t_{MDC_L}	160	—	ns
GE_MDC to GE_MDIO delay	t_{MDKHDX}	10	70	ns
GE_MDIO to GE_MDC rising edge setup time	t_{MDDVKH}	20	—	ns
GE_MDC rising edge to GE_MDIO hold time	t_{MDDXKH}	0	—	ns

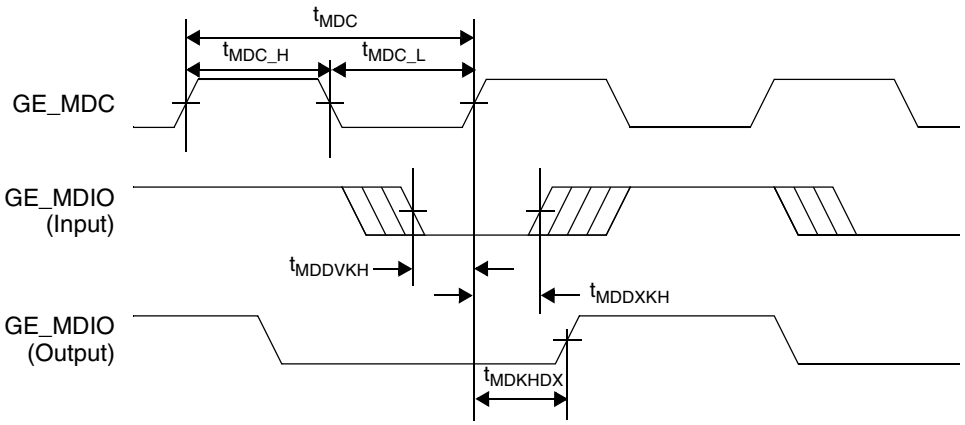

Figure 22. MII Management Interface Timing

3.6.4.2 RGMII AC Timing Specifications

Table 51 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 51. RGMII at 1 Gbps with On-Board Delay[2] AC Timing Specifications[1]

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[3]	t_{SKEWT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver)[3]	t_{SKEWR}	1	—	2.6	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. Program GCR4 as 0x00000000, UCC1_DELAY_HR as 0x00000000, and UCC3_DELAY_HR as 0x00000000.
3. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Figure 23 shows the RGMII AC timing and multiplexing diagrams.

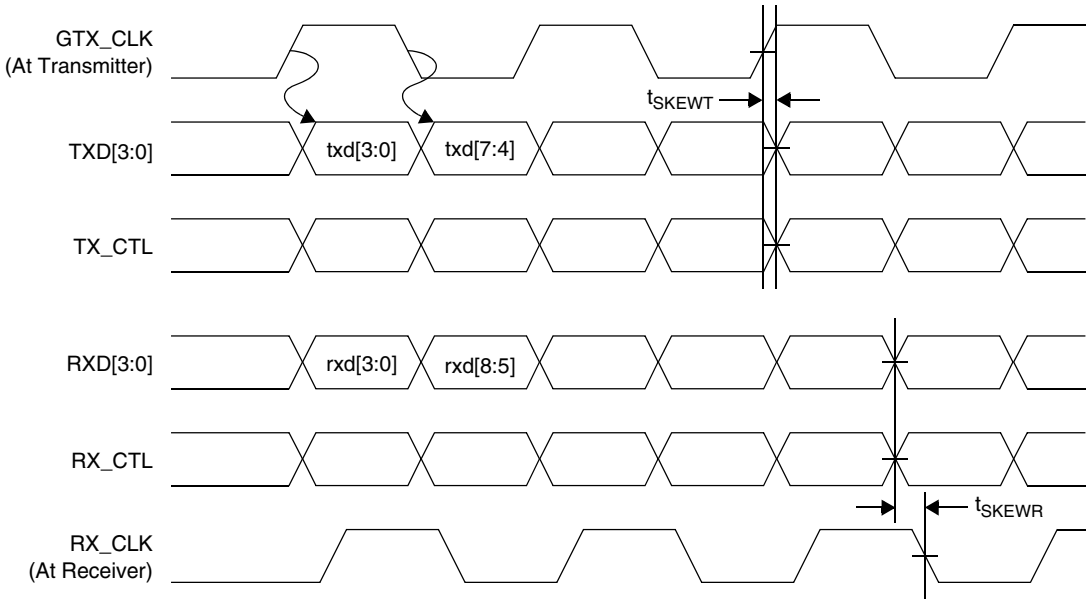

Figure 23. RGMII AC Timing and Multiplexing

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