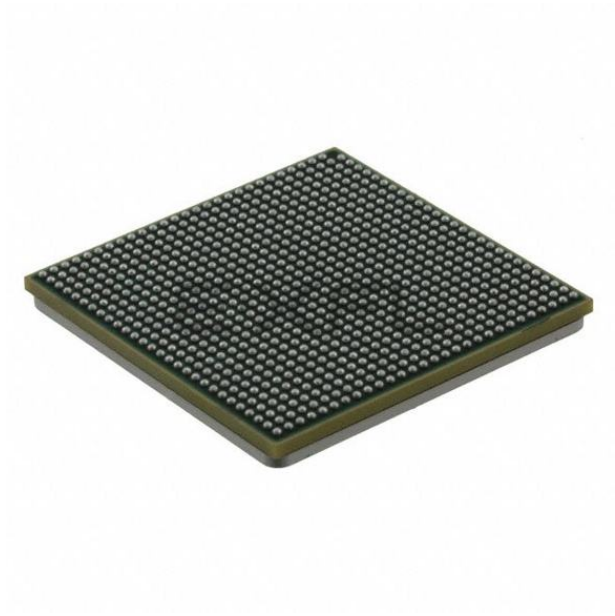

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	6.375MB
Voltage - I/O	1.0V, 1.5V, 2.5V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8157svt1000a

NOTE

See Figure 31 as a reference for correct ball grid layout.

2.2 Signal Lists

Table 1 presents the signal list sorted by ball number. Table 2 presents the signal list by signal name. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

NOTE

The information in Table 1 distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

Table 1. Signal List by Ball Number

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
A2	VSS	Ground	N/A
A3	MDQ57	I/O	GVDD
A4	GVDD	Power	N/A
A5	VSS	Ground	N/A
A6	MDQ63	I/O	GVDD
A7	GVDD	Power	N/A
A8	NC	Non-user	N/A
A9	NC	Non-user	N/A
A10	NC	Non-user	N/A
A11	NC	Non-user	N/A
A12	NC	Non-user	N/A
A13	CLKOUT	O	QVDD
A14	EE0	I	QVDD
A15	VSS	Ground	N/A
A16	MCLKIN (optional)	I	QVDD
A17	VSS	Ground	N/A
A18	CLKIN	I	QVDD
A19	VSS	Ground	N/A
A20	GPIO29/UART_TXD/CP_LOS2	I/O	NVDD
A21	GPIO31/I2C_SDA	I/O	NVDD
A22	GE1_TX_CTL	O	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
J3	MDQ35	I/O	GVDD
J4	GVDD	Power	N/A
J5	MDQ33	I/O	GVDD
J6	MDQ36	I/O	GVDD
J7	VDD	Power	N/A
J8	VSS	Ground	N/A
J9	VDD	Power	N/A
J10	VSS	Ground	N/A
J11	VDD	Power	N/A
J12	VSS	Ground	N/A
J13	VDD	Power	N/A
J14	VSS	Ground	N/A
J15	VDD	Power	N/A
J16	VSS	Ground	N/A
J17	VDD	Power	N/A
J18	VSS	Ground	N/A
J19	VDD	Power	N/A
J20	VSS	Ground	N/A
J21	NVDD	Power	N/A
J22	GPIO24/TMR1/RCW_SRC2	I/O	NVDD
J23	GPIO9/$\overline{\text{IRQ9}}$/RC9	I/O	NVDD
J24	$\overline{\text{RCW\_LSEL0}}$/RC17	I/O	NVDD
J25	$\overline{\text{RCW\_LSEL3}}$/RC20	I/O	NVDD
J26	$\overline{\text{RCW\_LSEL2}}$/RC19	I/O	NVDD
J27	RC21	I	NVDD
J28	GPIO3/DRQ1/$\overline{\text{IRQ3}}$/RC3	I/O	NVDD
K1	$\overline{\text{MCAS}}$	O	GVDD
K2	$\overline{\text{MCS0}}$	O	GVDD
K3	$\overline{\text{MCS1}}$	O	GVDD
K4	MDQ39	I/O	GVDD
K5	MDQ32	I/O	GVDD
K6	MDQ34	I/O	GVDD
K7	VSS	Ground	N/A
K8	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
T11	VSS	Ground	N/A
T12	VDD	Power	N/A
T13	VSS	Ground	N/A
T14	VDD	Power	N/A
T15	VSS	Ground	N/A
T16	VDD	Power	N/A
T17	VSS	Ground	N/A
T18	VDD	Power	N/A
T19	VSS	Ground	N/A
T20	VDD	Power	N/A
T21	NC	NC	N/A
T22	NC	Non-user	N/A
T23	NC	Non-user	N/A
T24	NC	NC	N/A
T25	SXPVDD	Power	N/A
T26	SXPVSS	Ground	N/A
T27	$\overline{\text{SD\_C\_RX}}$	I	SXCVDD
T28	SD_C_RX	I	SXCVDD
U1	MAVDD	Power	N/A
U2	VSS	Ground	N/A
U3	MCK1	O	GVDD
U4	GVDD	Power	N/A
U5	VSS	Ground	N/A
U6	MBA1	O	GVDD
U7	GVDD	Power	N/A
U8	VSS	Ground	N/A
U9	VDD	Power	N/A
U10	VSS	Ground	N/A
U11	VDD	Power	N/A
U12	VSS	Ground	N/A
U13	VDD	Power	N/A
U14	VSS	Ground	N/A
U15	VDD	Power	N/A
U16	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
U17	VDD	Power	N/A
U18	VSS	Ground	N/A
U19	VDD	Power	N/A
U20	VSS	Ground	N/A
U21	NC	NC	N/A
U22	NC	NC	N/A
U23	NC	NC	N/A
U24	NC	NC	N/A
U25	SD_D_TX	O	SXPVDD
U26	$\overline{\text{SD\_D\_TX}}$	O	SXPVDD
U27	SXCVSS	Ground	N/A
U28	SXCVDD	Power	N/A
V1	MVREF	Power	N/A
V2	VSS	Ground	N/A
V3	MA8	O	GVDD
V4	MA2	O	GVDD
V5	MA6	O	GVDD
V6	MCKE1	O	GVDD
V7	VSS	Ground	N/A
V8	GVDD	Power	N/A
V9	VSS	Ground	N/A
V10	VDD	Power	N/A
V11	VSS	Ground	N/A
V12	VDD	Power	N/A
V13	VSS	Ground	N/A
V14	VDD	Power	N/A
V15	VSS	Ground	N/A
V16	VDD	Power	N/A
V17	VSS	Ground	N/A
V18	VDD	Power	N/A
V19	VSS	Ground	N/A
V20	VDD	Power	N/A
V21	NC	NC	N/A
V22	NC	NC	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AH15	PLL1_AVDD	Power	N/A
AH16	PLL2_AVDD	Power	N/A
AH17	NC	NC	N/A
AH18	SXCVDD	Power	N/A
AH19	SD_REF_CLK2	I	SXCVDD
AH20	SXCVDD	Power	N/A
AH21	SD_J_RX	I	SXCVDD
AH22	SXCVDD	Power	N/A
AH23	SD_I_RX	I	SXCVDD
AH24	SXCVDD	Power	N/A
AH25	SXPVDD	Power	N/A
AH26	SXPVSS	Ground	N/A
AH27	$\overline{\text{SD\_H\_RX}}$	I	SXCVDD
AH28	SD_H_RX	I	SXCVDD

Notes:
1. Signal function during power-on reset is determined by the RCW source type. Selection of RapidIO, SGMII, CPRI, and PCI Express functionality during normal operation is configured by the RCW bit values. Selection of the GPIO function and other functions is done by GPIO register setup. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. For configuration details, see the *GPIO* chapter in the *MSC8157 Reference Manual*.
2. NC signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS or SXCVSS), or pulled up (VDD).
3. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected; non-user = connect as specified under Signal Name.
4. Connect power inputs to the power supplies via external filters. See the *MSC8157 Design Checklist* (AN4110) for details.

Table 2. Signal List by Primary Signal Name

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
A18	CLKIN	I	QVDD
A13	CLKOUT	O	QVDD
AA15	CPRIVDD	Power	N/A
AA17	CPRIVDD	Power	N/A
AA19	CPRIVDD	Power	N/A
AB16	CPRIVDD	Power	N/A
AB18	CPRIVDD	Power	N/A
AC15	CPRIVDD	Power	N/A
W17	CPRIVDD	Power	N/A
Y16	CPRIVDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
U1	MAVDD	Power	N/A
R6	MBA0	O	GVDD
U6	MBA1	O	GVDD
AB7	MBA2	O	GVDD
K1	$\overline{\text{MCAS}}$	O	GVDD
M1	$\overline{\text{MCK0}}$	O	GVDD
M2	MCK0	O	GVDD
T3	$\overline{\text{MCK1}}$	O	GVDD
U3	MCK1	O	GVDD
P1	$\overline{\text{MCK2}}$	O	GVDD
R1	MCK2	O	GVDD
AA7	MCKE0	O	GVDD
V6	MCKE1	O	GVDD
A16	MCLKIN (optional)	I	QVDD
K2	$\overline{\text{MCS0}}$	O	GVDD
K3	$\overline{\text{MCS1}}$	O	GVDD
AD7	MDM0	O	GVDD
AH12	MDM1	O	GVDD
AH4	MDM2	O	GVDD
AH7	MDM3	O	GVDD
L6	MDM4	O	GVDD
G3	MDM5	O	GVDD
F7	MDM6	O	GVDD
C6	MDM7	O	GVDD
AB2	MDM8	O	GVDD
AB10	MDQ0	I/O	GVDD
AB9	MDQ1	I/O	GVDD
AF12	MDQ10	I/O	GVDD
AF10	MDQ11	I/O	GVDD
AG12	MDQ12	I/O	GVDD
AG9	MDQ13	I/O	GVDD
AF9	MDQ14	I/O	GVDD
AH11	MDQ15	I/O	GVDD
AF4	MDQ16	I/O	GVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
D2	MDQ48	I/O	GVDD
D1	MDQ49	I/O	GVDD
AE9	MDQ5	I/O	GVDD
D5	MDQ50	I/O	GVDD
D6	MDQ51	I/O	GVDD
D7	MDQ52	I/O	GVDD
E1	MDQ53	I/O	GVDD
E6	MDQ54	I/O	GVDD
E3	MDQ55	I/O	GVDD
B7	MDQ56	I/O	GVDD
A3	MDQ57	I/O	GVDD
B6	MDQ58	I/O	GVDD
B2	MDQ59	I/O	GVDD
AD11	MDQ6	I/O	GVDD
B1	MDQ60	I/O	GVDD
C3	MDQ61	I/O	GVDD
B5	MDQ62	I/O	GVDD
A6	MDQ63	I/O	GVDD
AF8	MDQ7	I/O	GVDD
AF11	MDQ8	I/O	GVDD
AE12	MDQ9	I/O	GVDD
AD8	$\overline{\text{MDQS0}}$	I/O	GVDD
AD9	MDQS0	I/O	GVDD
AH10	MDQS1	I/O	GVDD
AH9	$\overline{\text{MDQS1}}$	I/O	GVDD
AE1	MDQS2	I/O	GVDD
AF1	$\overline{\text{MDQS2}}$	I/O	GVDD
AH5	$\overline{\text{MDQS3}}$	I/O	GVDD
AH6	MDQS3	I/O	GVDD
H2	$\overline{\text{MDQS4}}$	I/O	GVDD
H3	MDQS4	I/O	GVDD
F3	$\overline{\text{MDQS5}}$	I/O	GVDD
F4	MDQS5	I/O	GVDD
D3	$\overline{\text{MDQS6}}$	I/O	GVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AB24	NC	NC	N/A
AB5	NC	Non-user	N/A
AC17	NC	NC	N/A
AC18	NC	NC	N/A
AC19	NC	NC	N/A
AC20	NC	Non-user	N/A
AC21	NC	NC	N/A
AC22	NC	NC	N/A
AC23	NC	NC	N/A
AC24	NC	NC	N/A
AD17	NC	NC	N/A
AD19	NC	NC	N/A
AD20	NC	NC	N/A
AD21	NC	NC	N/A
AD22	NC	NC	N/A
AD23	NC	NC	N/A
AD24	NC	NC	N/A
AE17	NC	NC	N/A
AE19	NC	NC	N/A
AE24	NC	NC	N/A
AF17	NC	NC	N/A
AF18	NC	NC	N/A
AF19	NC	NC	N/A
AF24	NC	NC	N/A
AG17	NC	NC	N/A
AH17	NC	NC	N/A
B10	NC	Non-user	N/A
B12	NC	Non-user	N/A
B8	NC	Non-user	N/A
C10	NC	Non-user	N/A
C11	NC	Non-user	N/A
C12	NC	Non-user	N/A
C13	NC	Non-user	N/A
C15	NC	Non-user	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
C8	NC	Non-user	N/A
C9	NC	Non-user	N/A
D10	NC	Non-user	N/A
D12	NC	Non-user	N/A
D14	NC	Non-user	N/A
D8	NC	Non-user	N/A
E10	NC	Non-user	N/A
E11	NC	Non-user	N/A
E12	NC	Non-user	N/A
E13	NC	Non-user	N/A
E14	NC	Non-user	N/A
E9	NC	Non-user	N/A
F11	NC	Non-user	N/A
F12	NC	Non-user	N/A
F14	NC	Non-user	N/A
G11	NC	Non-user	N/A
G12	NC	Non-user	N/A
G13	NC	Non-user	N/A
G14	NC	Non-user	N/A
H13	NC	Non-user	N/A
L22	NC	NC	N/A
L23	NC	NC	N/A
L3	NC	Non-user	N/A
M21	NC	NC	N/A
M22	NC	NC	N/A
M5	NC	Non-user	N/A
M6	NC	Non-user	N/A
N21	NC	NC	N/A
N22	NC	NC	N/A
N3	NC	Non-user	N/A
P21	NC	NC	N/A
P23	NC	NC	N/A
P24	NC	NC	N/A
P3	NC	Non-user	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
E19	NVDD	Power	N/A
E23	NVDD	Power	N/A
G25	NVDD	Power	N/A
H20	NVDD	Power	N/A
H23	NVDD	Power	N/A
H27	NVDD	Power	N/A
J21	NVDD	Power	N/A
K25	NVDD	Power	N/A
L21	NVDD	Power	N/A
AH14	PLL0_AVDD	Power	N/A
AH15	PLL1_AVDD	Power	N/A
AH16	PLL2_AVDD	Power	N/A
C17	$\overline{\text{PORESET}}$	I	QVDD
G15	QVDD	Power	N/A
H14	QVDD	Power	N/A
J27	RC21	I	NVDD
J24	$\overline{\text{RCW\_LSEL0}}$/RC17	I/O	NVDD
K24	$\overline{\text{RCW\_LSEL1}}$/RC18	I/O	NVDD
J26	$\overline{\text{RCW\_LSEL2}}$/RC19	I/O	NVDD
J25	$\overline{\text{RCW\_LSEL3}}$/RC20	I/O	NVDD
M27	$\overline{\text{SD\_A\_RX}}$	I	SXCVDD
M28	SD_A_RX	I	SXCVDD
M23	SD_A_TX	O	SXPVDD
M24	$\overline{\text{SD\_A\_TX}}$	O	SXPVDD
P27	$\overline{\text{SD\_B\_RX}}$	I	SXCVDD
P28	SD_B_RX	I	SXCVDD
N25	SD_B_TX	O	SXPVDD
N26	$\overline{\text{SD\_B\_TX}}$	O	SXPVDD
T27	$\overline{\text{SD\_C\_RX}}$	I	SXCVDD
T28	SD_C_RX	I	SXCVDD
R25	SD_C_TX	O	SXPVDD
R26	$\overline{\text{SD\_C\_TX}}$	O	SXPVDD
V27	$\overline{\text{SD\_D\_RX}}$	I	SXCVDD
V28	SD_D_RX	I	SXCVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AG19	$\overline{\text{SD\_REF\_CLK2}}$	I	SXCVDD
AH19	SD_REF_CLK2	I	SXCVDD
G16	STOP_BS	I	QVDD
AA28	SXCVDD	Power	N/A
AC28	SXCVDD	Power	N/A
AE28	SXCVDD	Power	N/A
AG28	SXCVDD	Power	N/A
AH18	SXCVDD	Power	N/A
AH20	SXCVDD	Power	N/A
AH22	SXCVDD	Power	N/A
AH24	SXCVDD	Power	N/A
L28	SXCVDD	Power	N/A
N28	SXCVDD	Power	N/A
R28	SXCVDD	Power	N/A
U28	SXCVDD	Power	N/A
W28	SXCVDD	Power	N/A
AA27	SXCVSS	Ground	N/A
AC27	SXCVSS	Ground	N/A
AE27	SXCVSS	Ground	N/A
AG18	SXCVSS	Ground	N/A
AG20	SXCVSS	Ground	N/A
AG22	SXCVSS	Ground	N/A
AG24	SXCVSS	Ground	N/A
AG27	SXCVSS	Ground	N/A
L27	SXCVSS	Ground	N/A
N27	SXCVSS	Ground	N/A
R27	SXCVSS	Ground	N/A
U27	SXCVSS	Ground	N/A
W27	SXCVSS	Ground	N/A
AB25	SXPVDD	Power	N/A
AD25	SXPVDD	Power	N/A
AE21	SXPVDD	Power	N/A
AE23	SXPVDD	Power	N/A
AF25	SXPVDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AG14	VSS	Ground	N/A
AG15	VSS	Ground	N/A
AG16	VSS	Ground	N/A
AG4	VSS	Ground	N/A
AG7	VSS	Ground	N/A
AH13	VSS	Ground	N/A
B11	VSS	Ground	N/A
B13	VSS	Ground	N/A
B16	VSS	Ground	N/A
B17	VSS	Ground	N/A
B18	VSS	Ground	N/A
B19	VSS	Ground	N/A
B21	VSS	Ground	N/A
B22	VSS	Non-user	N/A
B23	VSS	Ground	N/A
B25	VSS	Ground	N/A
B27	VSS	Ground	N/A
B9	VSS	Ground	N/A
C1	VSS	Ground	N/A
C18	VSS	Ground	N/A
C4	VSS	Ground	N/A
C7	VSS	Ground	N/A
D11	VSS	Ground	N/A
D13	VSS	Ground	N/A
D16	VSS	Ground	N/A
D18	VSS	Ground	N/A
D19	VSS	Non-user	N/A
D23	VSS	Ground	N/A
D9	VSS	Ground	N/A
E18	VSS	Ground	N/A
E2	VSS	Ground	N/A
E21	VSS	Ground	N/A
E22	VSS	Non-user	N/A
E25	VSS	Ground	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
P11	VSS	Ground	N/A
P13	VSS	Ground	N/A
P15	VSS	Ground	N/A
P17	VSS	Ground	N/A
P19	VSS	Ground	N/A
P7	VSS	Ground	N/A
P9	VSS	Ground	N/A
R10	VSS	Ground	N/A
R12	VSS	Ground	N/A
R14	VSS	Ground	N/A
R16	VSS	Ground	N/A
R18	VSS	Ground	N/A
R20	VSS	Ground	N/A
R4	VSS	Ground	N/A
R8	VSS	Ground	N/A
T1	VSS	Ground	N/A
T11	VSS	Ground	N/A
T13	VSS	Ground	N/A
T15	VSS	Ground	N/A
T17	VSS	Ground	N/A
T19	VSS	Ground	N/A
T2	VSS	Ground	N/A
T7	VSS	Ground	N/A
T9	VSS	Ground	N/A
U10	VSS	Ground	N/A
U12	VSS	Ground	N/A
U14	VSS	Ground	N/A
U16	VSS	Ground	N/A
U18	VSS	Ground	N/A
U2	VSS	Ground	N/A
U20	VSS	Ground	N/A
U5	VSS	Ground	N/A
U8	VSS	Ground	N/A
V11	VSS	Ground	N/A

3.2 Recommended Operating Conditions

Table 4 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 4. Recommended Operating Conditions

Rating	Supply	Min	Nominal	Max	Unit
Core supply voltage[1]	VDD	0.97	1.0	1.05	V
PLL supply voltage[1,3]	PLL0_AVDD PLL1_AVDD PLL2_AVDD MAVDD SD_PLL1_AVDD SD_PLL2_AVDD	0.97	1.0	1.05	V
CRPE supply voltage[1]	CRPEVDD	0.97	1.0	1.05	V
CPRI supply voltage[1]	CPRIVDD	0.97	1.0	1.05	V
Switchable M3 memory supply voltage[1]	M3VDD	0.97	1.0	1.05	V
DDR memory supply voltage DDR reference voltage	GVDD MVREF	1.425 0.49 × GVDD (nom)	1.5 0.5 × GVDD (nom)	1.575 0.51 × GVDD (nom)	V V
RGMII Ethernet and GPIO supply voltage[2]	NVDD	2.375	2.5	2.625	V
Input/output clocks, reset signal, and JTAG supply voltage[2]	QVDD	2.375	2.5	2.625	V
SerDes pad supply voltage	SXPVDD	1.425	1.5	1.575	V
SerDes core supply voltage[1]	SXCVDD	0.97	1.0	1.05	V
Operating temperature range: • Standard • Extended	 T_J T_A T_J	 0 –40 —		 105 — 105	 °C °C °C

Notes: 1. Designates supplies that use the same 1.0 V nominal voltage level.
2. Designates supplies that use the same 2.5 V nominal voltage level.
3. PLL supply voltage is specified at the input of the filter and not at the MSC8157 pin for the supply.

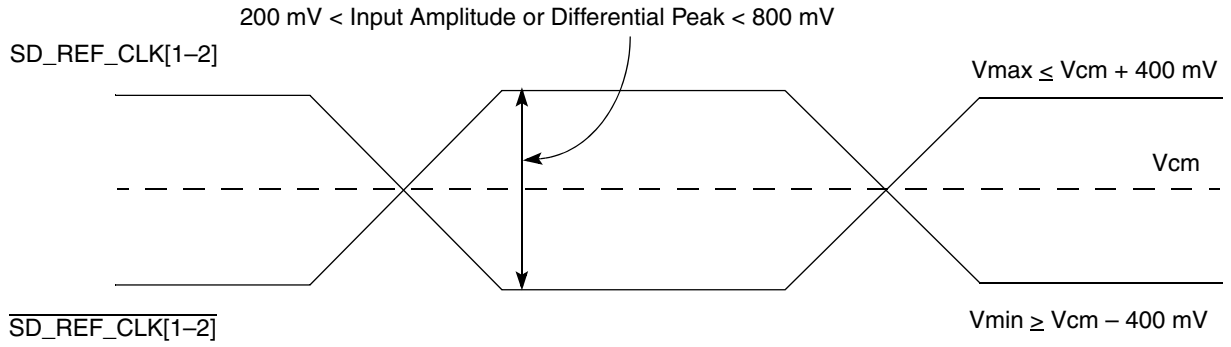

Figure 6. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD_REF_CLK[1–2] input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK[1–2]}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK[1–2] input average voltage must be between 200 and 400 mV. Figure 7 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK[1–2]}}$) through the same source impedance as the clock input (SD_REF_CLK[1–2]) in use.

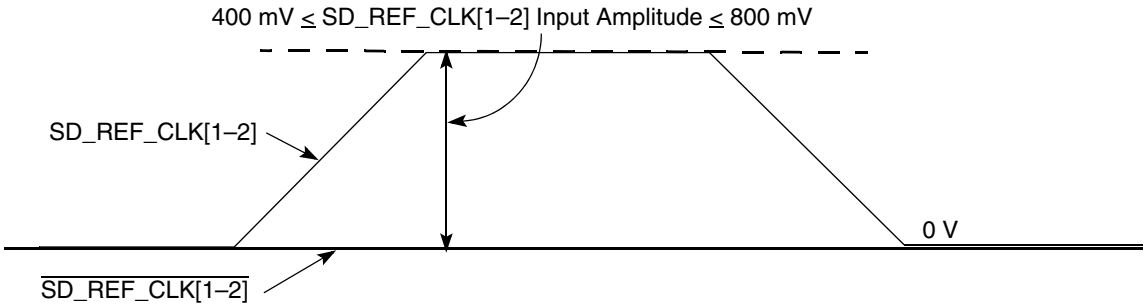

Figure 7. Single-Ended Reference Clock Input DC Requirements

3.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8157 supports a 2.5 Gbps and a 5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision*

3.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8157.

3.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

3.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 28 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.5 V.

Table 28. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{ILAC}	—	 MV_{REF} – 0.150 MV_{REF} – 0.175	V
AC input high voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{IHAC}	 MV_{REF} + 0.150 MV_{REF} + 0.175	—	V

Note: At recommended operating conditions with V_{DDDDR} of 1.5 ± 5%.

Table 29 provides the input AC timing specifications for the DDR SDRAM interface.

Table 29. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}				1, 2, 4
• 1333 MHz data rate		–125	125	ps	
• 1200 MHz data rate		–142	142	ps	
• 1066 MHz data rate		–170	170	ps	
• 800 MHz data rate		–200	200	ps	
• 667 MHz data rate		–240	240	ps	
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}				2, 3
• 1333 MHz data rate		–250	250	ps	
• 1200 MHz data rate		–275	275	ps	
• 1066 MHz data rate		–300	300	ps	
• 800 MHz data rate		–425	425	ps	
• 667 MHz data rate		–510	510	ps	

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.5 V) ± 5%
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
4. The t_{CISKEW} test coverage is derived from the t_{DISKEW} parameters.

transmitter specifications are defined in Table 35 and the receiver specifications are defined in Table 36. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Table 33. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Comments
Unit interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} =$ 0.25 UI. This does not include spread spectrum or REF_CLK jitter. It includes device random jitter at 10^{-12}. See notes 2 and 3.
Time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} =$ 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 15 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-NAX-JITTER}$ = 0.25 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 35. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Comments
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 15 and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER} = 0.25$ UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

Table 36. PCI Express 2.0 (5.0 Gbps) Differential Receiver (Rx) Input AC Specifications

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Conditions
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 400 ps ±300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max Rx inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common REF_CLK Rx architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max Rx inherent total timing error
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common REF_CLK Rx architecture

Note: No test load is necessarily accosted with this value.

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in Figure 15.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

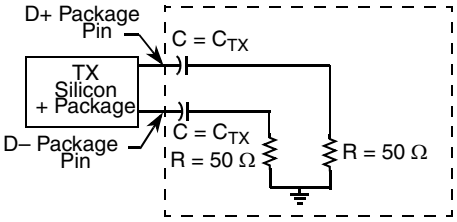

Figure 15. Test Measurement Load

3.6.2.4 Serial RapidIO AC Timing Specifications

Table 37 defines the transmitter AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 37. Serial RapidIO Transmitter AC Timing Specifications Up to 3.125 Gbaud

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit
Deterministic Jitter	J_D	—	—	0.17	UI p-p
Total Jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

Table 38 defines the Receiver AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 38. Serial RapidIO Receiver AC Timing Specifications Up to 3.125 Gbaud

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	—	—	0.37	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total Jitter Tolerance	J_T	—	—	0.65	UI p-p	1, 2
Bit Error Rate	BER	—	—	10^{-12}	—	—

7 Product Documentation

The following is a general list of supporting documentation:

- *MSC8157 Technical Data Sheet* (MSC8157). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8157 device.
- *MSC8157 Reference Manual* (MSC8157RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8157 device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.

8 Revision History

Table 56 provides a revision history for this data sheet.

Table 56. Document Revision History

Revision	Date	Description
3	12/2103	Updated Table 55, “Orderable Part Numbers.”
2	10/2013	Updated Table 55, “Orderable Part Numbers.”
1	12/2012	• In Table 52, “SPI AC Timing Specifications,” updated t_{NIKHOV} max value to 7 ns, t_{NEKHOV} max value to 13 ns, and t_{NIIVKH} min value to 13 ns. • In Table 55, “Orderable Part Numbers,” updated the list of supported parts.
0	11/2011	Initial release of this document.