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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | - |
| Interface | - |
| Clock Rate | - |
| Non-Volatile Memory | - |
| On-Chip RAM | - |
| Voltage - I/O | - |
| Voltage - Core | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8157tag1000a |

# 1 Block Diagram

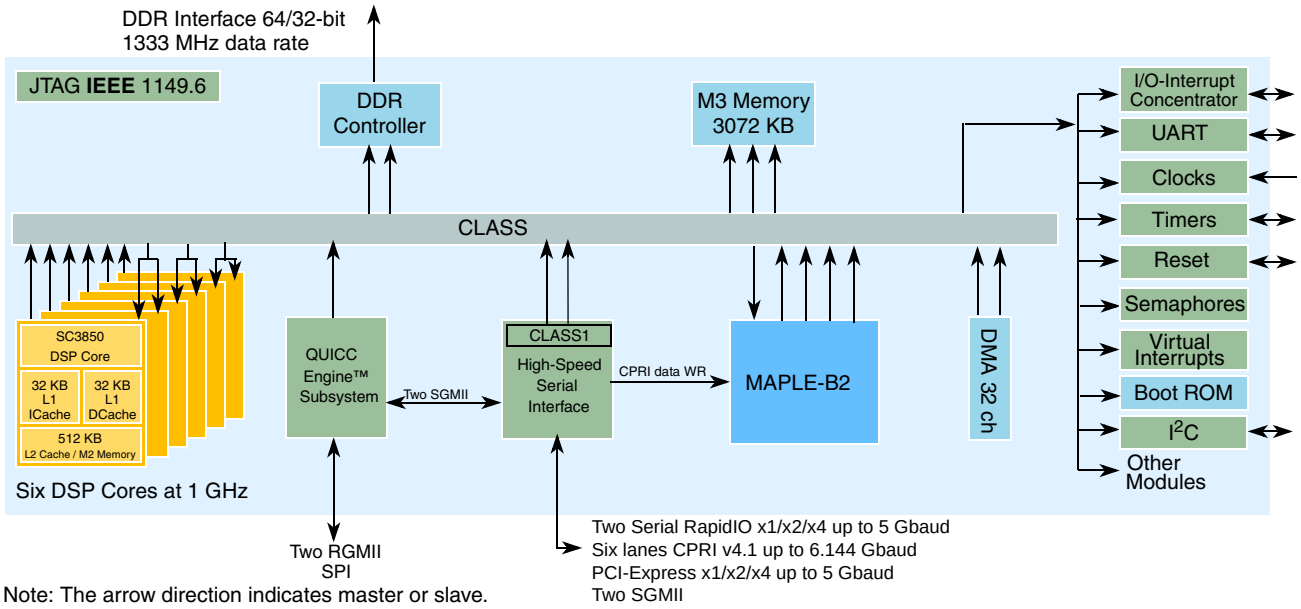



**Figure 1. MSC8157 Block Diagram**

**Table 1. Signal List by Ball Number (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| E13 | NC | Non-user | N/A |
| E14 | NC | Non-user | N/A |
| E15 | INT_OUT/CP_TX_INT | O | QVDD |
| E16 | HRESET | I/O | QVDD |
| E17 | TCK | I | QVDD |
| E18 | VSS | Ground | N/A |
| E19 | NVDD | Power | N/A |
| E20 | GE2_RD3/CP_LOS2 | I | NVDD |
| E21 | VSS | Ground | N/A |
| E22 | VSS | Non-user | N/A |
| E23 | NVDD | Power | N/A |
| E24 | GPIO27/TMR4/RCW_SRC0 | I/O | NVDD |
| E25 | VSS | Ground | N/A |
| E26 | GPIO0/IRQ0/RC0/CP_SYNC1 | I/O | NVDD |
| E27 | GPIO17/SPI_SCK/CP_LOS3 | I/O | NVDD |
| E28 | GPIO1/IRQ1/RC1/CP_SYNC2 | I/O | NVDD |
| F1 | MDQ40 | I/O | GVDD |
| F2 | MDQ41 | I/O | GVDD |
| F3 | MDQS5 | I/O | GVDD |
| F4 | MDQS5 | I/O | GVDD |
| F5 | MDQ43 | I/O | GVDD |
| F6 | MDQ47 | I/O | GVDD |
| F7 | MDM6 | O | GVDD |
| F8 | VDD | Power | N/A |
| F9 | VSS | Ground | N/A |
| F10 | VDD | Power | N/A |
| F11 | NC | Non-user | N/A |
| F12 | NC | Non-user | N/A |
| F13 | VSS | Ground | N/A |
| F14 | NC | Non-user | N/A |
| F15 | NMI_OUT/CP_RX_INT | O | QVDD |
| F16 | VSS | Ground | N/A |
| F17 | TDI | I | QVDD |
| F18 | VSS | Ground | N/A |

**Table 1. Signal List by Ball Number (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| M21 | NC | NC | N/A |
| M22 | NC | NC | N/A |
| M23 | SD_A_TX | O | SXPVDD |
| M24 | $\overline{\text{SD\_A\_TX}}$ | O | SXPVDD |
| M25 | SXPVDD | Power | N/A |
| M26 | SXPVSS | Ground | N/A |
| M27 | $\overline{\text{SD\_A\_RX}}$ | I | SXCVDD |
| M28 | SD_A_RX | I | SXCVDD |
| N1 | $\overline{\text{MRAS}}$ | O | GVDD |
| N2 | VSS | Ground | N/A |
| N3 | NC | Non-user | N/A |
| N4 | GVDD | Power | N/A |
| N5 | VSS | Ground | N/A |
| N6 | MODT1 | O | GVDD |
| N7 | CRPEVDD | Power | N/A |
| N8 | VSS | Ground | N/A |
| N9 | CRPEVDD | Power | N/A |
| N10 | VSS | Ground | N/A |
| N11 | CRPEVDD | Power | N/A |
| N12 | VSS | Ground | N/A |
| N13 | VDD | Power | N/A |
| N14 | VSS | Ground | N/A |
| N15 | VDD | Power | N/A |
| N16 | VSS | Ground | N/A |
| N17 | VDD | Power | N/A |
| N18 | VSS | Ground | N/A |
| N19 | VDD | Power | N/A |
| N20 | VSS | Ground | N/A |
| N21 | NC | NC | N/A |
| N22 | NC | NC | N/A |
| N23 | SXPVDD | Power | N/A |
| N24 | SXPVSS | Ground | N/A |
| N25 | SD_B_TX | O | SXPVDD |
| N26 | $\overline{\text{SD\_B\_TX}}$ | O | SXPVDD |

**Table 1. Signal List by Ball Number (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| N27 | SXCVSS | Ground | N/A |
| N28 | SXCVDD | Power | N/A |
| P1 | $\overline{\text{MCK2}}$ | O | GVDD |
| P2 | MA10 | O | GVDD |
| P3 | NC | Non-user | N/A |
| P4 | MA4 | O | GVDD |
| P5 | NC | Non-user | N/A |
| P6 | MODT0 | O | GVDD |
| P7 | VSS | Ground | N/A |
| P8 | CRPEVDD | Power | N/A |
| P9 | VSS | Ground | N/A |
| P10 | CRPEVDD | Power | N/A |
| P11 | VSS | Ground | N/A |
| P12 | VDD | Power | N/A |
| P13 | VSS | Ground | N/A |
| P14 | VDD | Power | N/A |
| P15 | VSS | Ground | N/A |
| P16 | VDD | Power | N/A |
| P17 | VSS | Ground | N/A |
| P18 | VDD | Power | N/A |
| P19 | VSS | Ground | N/A |
| P20 | VDD | Power | N/A |
| P21 | NC | NC | N/A |
| P22 | SD_IMP_CAL_RX | I | SXCVDD |
| P23 | NC | NC | N/A |
| P24 | NC | NC | N/A |
| P25 | SXPVDD | Power | N/A |
| P26 | SXPVSS | Ground | N/A |
| P27 | $\overline{\text{SD\_B\_RX}}$ | I | SXCVDD |
| P28 | SD_B_RX | I | SXCVDD |
| R1 | MCK2 | O | GVDD |
| R2 | GVDD | Power | N/A |
| R3 | MA0 | O | GVDD |
| R4 | VSS | Ground | N/A |

**Table 1. Signal List by Ball Number (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| AA7 | MCKE0 | O | GVDD |
| AA8 | VSS | Ground | N/A |
| AA9 | GVDD | Power | N/A |
| AA10 | VSS | Ground | N/A |
| AA11 | M3VDD | Power | N/A |
| AA12 | VSS | Ground | N/A |
| AA13 | M3VDD | Power | N/A |
| AA14 | VSS | Ground | N/A |
| AA15 | CPRIVDD | Power | N/A |
| AA16 | VSS | Ground | N/A |
| AA17 | CPRIVDD | Power | N/A |
| AA18 | VSS | Ground | N/A |
| AA19 | CPRIVDD | Power | N/A |
| AA20 | NC | NC | N/A |
| AA21 | SD_IMP_CAL_TX | I | SXPVDD |
| AA22 | NC | NC | N/A |
| AA23 | NC | NC | N/A |
| AA24 | NC | NC | N/A |
| AA25 | SD_E_TX | O | SXPVDD |
| AA26 | $\overline{\text{SD\_E\_TX}}$ | O | SXPVDD |
| AA27 | SXCVSS | Ground | N/A |
| AA28 | SXCVDD | Power | N/A |
| AB1 | $\overline{\text{MDQS8}}$ | I/O | GVDD |
| AB2 | MDM8 | O | GVDD |
| AB3 | MECC2 | I/O | GVDD |
| AB4 | MECC1 | I/O | GVDD |
| AB5 | NC | Non-user | N/A |
| AB6 | MAPAR_IN | I | GVDD |
| AB7 | MBA2 | O | GVDD |
| AB8 | MDQ2 | I/O | GVDD |
| AB9 | MDQ1 | I/O | GVDD |
| AB10 | MDQ0 | I/O | GVDD |
| AB11 | VSS | Ground | N/A |
| AB12 | M3VDD | Power | N/A |

**Table 1. Signal List by Ball Number (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| AC19 | NC | NC | N/A |
| AC20 | NC | Non-user | N/A |
| AC21 | NC | NC | N/A |
| AC22 | NC | NC | N/A |
| AC23 | NC | NC | N/A |
| AC24 | NC | NC | N/A |
| AC25 | SD_F_TX | O | SXPVDD |
| AC26 | $\overline{\text{SD\_F\_TX}}$ | O | SXPVDD |
| AC27 | SXCVSS | Ground | N/A |
| AC28 | SXCVDD | Power | N/A |
| AD1 | MECC7 | I/O | GVDD |
| AD2 | MECC6 | I/O | GVDD |
| AD3 | MECC0 | I/O | GVDD |
| AD4 | MECC5 | I/O | GVDD |
| AD5 | MECC3 | I/O | GVDD |
| AD6 | MDQ24 | I/O | GVDD |
| AD7 | MDM0 | O | GVDD |
| AD8 | $\overline{\text{MDQS0}}$ | I/O | GVDD |
| AD9 | MDQS0 | I/O | GVDD |
| AD10 | MDQ4 | I/O | GVDD |
| AD11 | MDQ6 | I/O | GVDD |
| AD12 | VSS | Non-user | N/A |
| AD13 | VSS | Non-user | N/A |
| AD14 | VSS | Non-user | N/A |
| AD15 | VSS | Ground | N/A |
| AD16 | VSS | Ground | N/A |
| AD17 | NC | NC | N/A |
| AD18 | SD_PLL2_AVDD | Power | N/A |
| AD19 | NC | NC | N/A |
| AD20 | NC | NC | N/A |
| AD21 | NC | NC | N/A |
| AD22 | NC | NC | N/A |
| AD23 | NC | NC | N/A |
| AD24 | NC | NC | N/A |

**Table 1. Signal List by Ball Number (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| AD25 | SXPVDD | Power | N/A |
| AD26 | SXPVSS | Ground | N/A |
| AD27 | $\overline{\text{SD\_F\_RX}}$ | I | SXCVDD |
| AD28 | SD_F_RX | I | SXCVDD |
| AE1 | MDQS2 | I/O | GVDD |
| AE2 | VSS | Ground | N/A |
| AE3 | MDQ18 | I/O | GVDD |
| AE4 | GVDD | Power | N/A |
| AE5 | VSS | Ground | N/A |
| AE6 | MDQ29 | I/O | GVDD |
| AE7 | GVDD | Power | N/A |
| AE8 | VSS | Ground | N/A |
| AE9 | MDQ5 | I/O | GVDD |
| AE10 | GVDD | Power | N/A |
| AE11 | VSS | Ground | N/A |
| AE12 | MDQ9 | I/O | GVDD |
| AE13 | VSS | Non-user | N/A |
| AE14 | VSS | Ground | N/A |
| AE15 | VSS | Ground | N/A |
| AE16 | VSS | Ground | N/A |
| AE17 | NC | NC | N/A |
| AE18 | SD_PLL2_AGND | Ground | N/A |
| AE19 | NC | NC | N/A |
| AE20 | SD_J_TX | O | SXPVDD |
| AE21 | SXPVDD | Power | N/A |
| AE22 | SD_I_TX | O | SXPVDD |
| AE23 | SXPVDD | Power | N/A |
| AE24 | NC | NC | N/A |
| AE25 | SD_G_TX | O | SXPVDD |
| AE26 | $\overline{\text{SD\_G\_TX}}$ | O | SXPVDD |
| AE27 | SXCVSS | Ground | N/A |
| AE28 | SXCVDD | Power | N/A |
| AF1 | $\overline{\text{MDQS2}}$ | I/O | GVDD |
| AF2 | MDQ17 | I/O | GVDD |

**Table 1. Signal List by Ball Number (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| AH15 | PLL1_AVDD | Power | N/A |
| AH16 | PLL2_AVDD | Power | N/A |
| AH17 | NC | NC | N/A |
| AH18 | SXCVDD | Power | N/A |
| AH19 | SD_REF_CLK2 | I | SXCVDD |
| AH20 | SXCVDD | Power | N/A |
| AH21 | SD_J_RX | I | SXCVDD |
| AH22 | SXCVDD | Power | N/A |
| AH23 | SD_I_RX | I | SXCVDD |
| AH24 | SXCVDD | Power | N/A |
| AH25 | SXPVDD | Power | N/A |
| AH26 | SXPVSS | Ground | N/A |
| AH27 | $\overline{\text{SD\_H\_RX}}$ | I | SXCVDD |
| AH28 | SD_H_RX | I | SXCVDD |

**Notes:**
1. Signal function during power-on reset is determined by the RCW source type. Selection of RapidIO, SGMII, CPRI, and PCI Express functionality during normal operation is configured by the RCW bit values. Selection of the GPIO function and other functions is done by GPIO register setup. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. For configuration details, see the *GPIO* chapter in the *MSC8157 Reference Manual*.
2. NC signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS or SXCVSS), or pulled up (VDD).
3. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected; non-user = connect as specified under Signal Name.
4. Connect power inputs to the power supplies via external filters. See the *MSC8157 Design Checklist* (AN4110) for details.

**Table 2. Signal List by Primary Signal Name**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| A18 | CLKIN | I | QVDD |
| A13 | CLKOUT | O | QVDD |
| AA15 | CPRIVDD | Power | N/A |
| AA17 | CPRIVDD | Power | N/A |
| AA19 | CPRIVDD | Power | N/A |
| AB16 | CPRIVDD | Power | N/A |
| AB18 | CPRIVDD | Power | N/A |
| AC15 | CPRIVDD | Power | N/A |
| W17 | CPRIVDD | Power | N/A |
| Y16 | CPRIVDD | Power | N/A |

**Table 2. Signal List by Primary Signal Name (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| U1 | MAVDD | Power | N/A |
| R6 | MBA0 | O | GVDD |
| U6 | MBA1 | O | GVDD |
| AB7 | MBA2 | O | GVDD |
| K1 | $\overline{\text{MCAS}}$ | O | GVDD |
| M1 | $\overline{\text{MCK0}}$ | O | GVDD |
| M2 | MCK0 | O | GVDD |
| T3 | $\overline{\text{MCK1}}$ | O | GVDD |
| U3 | MCK1 | O | GVDD |
| P1 | $\overline{\text{MCK2}}$ | O | GVDD |
| R1 | MCK2 | O | GVDD |
| AA7 | MCKE0 | O | GVDD |
| V6 | MCKE1 | O | GVDD |
| A16 | MCLKIN (optional) | I | QVDD |
| K2 | $\overline{\text{MCS0}}$ | O | GVDD |
| K3 | $\overline{\text{MCS1}}$ | O | GVDD |
| AD7 | MDM0 | O | GVDD |
| AH12 | MDM1 | O | GVDD |
| AH4 | MDM2 | O | GVDD |
| AH7 | MDM3 | O | GVDD |
| L6 | MDM4 | O | GVDD |
| G3 | MDM5 | O | GVDD |
| F7 | MDM6 | O | GVDD |
| C6 | MDM7 | O | GVDD |
| AB2 | MDM8 | O | GVDD |
| AB10 | MDQ0 | I/O | GVDD |
| AB9 | MDQ1 | I/O | GVDD |
| AF12 | MDQ10 | I/O | GVDD |
| AF10 | MDQ11 | I/O | GVDD |
| AG12 | MDQ12 | I/O | GVDD |
| AG9 | MDQ13 | I/O | GVDD |
| AF9 | MDQ14 | I/O | GVDD |
| AH11 | MDQ15 | I/O | GVDD |
| AF4 | MDQ16 | I/O | GVDD |

**Table 2. Signal List by Primary Signal Name (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| E19 | NVDD | Power | N/A |
| E23 | NVDD | Power | N/A |
| G25 | NVDD | Power | N/A |
| H20 | NVDD | Power | N/A |
| H23 | NVDD | Power | N/A |
| H27 | NVDD | Power | N/A |
| J21 | NVDD | Power | N/A |
| K25 | NVDD | Power | N/A |
| L21 | NVDD | Power | N/A |
| AH14 | PLL0_AVDD | Power | N/A |
| AH15 | PLL1_AVDD | Power | N/A |
| AH16 | PLL2_AVDD | Power | N/A |
| C17 | $\overline{\text{PORESET}}$ | I | QVDD |
| G15 | QVDD | Power | N/A |
| H14 | QVDD | Power | N/A |
| J27 | RC21 | I | NVDD |
| J24 | $\overline{\text{RCW\_LSEL0}}$/RC17 | I/O | NVDD |
| K24 | $\overline{\text{RCW\_LSEL1}}$/RC18 | I/O | NVDD |
| J26 | $\overline{\text{RCW\_LSEL2}}$/RC19 | I/O | NVDD |
| J25 | $\overline{\text{RCW\_LSEL3}}$/RC20 | I/O | NVDD |
| M27 | $\overline{\text{SD\_A\_RX}}$ | I | SXCVDD |
| M28 | SD_A_RX | I | SXCVDD |
| M23 | SD_A_TX | O | SXPVDD |
| M24 | $\overline{\text{SD\_A\_TX}}$ | O | SXPVDD |
| P27 | $\overline{\text{SD\_B\_RX}}$ | I | SXCVDD |
| P28 | SD_B_RX | I | SXCVDD |
| N25 | SD_B_TX | O | SXPVDD |
| N26 | $\overline{\text{SD\_B\_TX}}$ | O | SXPVDD |
| T27 | $\overline{\text{SD\_C\_RX}}$ | I | SXCVDD |
| T28 | SD_C_RX | I | SXCVDD |
| R25 | SD_C_TX | O | SXPVDD |
| R26 | $\overline{\text{SD\_C\_TX}}$ | O | SXPVDD |
| V27 | $\overline{\text{SD\_D\_RX}}$ | I | SXCVDD |
| V28 | SD_D_RX | I | SXCVDD |

**Table 2. Signal List by Primary Signal Name (continued)**

| Ball Number | Signal Name[1,2] | Pin Type[3] | Power Rail Name |
|---|---|---|---|
| AG14 | VSS | Ground | N/A |
| AG15 | VSS | Ground | N/A |
| AG16 | VSS | Ground | N/A |
| AG4 | VSS | Ground | N/A |
| AG7 | VSS | Ground | N/A |
| AH13 | VSS | Ground | N/A |
| B11 | VSS | Ground | N/A |
| B13 | VSS | Ground | N/A |
| B16 | VSS | Ground | N/A |
| B17 | VSS | Ground | N/A |
| B18 | VSS | Ground | N/A |
| B19 | VSS | Ground | N/A |
| B21 | VSS | Ground | N/A |
| B22 | VSS | Non-user | N/A |
| B23 | VSS | Ground | N/A |
| B25 | VSS | Ground | N/A |
| B27 | VSS | Ground | N/A |
| B9 | VSS | Ground | N/A |
| C1 | VSS | Ground | N/A |
| C18 | VSS | Ground | N/A |
| C4 | VSS | Ground | N/A |
| C7 | VSS | Ground | N/A |
| D11 | VSS | Ground | N/A |
| D13 | VSS | Ground | N/A |
| D16 | VSS | Ground | N/A |
| D18 | VSS | Ground | N/A |
| D19 | VSS | Non-user | N/A |
| D23 | VSS | Ground | N/A |
| D9 | VSS | Ground | N/A |
| E18 | VSS | Ground | N/A |
| E2 | VSS | Ground | N/A |
| E21 | VSS | Ground | N/A |
| E22 | VSS | Non-user | N/A |
| E25 | VSS | Ground | N/A |

transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 3.6.2, "HSSI AC Timing Specifications."

### 3.5.2.1 Signal Term Definitions

The SerDes interface uses differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 2 shows how the signals are defined in addition to the waveform for either a transmitter output (SD_[A–J]_TX and $\overline{\text{SD\_[A–J]\_TX}}$) or a receiver input (SD_[A–J]_RX and $\overline{\text{SD\_[A–J]\_RX}}$). Each signal swings between X volts and Y volts where X > Y.

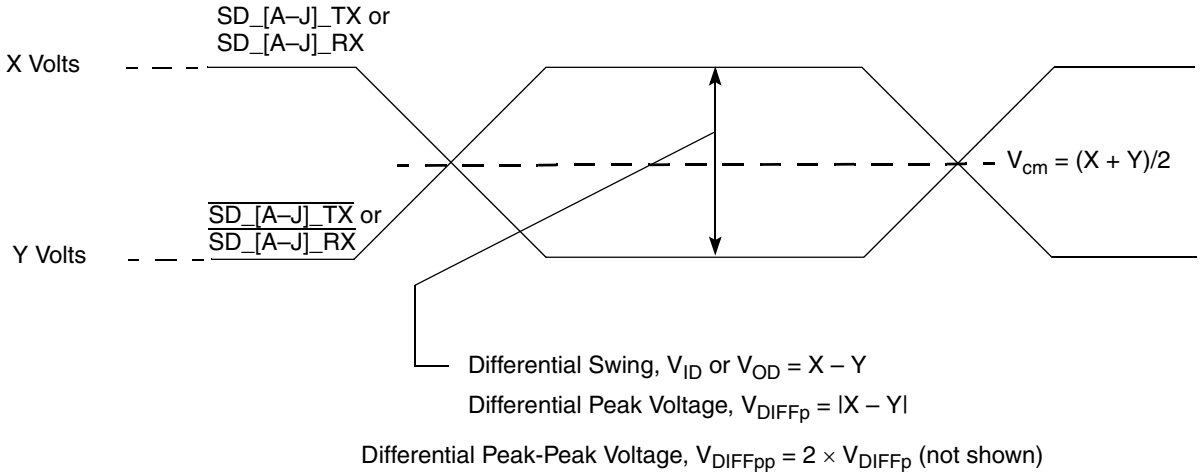



**Figure 2. Differential Voltage Definitions for Transmitter/Receiver**

Using this waveform, the definitions are listed in Table 10. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

**Table 10. Differential Signal Definitions**

| Term | Definition |
|---|---|
| Single-Ended Swing | The transmitter output signals and the receiver input signals SD[A–J]_TX, $\overline{\text{SD\_[A–J]\_TX}}$, SD_[A–J]_RX and $\overline{\text{SD\_[A–J]\_RX}}$ each have a peak-to-peak swing of X – Y volts. This is also referred to as each signal wire's single-ended swing. |
| Differential Output Voltage, VOD (or Differential Output Swing) | The differential output voltage (or swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SD\_[A–J]\_TX} – V_{\overline{SD[A–J]\_TX}}$. The $V_{OD}$ value can be either positive or negative. |
| Differential Input Voltage, VID (or Differential Input Swing) | The differential input voltage (or swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SD\_[A–J]\_RX} – V_{\overline{SD\_[A–J]\_RX}}$. The $V_{ID}$ value can be either positive or negative. |

*2.0*. The transmitter specifications for 2.5 Gbps are defined in Table 11 and the receiver specifications are defined in Table 12. For 5 Gbps, the transmitter specifications are defined in Table 13 and the receiver specifications are defined in Table 14.

### Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

At recommended operating conditions (see Table 4).

| Parameter | Symbol | Min | Nom | Max | Units | Condition |
|---|---|---|---|---|---|---|
| Differential peak-to-peak output voltage swing | $V_{TX\text{-}DIFFp\text{-}p}$ | 800 | 1000 | 1200 | mV | $V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$, Measured at the package pins with a test load of 50 Ω to GND on each pin. |
| De-emphasized differential output voltage (ratio) | $V_{TX\text{-}DE\text{-}RATIO}$ | 3.0 | 3.5 | 4.0 | dB | Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin. |
| DC differential Tx impedance | $Z_{TX\text{-}DIFF\text{-}DC}$ | 80 | 100 | 120 | Ω | Tx DC differential mode low Impedance |
| DC single-ended TX impedance | $Z_{TX\text{-}DC}$ | 40 | 50 | 60 | Ω | Required Tx D+ as well as D– DC Impedance during all states |

### Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

At recommended operating conditions (see Table 4).

| Parameter | Symbol | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Differential input peak-to-peak voltage | $V_{RX\text{-}DIFFp\text{-}p}$ | 120 | 1000 | 1200 | mV | 1 |
| DC differential Input Impedance | $Z_{RX\text{-}DIFF\text{-}DC}$ | 80 | 100 | 120 | Ω | 2 |
| DC input impedance | $Z_{RX\text{-}DC}$ | 40 | 50 | 60 | Ω | 3 |
| Powered down DC input impedance | $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$ | 50 | — | — | KΩ | 4 |
| Electrical idle detect threshold | $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$ | 65 | — | 175 | mV | 5 |

**Notes:**
1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$. Measured at the package pins of the receiver

### Table 13. PCI Express (5 Gbps) Differential Transmitter (Tx) Output DC Specifications

At recommended operating conditions (see Table 4).

| Parameter | Symbol | Min | Nom | Max | Units | Condition |
|---|---|---|---|---|---|---|
| Differential peak-to-peak output voltage swing | $V_{TX\text{-}DIFFp\text{-}p}$ | 800 | 1000 | 1200 | mV | $V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$, Measured at the package pins with a test load of 50 Ω to GND on each pin. |
| Low power differential peak-to-peak output voltage swing | $V_{TX\text{-}DIFFp\text{-}p\_low}$ | 400 | 500 | 1200 | mV | $V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$, Measured at the package pins with a test load of 50 Ω to GND on each pin. |
| De-emphasized differential output voltage (ratio) | $V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$ | 3.0 | 3.5 | 4.0 | dB | Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin. |
| De-emphasized differential output voltage (ratio) | $V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$ | 5.5 | 6.0 | 6.5 | dB | Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin. |
| DC differential Tx impedance | $Z_{TX\text{-}DIFF\text{-}DC}$ | 80 | 100 | 120 | Ω | Tx DC differential mode low impedance |
| Transmitter DC impedance | $Z_{TX\text{-}DC}$ | 40 | 50 | 60 | Ω | Required Tx D+ as well as D– DC impedance during all states |

### Table 14. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications

| Parameter | Symbol | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Differential input peak-to-peak voltage | $V_{RX\text{-}DIFFp\text{-}p}$ | 120 | 1000 | 1200 | mV | 1 |
| DC differential Input Impedance | $Z_{RX\text{-}DIFF\text{-}DC}$ | 80 | 100 | 120 | Ω | 2 |

**Table 14. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)**

| Parameter | Symbol | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| DC input impedance | $Z_{RX-DC}$ | 40 | 50 | 60 | Ω | 3 |
| Powered down DC input impedance | $Z_{RX-HIGH-IMP-DC}$ | 50 | — | — | KΩ | 4 |
| Electrical idle detect threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | — | 175 | mV | 5 |

**Notes:**
1. $V_{RX-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D–}|$. Measured at the package pins of the receiver

## 3.5.3.3 DC Level Requirements for Serial RapidIO Configurations

**Table 15. Serial RapidIO Transmitter DC Specifications for Transfer Rates ≤ 3.125 Gbaud**

At recommended operating conditions (see Table 4).

| Parameter | Symbol | Min | Nom | Max | Units | Condition |
|---|---|---|---|---|---|---|
| Output voltage | $V_O$ | –0.40 | — | 2.30 | V | — |
| Long run differential output voltage | $V_{DIFFPP}$ | 800 | — | 1600 | mVp-p | L[A–J]TECR0[AMP_RED] = 0b000000 |
| Short run differential output voltage | $V_{DIFFPP}$ | 500 | — | 1000 | mVp-p | L[A–J]TECR0[AMP_RED] = 0b001000 |
| DC differential TX impedance | ZTX-DIFF-DC | 80 | 100 | 120 | Ω | — |

**Note:** Voltage relative to COMMON of either signal comprising a differential pair.

**Table 16. Serial RapidIO Receiver DC Specifications for Transfer Rates ≤ 3.125 Gbaud**

At recommended operating conditions (see Table 4).

| Parameter | Symbol | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Differential input voltage | $V_{IN}$ | 200 | — | 1600 | mVp-p |
| DC differential RX impedance | ZRX-DIFF-DC | 80 | 100 | 120 | Ω |

**Notes:**
1. Voltage relative to COMMON of either signal comprising a differential pair.
2. Specifications are for Long and Short Run.

Figure 9 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

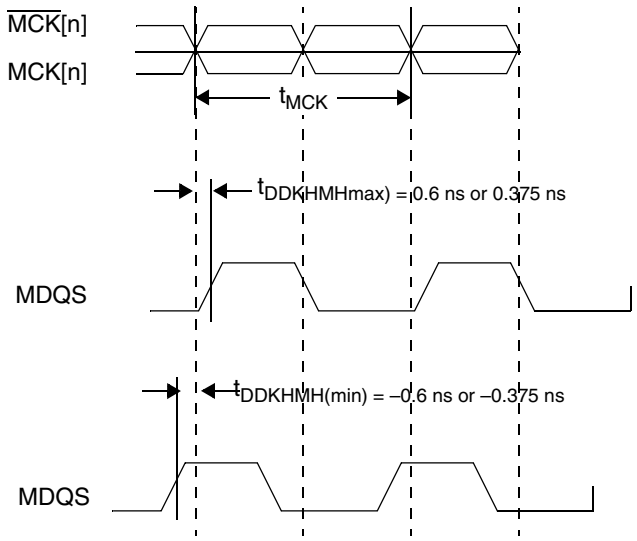



**Figure 9. MCK to MDQS Timing**

Figure 10 shows the DDR SDRAM output timing diagram.

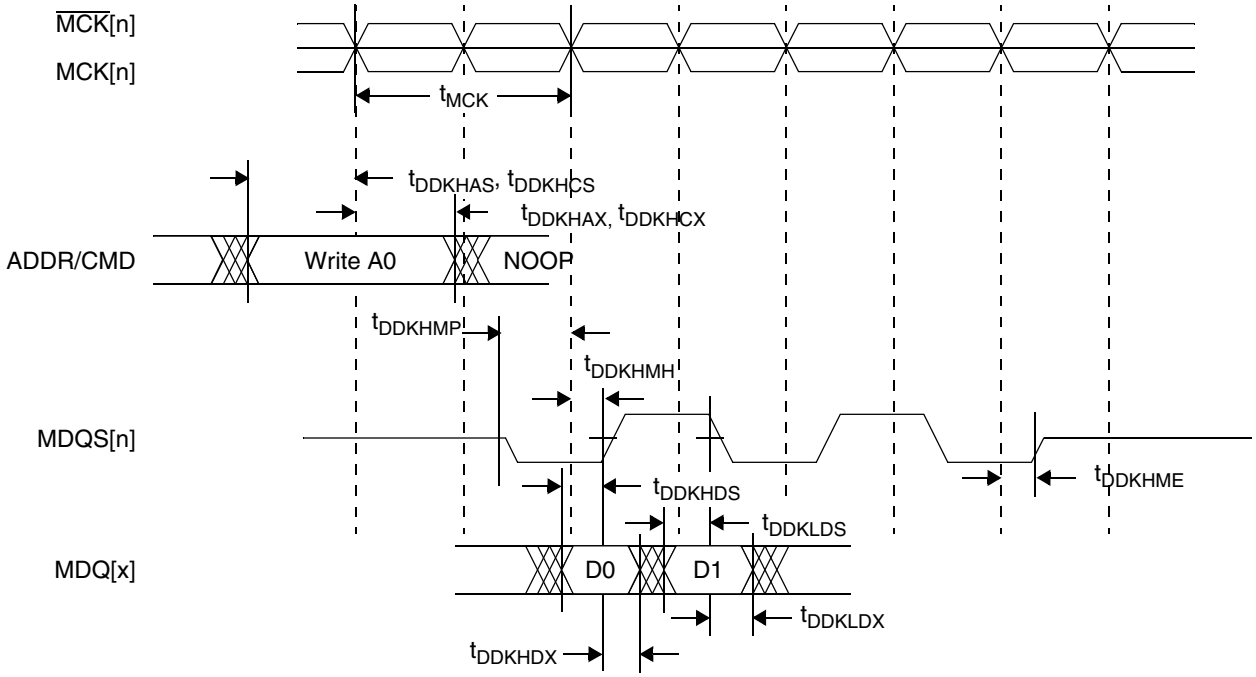



**Figure 10. DDR SDRAM Output Timing**

### 3.6.2.1 AC Requirements for SerDes Reference Clock

Table 32 lists AC requirements for the SerDes reference clocks.

**Table 32. SD_REF_CLK[1–2] and $\overline{\text{SD\_REF\_CLK[1–2]}}$ Input Clock Requirements**

At recommended operating conditions (see Table 4).

| Parameter | Symbol | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ frequency range | $t_{CLK\_REF}$ | — | 100/125<br>CPRI: 122.88 | — | MHz | 1 |
| SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ clock frequency tolerance<br>• Serial RapidIO, CPRI, SGMII<br>• PCI Express interface | $t_{CLK\_TOL}$ | <br>–100<br>–300 | <br>—<br>— | <br>100<br>300 | <br>ppm<br>ppm | — |
| SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ reference clock duty cycle | $t_{CLK\_DUTY}$ | 40 | 50 | 60 | % | 4 |
| SD_REF_CLK[1–2]/$\overline{\text{SD_REF_CLK[1–2]}}$max deterministic peak-peak jitter at $10^{-6}$ BER | $t_{CLK\_DJ}$ | — | — | 42 | ps | — |
| SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ total reference clock jitter at $10^{-6}$ BER (peak-to-peak jitter at ref_clk input) | $t_{CLK\_TJ}$ | — | — | 86 | ps | 2 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate | $t_{CLKRR}/t_{CLKFR}$ | 1 | — | 4 | V/ns | 3 |
| Differential input high voltage | $V_{IH}$ | 200 | — | — | mV | 4 |
| Differential input low voltage | $V_{IL}$ | — | — | –200 | mV | 4 |
| Rising edge rate (SD_REF_CLKn to falling edge rate) | Rise-Fall | — | — | 20 | % | 5, 6 |

**Notes:**
1. Only 100, 122.88, and 125 MHz have been tested. CPRI uses 122.88 MHz. The other interfaces use 100 or 125 MHz. Other values do not work correctly with the rest of the system.
2. Limits are from PCI Express CEM Rev 2.0.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLKn minus $\overline{\text{SD\_REF\_CLKn}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 13.
4. Measurement taken from differential waveform.
5. Measurement taken from single-ended waveform.
6. Matching applies to rising edge for SD_REF_CLKn and falling edge rate for $\overline{\text{SD\_REF\_CLKn}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLKn rising meets $\overline{\text{SD\_REF\_CLKn}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rising edge rate of SD_RF_CLKn should be compared to the falling edge rate of $\overline{\text{SD\_REF\_CLKn}}$; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 14.
7. REF_CLK jitter must be less than 0.05 UI when measured against a Golden PLL reference. The Golden PLL must have a maximum baud rate bandwidth greater than 1667, with a maximum 20 dB/dec rolloff down to a baud rate of 16.67 with no peaking around the corner frequency.

transmitter specifications are defined in Table 35 and the receiver specifications are defined in Table 36. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

**Table 33. PCI Express 2.0 (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications**

At recommended operating conditions (see Table 4).

| Parameter | Symbol | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| Unit interval | UI | 399.88 | 400.00 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1. |
| Tx eye width | $T_{TX-EYE}$ | 0.75 | — | — | UI | The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} =$ 0.25 UI. This does not include spread spectrum or REF_CLK jitter. It includes device random jitter at $10^{-12}$. See notes 2 and 3. |
| Time between the jitter median and maximum deviation from the median. | $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.125 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} =$ 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See notes 2 and 3. |
| AC coupling capacitor | $C_{TX}$ | 75 | — | 200 | nF | All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 15 and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE}$ = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-NAX-JITTER}$ = 0.25 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The DSP device SerDes transmitter does not have a built-in $C_{TX}$. An external AC coupling capacitor is required.

### 3.6.3 Timers and Timers_32b AC Timing Specifications

Table 49 lists the timer input AC timing specifications.

**Table 49. Timers Input AC Timing Specifications**

At recommended operating conditions (see Table 4).

| Characteristics | Symbol | Minimum | Unit | Notes |
|---|---|---|---|---|
| Timers inputs—minimum pulse width | $T_{TIWID}$ | 8 | ns | 1, 2 |

**Notes:**
1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least $t_{TIWID}$ ns to ensure proper operation.

Figure 21 shows the AC test load for the timers

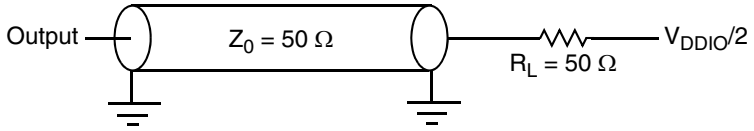



**Figure 21. Timer AC Test Load**

### 3.6.4 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are three general configuration registers used to configure the timing: GCR4, UCC1_DELAY_HR, and UCC3_DELAY_HR. These registers configure the programmable delay units (PDU) that should be programmed differently for each Interface to meet timing requirements. For additional information, see the *MSC8157 Reference Manual*.

#### 3.6.4.1 Management Interface Timing

**Table 50. Ethernet Controller Management Interface Timing**

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| GE_MDC frequency | $f_{MDC}$ | — | 2.5 | MHz |
| GE_MDC period | $t_{MDC}$ | 400 | — | ns |
| GE_MDC clock pulse width high | $t_{MDC\_H}$ | 160 | — | ns |
| GE_MDC clock pulse width low | $t_{MDC\_L}$ | 160 | — | ns |
| GE_MDC to GE_MDIO delay | $t_{MDKHDX}$ | 10 | 70 | ns |
| GE_MDIO to GE_MDC rising edge setup time | $t_{MDDVKH}$ | 20 | — | ns |
| GE_MDC rising edge to GE_MDIO hold time | $t_{MDDXKH}$ | 0 | — | ns |

## 3.6.5 SPI Timing

Table 52 lists the SPI input and output AC timing specifications.

**Table 52. SPI AC Timing Specifications**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SPI outputs valid—Master mode (internal clock) delay | $t_{NIKHOV}$ | — | 7 | ns | 2 |
| SPI outputs hold—Master mode (internal clock) delay | $t_{NIKHOX}$ | 0.5 | — | ns | 2 |
| SPI outputs valid—Slave mode (external clock) delay | $t_{NEKHOV}$ | — | 13 | ns | 2 |
| SPI outputs hold—Slave mode (external clock) delay | $t_{NEKHOX}$ | 2 | — | ns | 2 |
| SPI inputs—Master mode (internal clock) input setup time | $t_{NIIVKH}$ | 13 | — | ns | — |
| SPI inputs—Master mode (internal clock) input hold time | $t_{NIIXKH}$ | 0 | — | ns | — |
| SPI inputs—Slave mode (external clock) input setup time | $t_{NEIVKH}$ | 4 | — | ns | — |
| SPI inputs—Slave mode (external clock) input hold time | $t_{NEIXKH}$ | 2 | — | ns | — |

**Notes:** 1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{NIKHOX}$ symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.

Figure 24 provides the AC test load for the SPI.

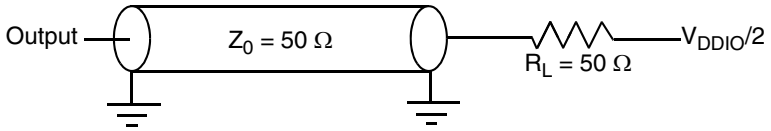
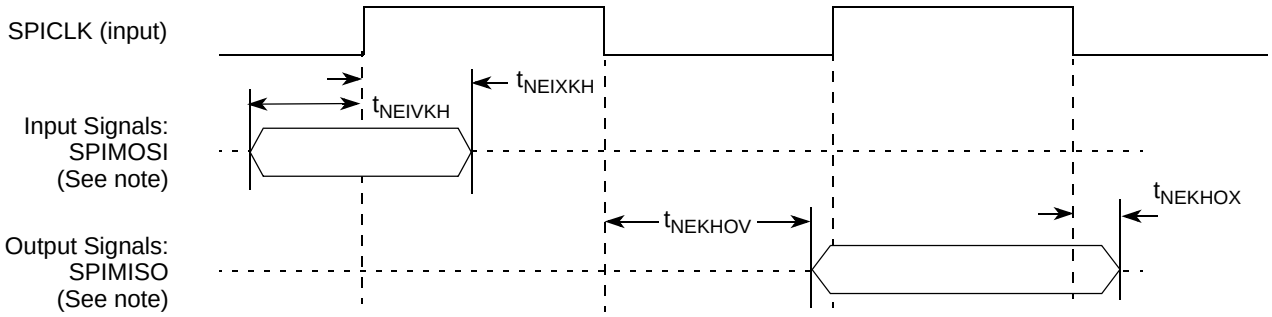



**Figure 24. SPI AC Test Load**

Figure 25 and Figure 26 represent the AC timings from Table 52. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 25 shows the SPI timings in slave mode (external clock).




**Note:** measured with SPMODE[CI] = 0, SPMODE[CP] = 0

**Figure 25. SPI AC Timing in Slave Mode (External Clock)**