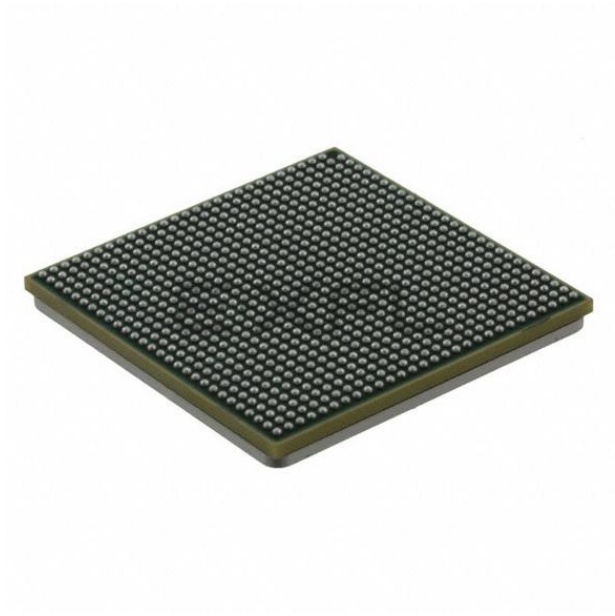

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	6.375MB
Voltage - I/O	1.0V, 1.5V, 2.5V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8157tvt1000a

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2 Pin Assignment

This section includes a MSC8157 package ball grid array layout and table listing the signal allocation by ball location.

2.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 2 with the ball location index numbers. Only the first multiplexed signal is shown. See Table 1 for a complete signal list by ball location.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A		VSS	MDQ57	GVDD	VSS	MDQ63	GVDD	NC	NC	NC	NC	NC	CLKOUT	EE0	VSS	MCLKIN (optional)	VSS	CLKIN	VSS	GPIO29	GPIO31	GE1_TX_CTL	GE1_GTX_CLK	GE1_TD0	GE1_TX_CLK	GE1_TD2	GE1_TD1	GE1_TD3	A
B	MDQ60	MDQ59	MDQ57	MDQS7	MDQ62	MDQ58	MDQ56	NC	VSS	NC	VSS	NC	VSS	TDO	TMS	VSS	VSS	VSS	VSS	GE2_TX_CLK	VSS	VSS	VSS	GPIO25	VSS	GE_MDC	VSS	GPIO18	B
C	VSS	GVDD	MDQ61	VSS	GVDD	MDM7	VSS	NC	NC	NC	NC	NC	NC	EE1	NC	DFT_TEST	PORESET	VSS	GPIO15	GE2_TD2	GE2_GTX_CLK	GE2_TX_CTL	GE2_TD1	GE2_TD0	GPIO30	GPIO20	GE_MDIO	GPIO21	C
D	MDQ49	MDQ48	MDQS6	MDQS6	MDQ50	MDQ51	MDQ52	NC	VSS	NC	VSS	NC	VSS	NC	NMI	VSS	HRESET_IN	VSS	VSS	GPIO13	NVDD	GE2_TD3	VSS	GPIO5	NVDD	GPIO16	VSS	GPIO10	D
E	MDQ53	VSS	MDQ55	GVDD	VSS	MDQ54	GVDD	VSS	NC	NC	NC	NC	NC	NC	INT_OUT	HRESET	TCK	VSS	NVDD	GE2_RD3	VSS	VSS	NVDD	GPIO27	VSS	GPIO0	GPIO17	GPIO1	E
F	MDQ40	MDQ41	MDQS5	MDQS5	MDQ43	MDQ47	MDM6	VDD	VSS	VDD	NC	NC	VSS	NC	NMI_OUT	VSS	TDI	VSS	GE2_RD2	GE2_RX_CTL	GE2_RD0	GE2_RX_CLK	GE2_RD1	GPIO26	GPIO6	GPIO22	GPIO23	GPIO8	F
G	VSS	GVDD	MDM5	VSS	GVDD	MDQ46	VDD	VSS	VDD	VSS	NC	NC	NC	NC	QVDD	STOP_BS	TRST	VSS	GPIO28	GE1_RD3	GE1_RD2	GE1_RX_CLK	VSS	GE1_RX_CTL	NVDD	GPIO19	VSS	GPIO11	G
H	MDQ38	MDQS4	MDQS4	MDQ44	MDQ45	MDQ42	VSS	VDD	VSS	VDD	VSS	VSS	NC	QVDD	VSS	VDD	VSS	VDD	VSS	NVDD	VSS	GE1_RD0	NVDD	GE1_RD1	VSS	GPIO14	NVDD	GPIO12	H
J	MDQ37	VSS	MDQ35	GVDD	MDQ33	MDQ36	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NVDD	GPIO24	GPIO9	RCW_LSEL0	RCW_LSEL3	RCW_LSEL2	RC21	GPIO3	J
K	MCAS	MCS0	MCS1	MDQ39	MDQ32	MDQ34	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	GPIO4	VSS	RCW_LSEL1	NVDD	GPIO7	VSS	GPIO2	K
L	VSS	GVDD	NC	VSS	GVDD	MDM4	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NVDD	NC	NC	VSS	VSS	VSS	SXCVSS	SXCVDD	L
M	MCK0	MCK0	MA13	MWE	NC	NC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	NC	NC	SD_A_TX	SD_A_TX	SXPVDD	SXPVSS	SD_A_RX	SD_A_RX	M
N	MRAS	VSS	NC	GVDD	VSS	MODT1	CRPEVDD	VSS	CRPEVDD	VSS	CRPEVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	SXPVDD	SXPVSS	SD_B_TX	SD_B_TX	SXCVSS	SXCVDD	N
P	MCK2	MA10	NC	MA4	NC	MODT0	VSS	CRPEVDD	VSS	CRPEVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	NC	SD_IMP_CAL_RX	NC	NC	SXPVDD	SXPVSS	SD_B_RX	SD_B_RX	P
R	MCK2	GVDD	MA0	VSS	GVDD	MBA0	GVDD	VSS	VDD	VSS	CRPEVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	NC	NC	SD_C_TX	SD_C_TX	SXCVSS	SXCVDD	R
T	VSS	VSS	MCK1	MA1	MA3	MAPAR_OUT	VSS	GVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	NC	NC	NC	NC	SXPVDD	SXPVSS	SD_C_RX	SD_C_RX	T
U	MAVDD	VSS	MCK1	GVDD	VSS	MBA1	GVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	NC	NC	NC	NC	SD_D_TX	SD_D_TX	SXCVSS	SXCVDD	U
V	MVREF	VSS	MA8	MA2	MA6	MCKE1	VSS	GVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	NC	NC	NC	NC	NC	NC	SD_D_RX	SD_D_RX	V
W	VSS	VSS	MA5	VSS	GVDD	MMDIC1	GVDD	VSS	VDD	VSS	M3VDD	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	VDD	VSS	NC	NC	NC	SD_PLL1_AVDD	SD_PLL1_AGND	NC	SXCVSS	SXCVDD	W
Y	MA11	MA9	MA12	MA7	NC	MMDIC0	VSS	GVDD	VSS	VDD	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	CPRIVDD	VSS	VDD	NC	NC	NC	NC	NC	NC	SD_REF_CLK1	SD_REF_CLK1	Y
AA	MDQS8	VSS	MA14	GVDD	VSS	MA15	MCKE0	VSS	GVDD	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	CPRIVDD	VSS	CPRIVDD	NC	SD_IMP_CAL_TX	NC	NC	NC	SD_E_TX	SD_E_TX	SXCVSS	SXCVDD	AA
AB	MDQS8	MDM8	MECC2	MECC1	NC	MAPAR_IN	MBA2	MDQ2	MDQ1	MDQ0	VSS	M3VDD	VSS	M3VDD	VSS	CPRIVDD	VSS	CPRIVDD	NC	NC	NC	NC	NC	NC	SXPVDD	SXPVSS	SD_E_RX	SD_E_RX	AB
AC	VSS	GVDD	MECC4	VSS	GVDD	MDQ25	VSS	GVDD	MDQ3	VSS	GVDD	VSS	M3VDD	VSS	CPRIVDD	VSS	NC	NC	NC	NC	NC	NC	NC	NC	SD_F_TX	SD_F_TX	SXCVSS	SXCVDD	AC
AD	MECC7	MECC6	MECC0	MECC5	MECC3	MDQ24	MDM0	MDQS0	MDQS0	MDQ4	MDQ6	VSS	VSS	VSS	VSS	VSS	NC	SD_PLL2_AVDD	NC	NC	NC	NC	NC	NC	SXPVDD	SXPVSS	SD_F_RX	SD_F_RX	AD
AE	MDQS2	VSS	MDQ18	GVDD	VSS	MDQ29	GVDD	VSS	MDQ5	GVDD	VSS	MDQ9	VSS	VSS	VSS	VSS	NC	SD_PLL2_AGND	NC	SD_J_TX	SXPVDD	SD_I_TX	SXPVDD	NC	SD_G_TX	SD_G_TX	SXCVSS	SXCVDD	AE
AF	MDQS2	MDQ17	MDQ21	MDQ16	MDQ30	MDQ27	MDQ28	MDQ7	MDQ14	MDQ11	MDQ8	MDQ10	VSS	VSS	VSS	VSS	NC	NC	NC	SD_J_TX	SXPVSS	SD_I_TX	SXPVSS	NC	SXPVDD	SXPVSS	SD_G_RX	SD_G_RX	AF
AG	VSS	GVDD	MDQ22	VSS	GVDD	MDQ26	VSS	GVDD	MDQ13	VSS	GVDD	MDQ12	VSS	VSS	VSS	VSS	NC	SXCVSS	SD_REF_CLK2	SXCVSS	SD_J_RX	SXCVSS	SD_I_RX	SXCVSS	SD_H_TX	SD_H_TX	SXCVSS	SXCVDD	AG
AH	MDQ20	MDQ19	MDQ23	MDM2	MDQS3	MDQS3	MDM3	MDQ31	MDQS1	MDQS1	MDQ15	MDM1	VSS	PLL0_AVDD	PLL1_AVDD	PLL2_AVDD	NC	SXCVDD	SD_REF_CLK2	SXCVDD	SD_J_RX	SXCVDD	SD_I_RX	SXCVDD	SXPVDD	SXPVSS	SD_H_RX	SD_H_RX	AH
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

Figure 2. MSC8157 FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
A23	GE1_GTX_CLK	O	NVDD
A24	GE1_TD0	O	NVDD
A25	GE1_TX_CLK	I	NVDD
A26	GE1_TD2	O	NVDD
A27	GE1_TD1	O	NVDD
A28	GE1_TD3	O	NVDD
B1	MDQ60	I/O	GVDD
B2	MDQ59	I/O	GVDD
B3	$\overline{\text{MDQS7}}$	I/O	GVDD
B4	MDQS7	I/O	GVDD
B5	MDQ62	I/O	GVDD
B6	MDQ58	I/O	GVDD
B7	MDQ56	I/O	GVDD
B8	NC	Non-user	N/A
B9	VSS	Ground	N/A
B10	NC	Non-user	N/A
B11	VSS	Ground	N/A
B12	NC	Non-user	N/A
B13	VSS	Ground	N/A
B14	TDO	O	QVDD
B15	TMS	I	QVDD
B16	VSS	Ground	N/A
B17	VSS	Ground	N/A
B18	VSS	Ground	N/A
B19	VSS	Ground	N/A
B20	GE2_TX_CLK	I	NVDD
B21	VSS	Ground	N/A
B22	VSS	Non-user	N/A
B23	VSS	Ground	N/A
B24	GPIO25/TMR2/RCW_SRC1	I/O	NVDD
B25	VSS	Ground	N/A
B26	GE_MDC	O	NVDD
B27	VSS	Ground	N/A
B28	GPIO18/SPI_MOSI/CP_LOS4	I/O	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
R5	GVDD	Power	N/A
R6	MBA0	O	GVDD
R7	GVDD	Power	N/A
R8	VSS	Ground	N/A
R9	VDD	Power	N/A
R10	VSS	Ground	N/A
R11	CRPEVDD	Power	N/A
R12	VSS	Ground	N/A
R13	VDD	Power	N/A
R14	VSS	Ground	N/A
R15	VDD	Power	N/A
R16	VSS	Ground	N/A
R17	VDD	Power	N/A
R18	VSS	Ground	N/A
R19	VDD	Power	N/A
R20	VSS	Ground	N/A
R21	NC	NC	N/A
R22	NC	NC	N/A
R23	NC	NC	N/A
R24	NC	NC	N/A
R25	SD_C_TX	O	SXPVDD
R26	$\overline{\text{SD\_C\_TX}}$	O	SXPVDD
R27	SXCVSS	Ground	N/A
R28	SXCVDD	Power	N/A
T1	VSS	Ground	N/A
T2	VSS	Ground	N/A
T3	$\overline{\text{MCK1}}$	O	GVDD
T4	MA1	O	GVDD
T5	MA3	O	GVDD
T6	MAPAR_OUT	O	GVDD
T7	VSS	Ground	N/A
T8	GVDD	Power	N/A
T9	VSS	Ground	N/A
T10	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AF3	MDQ21	I/O	GVDD
AF4	MDQ16	I/O	GVDD
AF5	MDQ30	I/O	GVDD
AF6	MDQ27	I/O	GVDD
AF7	MDQ28	I/O	GVDD
AF8	MDQ7	I/O	GVDD
AF9	MDQ14	I/O	GVDD
AF10	MDQ11	I/O	GVDD
AF11	MDQ8	I/O	GVDD
AF12	MDQ10	I/O	GVDD
AF13	VSS	Non-user	N/A
AF14	VSS	Ground	N/A
AF15	VSS	Ground	N/A
AF16	VSS	Ground	N/A
AF17	NC	NC	N/A
AF18	NC	NC	N/A
AF19	NC	NC	N/A
AF20	$\overline{\text{SD\_J\_TX}}$	O	SXPVDD
AF21	SXPVSS	Ground	N/A
AF22	$\overline{\text{SD\_I\_TX}}$	O	SXPVDD
AF23	SXPVSS	Ground	N/A
AF24	NC	NC	N/A
AF25	SXPVDD	Power	N/A
AF26	SXPVSS	Ground	N/A
AF27	$\overline{\text{SD\_G\_RX}}$	I	SXCVDD
AF28	SD_G_RX	I	SXCVDD
AG1	VSS	Ground	N/A
AG2	GVDD	Power	N/A
AG3	MDQ22	I/O	GVDD
AG4	VSS	Ground	N/A
AG5	GVDD	Power	N/A
AG6	MDQ26	I/O	GVDD
AG7	VSS	Ground	N/A
AG8	GVDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
D2	MDQ48	I/O	GVDD
D1	MDQ49	I/O	GVDD
AE9	MDQ5	I/O	GVDD
D5	MDQ50	I/O	GVDD
D6	MDQ51	I/O	GVDD
D7	MDQ52	I/O	GVDD
E1	MDQ53	I/O	GVDD
E6	MDQ54	I/O	GVDD
E3	MDQ55	I/O	GVDD
B7	MDQ56	I/O	GVDD
A3	MDQ57	I/O	GVDD
B6	MDQ58	I/O	GVDD
B2	MDQ59	I/O	GVDD
AD11	MDQ6	I/O	GVDD
B1	MDQ60	I/O	GVDD
C3	MDQ61	I/O	GVDD
B5	MDQ62	I/O	GVDD
A6	MDQ63	I/O	GVDD
AF8	MDQ7	I/O	GVDD
AF11	MDQ8	I/O	GVDD
AE12	MDQ9	I/O	GVDD
AD8	$\overline{\text{MDQS0}}$	I/O	GVDD
AD9	MDQS0	I/O	GVDD
AH10	MDQS1	I/O	GVDD
AH9	$\overline{\text{MDQS1}}$	I/O	GVDD
AE1	MDQS2	I/O	GVDD
AF1	$\overline{\text{MDQS2}}$	I/O	GVDD
AH5	$\overline{\text{MDQS3}}$	I/O	GVDD
AH6	MDQS3	I/O	GVDD
H2	$\overline{\text{MDQS4}}$	I/O	GVDD
H3	MDQS4	I/O	GVDD
F3	$\overline{\text{MDQS5}}$	I/O	GVDD
F4	MDQS5	I/O	GVDD
D3	$\overline{\text{MDQS6}}$	I/O	GVDD

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AG19	$\overline{\text{SD\_REF\_CLK2}}$	I	SXCVDD
AH19	SD_REF_CLK2	I	SXCVDD
G16	STOP_BS	I	QVDD
AA28	SXCVDD	Power	N/A
AC28	SXCVDD	Power	N/A
AE28	SXCVDD	Power	N/A
AG28	SXCVDD	Power	N/A
AH18	SXCVDD	Power	N/A
AH20	SXCVDD	Power	N/A
AH22	SXCVDD	Power	N/A
AH24	SXCVDD	Power	N/A
L28	SXCVDD	Power	N/A
N28	SXCVDD	Power	N/A
R28	SXCVDD	Power	N/A
U28	SXCVDD	Power	N/A
W28	SXCVDD	Power	N/A
AA27	SXCVSS	Ground	N/A
AC27	SXCVSS	Ground	N/A
AE27	SXCVSS	Ground	N/A
AG18	SXCVSS	Ground	N/A
AG20	SXCVSS	Ground	N/A
AG22	SXCVSS	Ground	N/A
AG24	SXCVSS	Ground	N/A
AG27	SXCVSS	Ground	N/A
L27	SXCVSS	Ground	N/A
N27	SXCVSS	Ground	N/A
R27	SXCVSS	Ground	N/A
U27	SXCVSS	Ground	N/A
W27	SXCVSS	Ground	N/A
AB25	SXPVDD	Power	N/A
AD25	SXPVDD	Power	N/A
AE21	SXPVDD	Power	N/A
AE23	SXPVDD	Power	N/A
AF25	SXPVDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
J9	VDD	Power	N/A
K10	VDD	Power	N/A
K12	VDD	Power	N/A
K14	VDD	Power	N/A
K16	VDD	Power	N/A
K18	VDD	Power	N/A
K20	VDD	Power	N/A
K8	VDD	Power	N/A
L11	VDD	Power	N/A
L13	VDD	Power	N/A
L15	VDD	Power	N/A
L17	VDD	Power	N/A
L19	VDD	Power	N/A
L7	VDD	Power	N/A
L9	VDD	Power	N/A
M10	VDD	Power	N/A
M12	VDD	Power	N/A
M14	VDD	Power	N/A
M16	VDD	Power	N/A
M18	VDD	Power	N/A
M20	VDD	Power	N/A
M8	VDD	Power	N/A
N13	VDD	Power	N/A
N15	VDD	Power	N/A
N17	VDD	Power	N/A
N19	VDD	Power	N/A
P12	VDD	Power	N/A
P14	VDD	Power	N/A
P16	VDD	Power	N/A
P18	VDD	Power	N/A
P20	VDD	Power	N/A
R13	VDD	Power	N/A
R15	VDD	Power	N/A
R17	VDD	Power	N/A

Table 2. Signal List by Primary Signal Name (continued)

Ball Number	Signal Name[1,2]	Pin Type[3]	Power Rail Name
AG14	VSS	Ground	N/A
AG15	VSS	Ground	N/A
AG16	VSS	Ground	N/A
AG4	VSS	Ground	N/A
AG7	VSS	Ground	N/A
AH13	VSS	Ground	N/A
B11	VSS	Ground	N/A
B13	VSS	Ground	N/A
B16	VSS	Ground	N/A
B17	VSS	Ground	N/A
B18	VSS	Ground	N/A
B19	VSS	Ground	N/A
B21	VSS	Ground	N/A
B22	VSS	Non-user	N/A
B23	VSS	Ground	N/A
B25	VSS	Ground	N/A
B27	VSS	Ground	N/A
B9	VSS	Ground	N/A
C1	VSS	Ground	N/A
C18	VSS	Ground	N/A
C4	VSS	Ground	N/A
C7	VSS	Ground	N/A
D11	VSS	Ground	N/A
D13	VSS	Ground	N/A
D16	VSS	Ground	N/A
D18	VSS	Ground	N/A
D19	VSS	Non-user	N/A
D23	VSS	Ground	N/A
D9	VSS	Ground	N/A
E18	VSS	Ground	N/A
E2	VSS	Ground	N/A
E21	VSS	Ground	N/A
E22	VSS	Non-user	N/A
E25	VSS	Ground	N/A

transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 3.6.2, "HSSI AC Timing Specifications."

3.5.2.1 Signal Term Definitions

The SerDes interface uses differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 2 shows how the signals are defined in addition to the waveform for either a transmitter output (SD_[A–J]_TX and $\overline{\text{SD\_[A–J]\_TX}}$) or a receiver input (SD_[A–J]_RX and $\overline{\text{SD\_[A–J]\_RX}}$). Each signal swings between X volts and Y volts where X > Y.

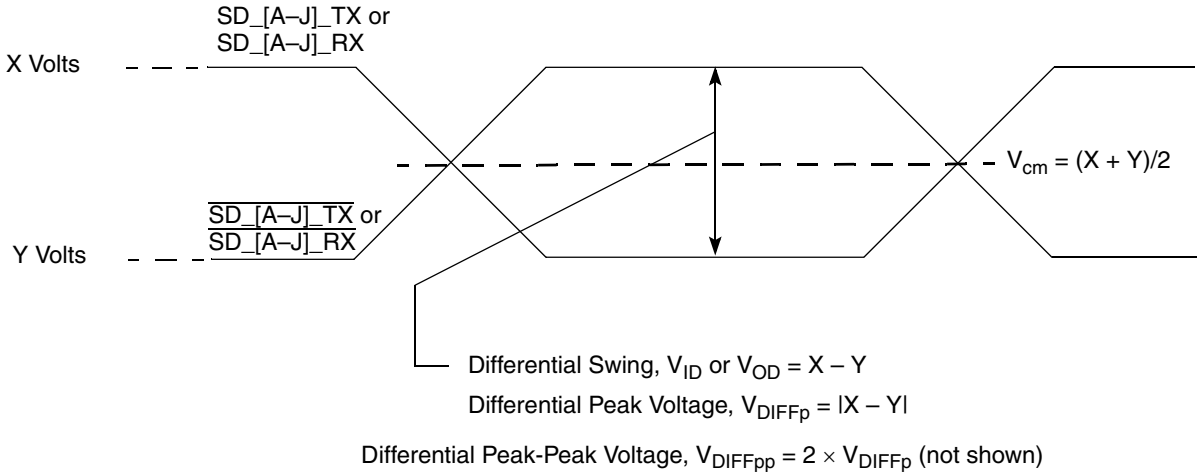


Figure 2. Differential Voltage Definitions for Transmitter/Receiver

Using this waveform, the definitions are listed in Table 10. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

Table 10. Differential Signal Definitions

Term	Definition
Single-Ended Swing	The transmitter output signals and the receiver input signals SD[A–J]_TX, $\overline{\text{SD\_[A–J]\_TX}}$, SD_[A–J]_RX and $\overline{\text{SD\_[A–J]\_RX}}$ each have a peak-to-peak swing of X – Y volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, VOD (or Differential Output Swing)	The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_[A–J]\_TX} – V_{\overline{SD[A–J]\_TX}}$. The V_{OD} value can be either positive or negative.
Differential Input Voltage, VID (or Differential Input Swing)	The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_[A–J]\_RX} – V_{\overline{SD\_[A–J]\_RX}}$. The V_{ID} value can be either positive or negative.

Table 14. PCI Express (5 Gbps) Differential Receiver (Rx) Input DC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Units	Notes
DC input impedance	Z_{RX-DC}	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	5

Notes:
1. $V_{RX-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D–}|$. Measured at the package pins of the receiver

3.5.3.3 DC Level Requirements for Serial RapidIO Configurations

Table 15. Serial RapidIO Transmitter DC Specifications for Transfer Rates ≤ 3.125 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output voltage	V_O	–0.40	—	2.30	V	—
Long run differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	L[A–J]TECR0[AMP_RED] = 0b000000
Short run differential output voltage	V_{DIFFPP}	500	—	1000	mVp-p	L[A–J]TECR0[AMP_RED] = 0b001000
DC differential TX impedance	ZTX-DIFF-DC	80	100	120	Ω	—

Note: Voltage relative to COMMON of either signal comprising a differential pair.

Table 16. Serial RapidIO Receiver DC Specifications for Transfer Rates ≤ 3.125 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units
Differential input voltage	V_{IN}	200	—	1600	mVp-p
DC differential RX impedance	ZRX-DIFF-DC	80	100	120	Ω

Notes:
1. Voltage relative to COMMON of either signal comprising a differential pair.
2. Specifications are for Long and Short Run.

Table 17. Serial RapidIO Transmitter DC Specifications for Short Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Condition
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	400	—	750	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b001101
Differential resistance	T_Rd	80	100	120	Ω	—

Table 18. Serial RapidIO Receiver DC Specifications for Short Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units
Input differential voltage	R_Vdiff	125	—	1200	mV
Differential resistance	R_Rdin	80	—	120	Ω

Table 19. Serial RapidIO Transmitter DC Specifications for Long Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Conditions
Output differential voltage (into floating load Rload = 100 Ω)	T_Vdiff	800	—	1200	mV	Amplitude setting L[A–J]TECR0[AMP_RED] = 0b000000 (with de-emphasis disabled)
De-emphasized differential output voltage	$T\_V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3	3.5	4	dB	• p(n)_(y)_tx_eq_type[1:0] = 01 • p(n)_(y)_tx_ratio_post1q[3:0] = 1110
Tx De-emphasized level	$T\_V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6	6.5	dB	• p(n)_(y)_tx_eq_type[1:0] = 01 • p(n)_(y)_tx_ratio_post1q[3:0] = 1100
Differential resistance	T_Rd	80	100	120	Ω	—

Table 20. Serial RapidIO Receiver DC Specifications for Long Run at 5 Gbaud

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Condition
Input differential voltage	R_Vdiff	N/A	—	1200	mV	It is assumed that for the R_Vdiff min specification, that the eye can be closed at the receiver after passing the signal through a CEI/SRIO Level II LR compliant channel.
Differential resistance	R_Rdin	80	—	120	Ω	—

Figure 9 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

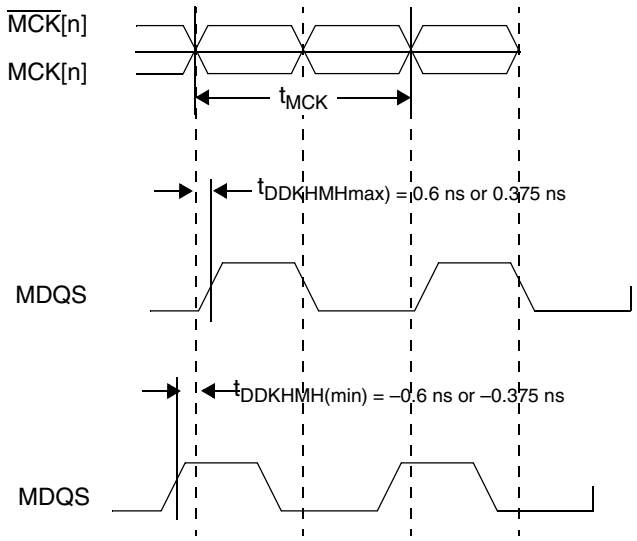


Figure 9. MCK to MDQS Timing

Figure 10 shows the DDR SDRAM output timing diagram.

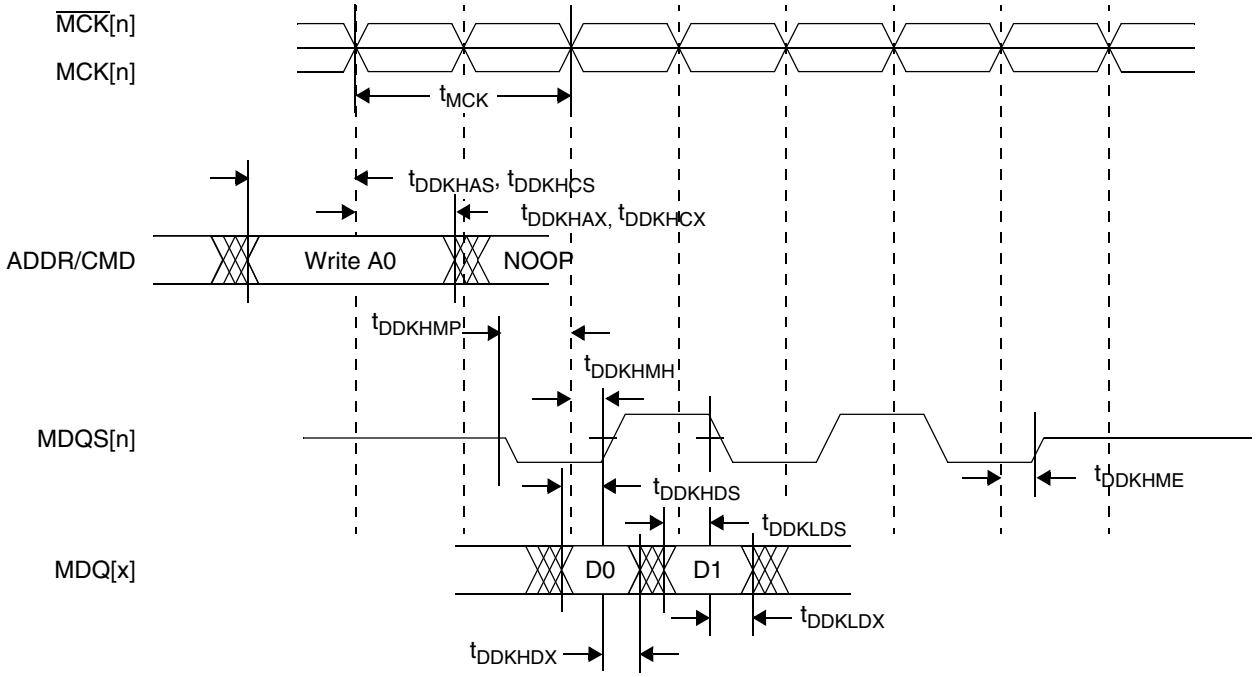


Figure 10. DDR SDRAM Output Timing

3.6.2.1 AC Requirements for SerDes Reference Clock

Table 32 lists AC requirements for the SerDes reference clocks.

Table 32. SD_REF_CLK[1–2] and $\overline{\text{SD\_REF\_CLK[1–2]}}$ Input Clock Requirements

At recommended operating conditions (see Table 4).

Parameter	Symbol	Min	Nom	Max	Units	Notes
SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ frequency range	t_{CLK_REF}	—	100/125 CPRI: 122.88	—	MHz	1
SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ clock frequency tolerance • Serial RapidIO, CPRI, SGMII • PCI Express interface	t_{CLK_TOL}	 –100 –300	 — —	 100 300	 ppm ppm	—
SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK[1–2]/$\overline{\text{SD_REF_CLK[1–2]}}$max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK[1–2]/$\overline{\text{SD\_REF\_CLK[1–2]}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at ref_clk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLKn to falling edge rate)	Rise-Fall	—	—	20	%	5, 6

Notes:
1. Only 100, 122.88, and 125 MHz have been tested. CPRI uses 122.88 MHz. The other interfaces use 100 or 125 MHz. Other values do not work correctly with the rest of the system.
2. Limits are from PCI Express CEM Rev 2.0.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLKn minus $\overline{\text{SD\_REF\_CLKn}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 13.
4. Measurement taken from differential waveform.
5. Measurement taken from single-ended waveform.
6. Matching applies to rising edge for SD_REF_CLKn and falling edge rate for $\overline{\text{SD\_REF\_CLKn}}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLKn rising meets $\overline{\text{SD\_REF\_CLKn}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rising edge rate of SD_RF_CLKn should be compared to the falling edge rate of $\overline{\text{SD\_REF\_CLKn}}$; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 14.
7. REF_CLK jitter must be less than 0.05 UI when measured against a Golden PLL reference. The Golden PLL must have a maximum baud rate bandwidth greater than 1667, with a maximum 20 dB/dec rolloff down to a baud rate of 16.67 with no peaking around the corner frequency.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

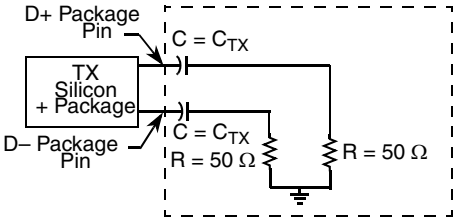


Figure 15. Test Measurement Load

3.6.2.4 Serial RapidIO AC Timing Specifications

Table 37 defines the transmitter AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 37. Serial RapidIO Transmitter AC Timing Specifications Up to 3.125 Gbaud

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit
Deterministic Jitter	J_D	—	—	0.17	UI p-p
Total Jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

Table 38 defines the Receiver AC specifications for the Serial RapidIO interface at frequencies up to 3.125 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 38. Serial RapidIO Receiver AC Timing Specifications Up to 3.125 Gbaud

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	—	—	0.37	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total Jitter Tolerance	J_T	—	—	0.65	UI p-p	1, 2
Bit Error Rate	BER	—	—	10^{-12}	—	—

Table 38. Serial RapidIO Receiver AC Timing Specifications Up to 3.125 Gbaud (continued)

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes: 1. Measured at receiver.
2. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 16. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 39 defines the short run transmitter AC specifications for the Serial RapidIO interface at 5 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 39. Serial RapidIO Short Run Transmitter AC Timing Specifications at 5.0 Gbaud

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit
Uncorrelated High Probability Jitter	T_UHPJ	—	—	0.15	UI p-p
Total Jitter	T_TJ	—	—	0.30	UI p-p
Baud Rate	UI	5.000 – 100ppm	5.000	5.000 + 100ppm	Gbaud

Table 40 defines the short run Receiver AC specifications for the Serial RapidIO interface at 5 Gbaud. The AC timing specifications do not include REF_CLK jitter.

Table 40. Serial RapidIO Short Run Receiver AC Timing Specifications at 5 Gbaud

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit
Rx Baud Rate	R_Baud	5.000 – 100ppm	5.000	5.000 + 100ppm	Gbaud
Uncorrelated Bounded High Probability Jitter	R_UBHPJ	—	—	0.15	UIp-p
Correlated Bounded High Probability Jitter	R_CBHPJ	—	—	0.3	UIp-p
Bounded High Probability Jitter	R_BHPJ	—	—	0.45	UIp-p
Sinusoidal Jitter maximum	R_SJ-max	—	—	5	UIp-p
Sinusoidal Jitter, High Frequency	R_SJ-hf	—	—	0.05	UIp-p
Total jitter (without sinusoidal jitter)	R_Tj	—	—	0.6	UIp-p

Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region in Figure 17. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PCB trace.

Table 41 defines the Transmitter AC specifications for long run Serial RapidIO interfaces using a transfer rate of 5 Gbps. The AC timing specifications do not include REF_CLK jitter.

Table 41. Serial RapidIO Transmitter Long Run AC Timing for Transfer Rate of 5 Gbps

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit	Conditions
Tx Baud Rate	T_Baud	5.000 – 100 ppm	5.000	5.000 + 100 ppm	Gbps	± 100 ppm
Uncorrelated high probability jitter	T_UHPJ	—	—	0.15	UI p-p	With de-emphasis disabled.
Total Jitter	T_TJ	—	—	0.30	UI p-p	With de-emphasis disabled.

Table 42 defines the Receiver AC specifications for long run Serial RapidIO interfaces using a transfer rate of 5 Gbps. The AC timing specifications do not include REF_CLK jitter.

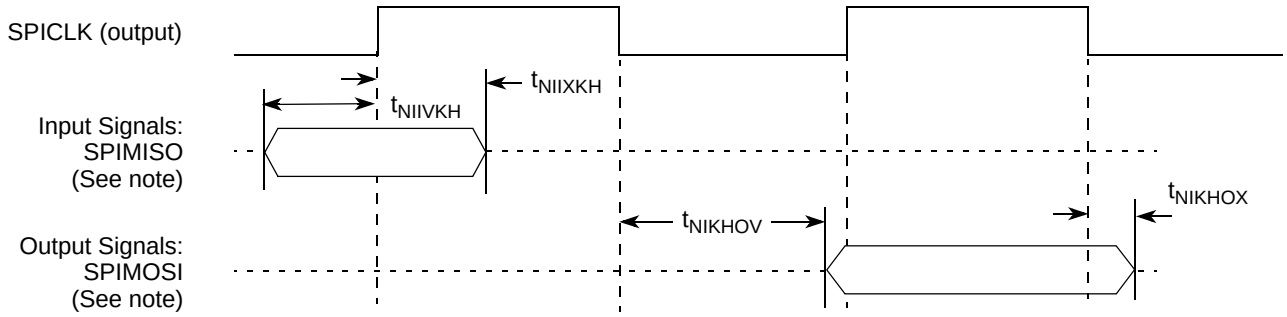
Table 42. Serial RapidIO Receiver Long Run AC Timing for Transfer Rate of 5 Gbps

At recommended operating conditions (see Table 4).

Characteristic	Symbol	Min	Nom	Max	Unit	Condition
Rx Baud Rate	R_Baud	5.000 – 100 ppm	5.000	5.000 + 100 ppm	Gbps	—
Gaussian	R_GJ	—	—	0.275	UI p-p	Informative jitter budget @Rx input
Uncorrelated bounded high probability jitter (D_J)	R_UBHPJ	—	—	0.15	UI p-p	Informative jitter budget @Rx input
Correlated bounded high probability jitter (ISI)	R_CBHPJ	—	—	0.525	UI p-p	Informative jitter budget @Rx input
Bounded high probability jitter (D_J + ISI)	R_BHPJ	—	—	0.675	UI p-p	Informative jitter budget @Rx input
Sinusoidal jitter, maximum	R_SJ-max	—	—	5	UI p-p	Informative jitter budget @Rx input
Sinusoidal jitter, high frequency	R_SJ-hf	—	—	0.05	UI p-p	Informative jitter budget @Rx input
Total Jitter (does not include sinusoidal jitter).	R_TJ	—	—	0.95	UI p-p	Informative jitter budget @Rx input

Note: The AC specifications do not include REF_CLK jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 17. The ISI jitter (R_CBHPJ) and amplitude have to be correlated, for example, by a PC trace.

Figure 26 shows the SPI timings in master mode (internal clock).



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 26. SPI AC Timing in Master Mode (Internal Clock)

3.6.6 Asynchronous Signal Timing

Table 53 lists the asynchronous signal timing specifications.

Table 53. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN/MCLKIN cycle
Output	t_{OUT}	Asynchronous	Application dependent

Note: Input value relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

NOTE

When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8157 device, that is, when the expected input value is read from the GPIO data register.

- *EE port*. Signals EE0, EE1.
- *Boot function*. Signal STOP_BS.
- *I^2C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- *Interrupt outputs*. Signals $\overline{\text{INT\_OUT}}$/CP_TX_INT and $\overline{\text{NMI\_OUT}}$/CP_RX_INT (minimum pulse width is 32 ns).

3.6.7 JTAG Signals

Table 54. JTAG Timing

Characteristics	Symbol	All Frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at $V_M = V_{DDIO}/2$	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	5.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{TRST}$ assert time	t_{TRST}	100.0	—	ns

Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.

Figure 27 shows the test clock input timing diagram.

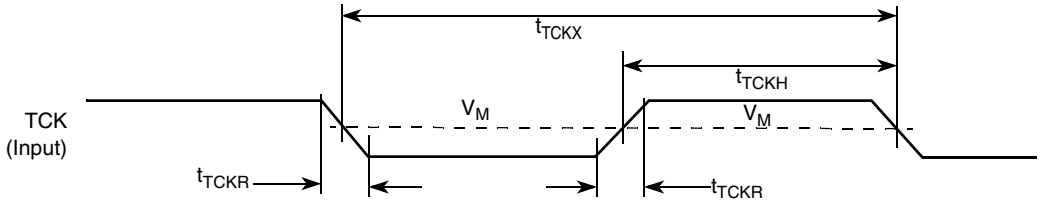


Figure 27. Test Clock Input Timing

Figure 28 shows the boundary scan (JTAG) timing diagram.

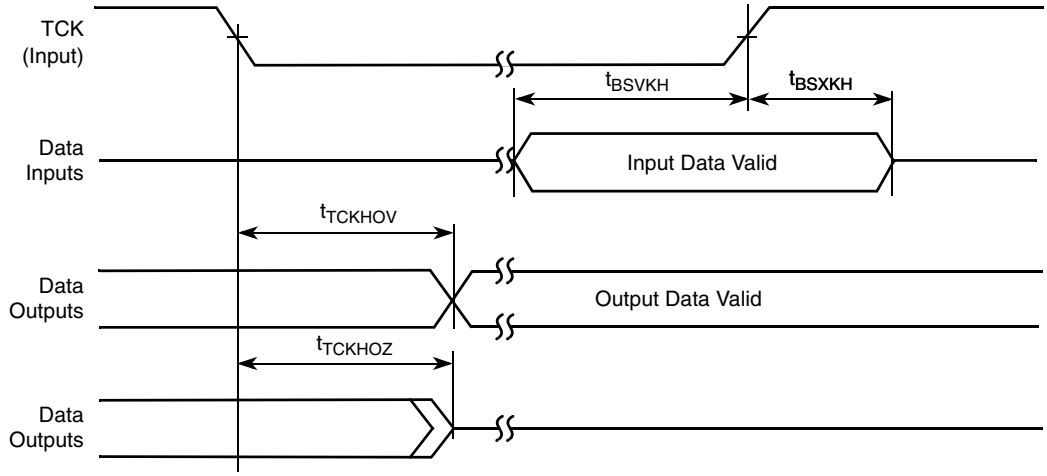


Figure 28. Boundary Scan (JTAG) Timing

6 Package Information

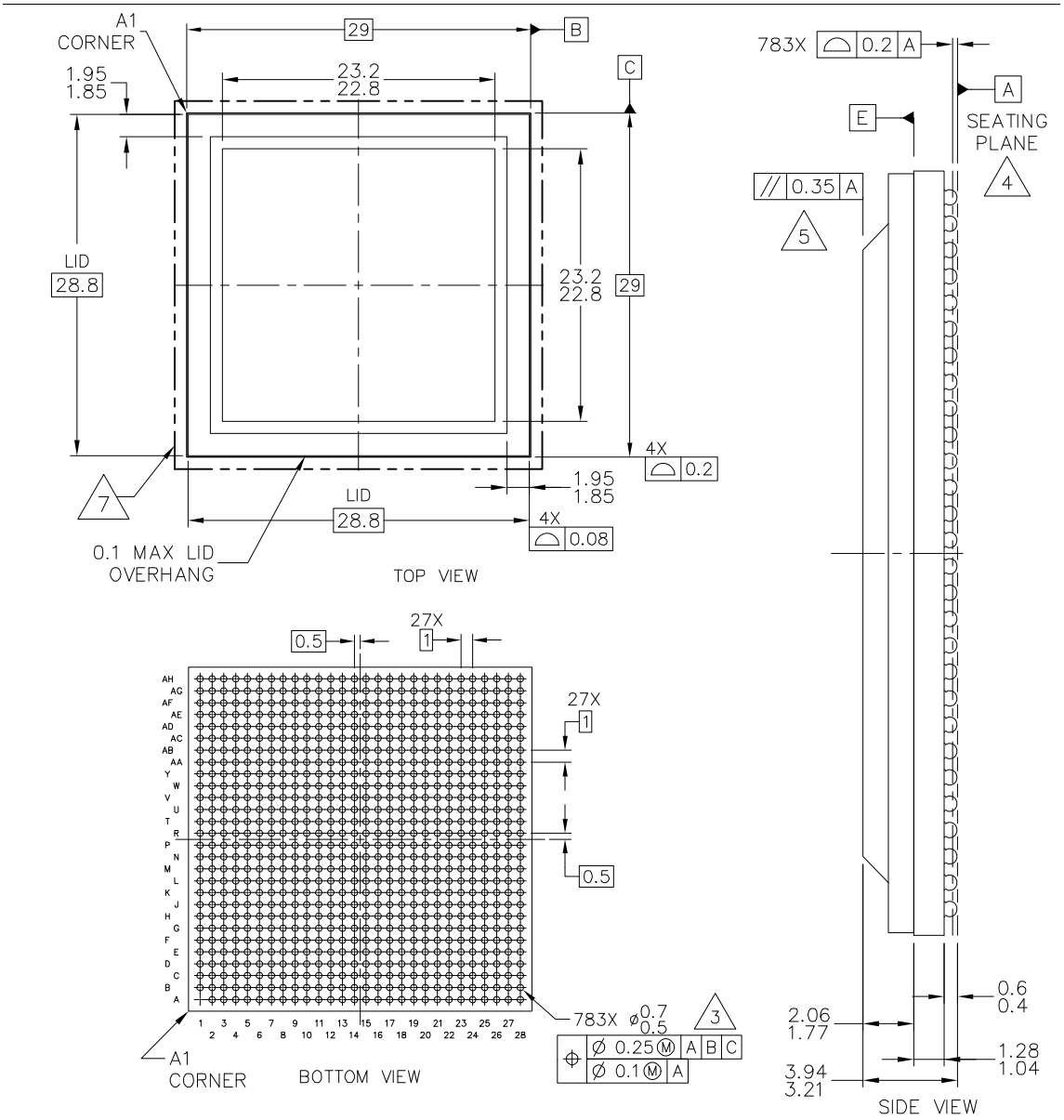


Figure 31. MSC8157 Mechanical Information, 783-ball FC-PBGA Package

NOTES:

1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measure parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. 29.2mm maximum package assembly (lid + laminate) X and Y.