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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamc20e16a-aut

1. The AHB-APB bridge D is available only on C21N and C20N.
2. The CAN peripheral is available only on C21.

Table 10-5. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1
DMAC - Direct Memory Access Controller / Data Access	2

Table 10-6. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
SRAM Port 4 - CM0+ Access	1
SRAM Port 6 - DSU Access	2
AHB-APB Bridge A	3
AHB-APB Bridge B	4
AHB-APB Bridge C	5
SRAM Port 5 - DMAC Data Access	6
DIVAS - Divide Accelerator	7

Table 10-7. SRAM Port Connections

SRAM Port Connection	Port ID	Connection Type
CM0+ - Cortex M0+ Processor	0	Bus Matrix
DSU - Device Service Unit	1	Bus Matrix
DMAC - Direct Memory Access Controller - Data Access	2	Bus Matrix
DMAC - Direct Memory Access Controller - Fetch Access 0	3	Direct
DMAC - Direct Memory Access Controller - Fetch Access 1	4	Direct
DMAC - Direct Memory Access Controller - Write-Back Access 0	5	Direct
DMAC - Direct Memory Access Controller - Write-Back Access 1	6	Direct
CAN0 - Controller Area Network 0	7	Direct
CAN1 - Controller Area Network 1	8	Direct
MTB - Micro Trace Buffer	9	Direct

10.4.3 SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, the different masters can be configured to have a given priority for different type of access.

Value	Description
0	Peripheral is not write protected.
1	Peripheral is write protected.

Name: STATUSC
Offset: 0x3C [ID-00000a18]
Reset: 0x000000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CCL	PTC	DAC	AC	SDADC	ADC1	ADC0	TC4
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC3	TC2	TC1	TC0	TCC2	TC2	TC1	TC0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CAN0	SERCOM5	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0	EVSYS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 23 – CCL: Peripheral CCL Write Protection Status

Bit 22 – PTC: Peripheral PTC Write Protection Status

Bit 21 – DAC: Peripheral DAC Write Protection Status

Bit 20 – AC: Peripheral AC Write Protection Status

Bit 19 – SDADC: Peripheral SDADC Write Protection Status

Bits 17, 18 – ADC: Peripheral ADCn [n=1..0] Write Protection Status

Bits 12, 13, 14, 15, 16 – TC: Peripheral TCn Write Protection Status [n = 4..0]

Bits 9, 10, 11 – TCC: Peripheral TCCn [n = 2..0] Write Protection Status TCCn [n = 2..0]

Bits 8, 9, 10 – TC: Peripheral TCn Write Protection Status [n = 2..0]

Bit 7 – CAN: Peripheral CAN Write Protection Status

Bit	31	30	29	28	27	26	25	24
	DIV[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			RUNSTDBY	DIVSEL	OE	OOV	IDC	GENEN
Access								
Reset			0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
				SRC[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 31:16 – DIV[15:0]: Division Factor
These bits represent a division value for the corresponding Generator. The actual division factor is dependent on the state of DIVSEL. The number of relevant DIV bits for each Generator can be seen in this table. Written bits outside of the specified range will be ignored.

Table 16-3. Division Factor Bits

Generic Clock Generator	Division Factor Bits
Generator 0	8 division factor bits - DIV[7:0]
Generator 1	16 division factor bits - DIV[15:0]
Generator 2-11	8 division factor bits - DIV[4:0]

Bit 13 – RUNSTDBY: Run in Standby
This bit is used to keep the Generator running in Standby as long as it is configured to output to a dedicated GCLK_IO pin. If GENCTRLn.OE is zero, this bit has no effect and the generator will only be running if a peripheral requires the clock.

Value	Description
0	The Generator is stopped in Standby and the GCLK_IO pin state (one or zero) will be dependent on the setting in GENCTRL.OOV.
1	The Generator is kept running and output to its dedicated GCLK_IO pin during Standby mode.

Bit 12 – DIVSEL: Divide Selection
This bit determines how the division factor of the clock source of the Generator will be calculated from DIV. If the clock source should not be divided, DIVSEL must be 0 and the GENCTRLn.DIV value must be either 0 or 1.

20. OSCCTRL – Oscillators Controller

20.1 Overview

The Oscillators Controller (OSCCTRL) provides a user interface to the XOSC, OSC48M and FDPLL96M.

Through the interface registers, it is possible to enable, disable, calibrate, and monitor the OSCCTRL oscillators.

All oscillators statuses are collected in the Status register (STATUS). They can additionally trigger interrupts upon status changes via the INTENSET, INTENCLR, and INTFLAG registers.

Related Links

INTENCLR

INTENSET

INTFLAG

STATUS

20.2 Features

- 0.4-32MHz Crystal Oscillator (XOSC)
  - Tunable gain control
  - Programmable start-up time
  - Crystal or external input clock on XIN I/O
  - Clock failure detection with safe clock switch
  - Clock failure event output
- 48MHz Internal Oscillator (OSC48M)
  - Fast start-up
  - Programmable start-up time
  - 4-bit linear divider available
- Fractional Digital Phase Locked Loop (FDPLL96M)
  - 48MHz to 96MHz output frequency
  - 32kHz to 2MHz reference clock
  - A selection of sources for the reference clock
  - Adjustable proportional integral controller
  - Fractional part used to achieve 1/16th of reference clock step

Bit 8 – DPLLLCKR: DPLL Lock Rise Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the DPLL Lock Rise Interrupt Enable bit, which disables the DPLL Lock Rise interrupt.

Value	Description
0	The DPLL Lock Rise interrupt is disabled.
1	The DPLL Lock Rise interrupt is enabled, and an interrupt request will be generated when the DPLL Lock Rise Interrupt flag is set.

Bit 4 – OSC48MRDY: OSC48M Ready Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the OSC48M Ready Interrupt Enable bit, which disables the OSC48M Ready interrupt.

Value	Description
0	The OSC48M Ready interrupt is disabled.
1	The OSC48M Ready interrupt is enabled, and an interrupt request will be generated when the OSC48M Ready Interrupt flag is set.

Bit 1 – CLKFAIL: Clock Failure Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the XOSC Clock Failure Interrupt Enable bit, which disables the XOSC Clock Failure interrupt.

Value	Description
0	The XOSC Clock Failure interrupt is disabled.
1	The XOSC Clock Failure interrupt is enabled, and an interrupt request will be generated when the XOSC Clock Failure Interrupt flag is set.

Bit 0 – XOSCRDY: XOSC Ready Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the XOSC Ready Interrupt Enable bit, which disables the XOSC Ready interrupt.

Value	Description
0	The XOSC Ready interrupt is disabled.
1	The XOSC Ready interrupt is enabled, and an interrupt request will be generated when the XOSC Ready Interrupt flag is set.

20.8.2 Interrupt Enable Set

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Name: INTENSET
Offset: 0x04 [ID-00001eee]
Reset: 0x00000000
Property: PAC Write-Protection

Bit 1 – SWBACK: Clock Switch Back
This bit clontrols the XOSC32K output switch back to the external clock or crystal scillator in case of clock recovery.

Value	Description
0	The clock switch is disabled.
1	The clock switch is enabled. This bit is reset when the XOSC32K output is switched back to the external clock or crystal oscillator.

Bit 0 – CFDEN: Clock Failure Detector Enable
This bit selects the Clock Failure Detector state.

Value	Description
0	The CFD is disabled.
1	The CFD is enabled.

21.8.7 Event Control

Name: EVCTRL
Offset: 0x17
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								CFDEO
Access								R/W
Reset								0

Bit 0 – CFDEO: Clock Failure Detector Event Out Enable
This bit controls whether the Clock Failure Detector event output is enabled and an event will be generated when the CFD detects a clock failure.

Value	Description
0	Clock Failure Detector Event output is disabled, no event will be generated.
1	Clock Failure Detector Event output is enabled, an event will be generated.

21.8.8 32KHz Internal Oscillator (OSC32K) Control

Name: OSC32K
Offset: 0x18 [ID-00001010]
Reset: 0x0000 0080 (Writing action by User required)
Property: PAC Write-Protection

The Sign bit in the Frequency Correction register (FREQCORR.SIGN) determines the direction of the correction. A positive value will add counts and increase the period (reducing the frequency), and a negative value will reduce counts per period (speeding up the frequency).

Digital correction also affects the generation of the periodic events from the prescaler. When the correction is applied at the end of the correction cycle period, the interval between the previous periodic event and the next occurrence may also be shortened or lengthened depending on the correction value.

Bit	31	30	29	28	27	26	25	24
	SRCADDR[31:24]							
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	SRCADDR[23:16]							
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	SRCADDR[15:8]							
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	SRCADDR[7:0]							
Access								
Reset								

Bits 31:0 – SRCADDR[31:0]: Transfer Source Address
This bit group holds the source address corresponding to the last beat transfer address in the block transfer.

25.10.4 Block Transfer Destination Address

The DSTADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Name: DSTADDR
Offset: 0x08
Property: -

Offset	Name	Bit Pos.								
0x2C ... 0x2F	Reserved									
0x30	DEBOUNCEN	7:0	DEBOUNCEN[7:0]							
0x31		15:8	DEBOUNCEN[15:8]							
0x32		23:16	DEBOUNCEN[23:16]							
0x33		31:24	DEBOUNCEN[31:24]							
0x34	DPRESCALER	7:0	STATESx	PRESCALERx[2:0]			STATESx	PRESCALERx[2:0]		
0x35		15:8	STATESx	PRESCALERx[2:0]			STATESx	PRESCALERx[2:0]		
0x36		23:16								TICKON
0x37		31:24								
0x38	PINSTATE	7:0	PINSTATE[7:0]							
0x39		15:8	PINSTATE[15:8]							
0x3A		23:16	PINSTATE[23:16]							
0x3B		31:24	PINSTATE[31:24]							

26.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

26.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
				CKSEL			ENABLE	SWRST
Access				RW			RW	W
Reset				0			0	0

Bit 4 – CKSEL: Clock Selection
The EIC can be clocked either by GCLK_EIC (when a frequency higher than 32KHz is required for filtering) or by CLK_ULP32K (when power consumption is the priority).

This bit is not Write-Synchronized.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Related Links

PAC - Peripheral Access Controller

27.5.6 Analog Connections

Not applicable.

27.6 Functional Description

27.6.1 Principle of Operation

The NVM Controller is a slave on the AHB and APB buses. It responds to commands, read requests and write requests, based on user configuration.

27.6.1.1 Initialization

After power up, the NVM Controller goes through a power-up sequence. During this time, access to the NVM Controller from the AHB bus is halted. Upon power-up completion, the NVM Controller is operational without any need for user configuration.

27.6.2 Memory Organization

Refer to the Physical Memory Map for memory sizes and addresses for each device.

The NVM is organized into rows, where each row contains four pages, as shown in the NVM Row Organization figure. The NVM has a row-erase granularity, while the write granularity is by page. In other words, a single row erase will erase all four pages in the row, while four write operations are used to write the complete row.

Figure 27-2. NVM Row Organization

Row n	Page (n*4) + 3	Page (n*4) + 2	Page (n*4) + 1	Page (n*4) + 0

The NVM block contains a calibration and auxiliary space plus a dedicated EEPROM emulation space that are memory mapped. Refer to the NVM Organization figure below for details.

The calibration and auxiliary space contains factory calibration and system configuration information. These spaces can be read from the AHB bus in the same way as the main NVM main address space.

In addition, a boot loader section can be allocated at the beginning of the main array, and an EEPROM section can be allocated at the end of the NVM main address space.

PMUXO[3:0]	Name	Description
0x0	A	Peripheral function A selected
0x1	B	Peripheral function B selected
0x2	C	Peripheral function C selected
0x3	D	Peripheral function D selected
0x4	E	Peripheral function E selected
0x6	G	Peripheral function G selected
0x7	H	Peripheral function H selected
0x8	I	Peripheral function I selected
0x9-0xF	-	Reserved

Bits 3:0 – PMUXE[3:0]: Peripheral Multiplexing for Even-Numbered Pin
These bits select the peripheral function for even-numbered pins (2*n) of a PORT group, if the corresponding PINCFGy.PMUXEN bit is '1'.

Not all possible values for this selection may be valid. For more details, refer to the *I/O Multiplexing and Considerations.*

PMUXE[3:0]	Name	Description
0x0	A	Peripheral function A selected
0x1	B	Peripheral function B selected
0x2	C	Peripheral function C selected
0x3	D	Peripheral function D selected
0x4	E	Peripheral function E selected
0x6	G	Peripheral function G selected
0x7	H	Peripheral function H selected
0x8	I	Peripheral function I selected
0x9-0xF	-	Reserved

Related Links
I/O Multiplexing and Considerations

28.9.14 Pin Configuration

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

Bit	31	30	29	28	27	26	25	24
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOn	TOn	TOn	TOn	TOn	TOn	TOn	TOn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TOn: Transmission Occurred

Each Tx Buffer has its own Transmission Occurred bit.

The bits are set when the corresponding TXBRP bit is cleared after a successful transmission.

The bits are reset when a new transmission is requested by writing ‘1’ to the corresponding bit of register TXBAR.

34.8.42 Tx Buffer Cancellation Finished

Name: TXBCF
Offset: 0xDC [ID-0000a4bb]
Reset: 0x00000000
Property: Read-only

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
					ALOCK	PRESCALER[2:0]		
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0]: Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0]: Capture mode Channel 0
These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

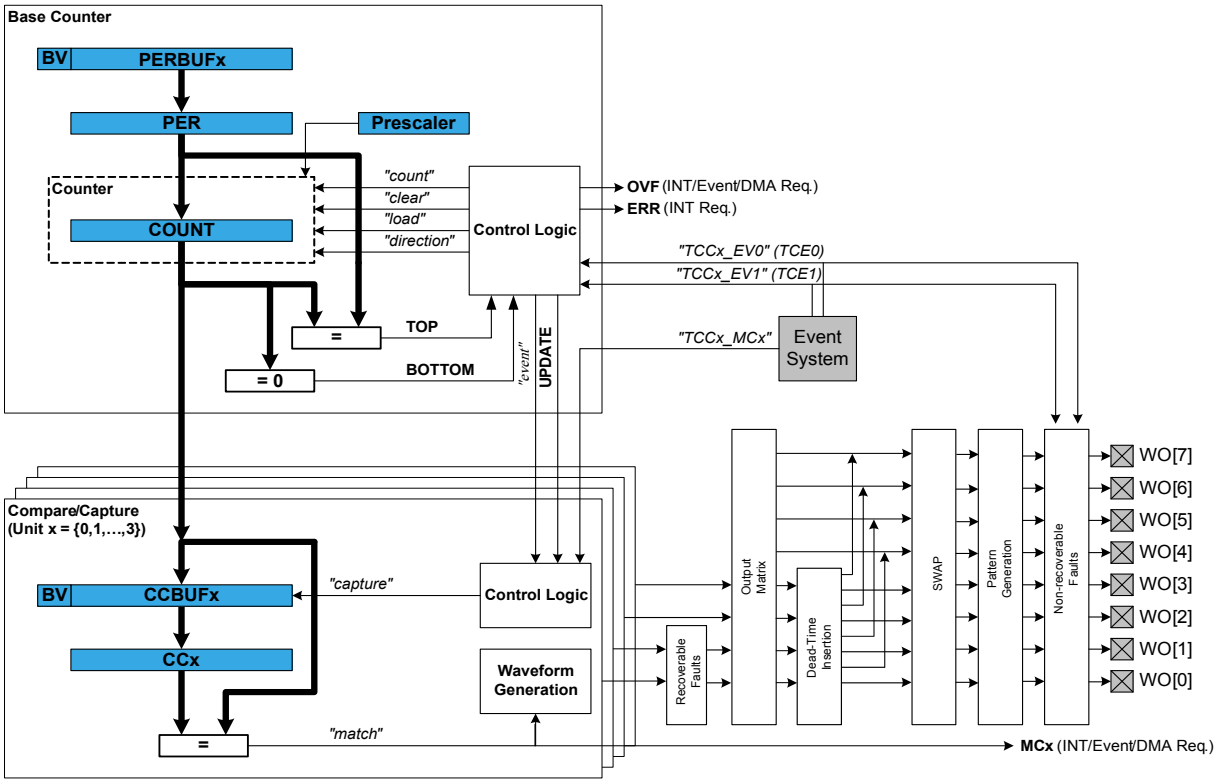
Bits 20, 21 – COPENx: Capture On Pin x Enable
Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

  - Two non-recoverable fault sources
  - Debugger can be source of non-recoverable fault
- Input events:
  - Two input events for counter
  - One input event for each channel
- Output events:
  - Three output events (Count, Re-Trigger and Overflow) available for counter
  - One Compare Match/Input Capture event output for each channel
- Interrupts:
  - Overflow and Re-Trigger interrupt
  - Compare Match/Input Capture interrupt
  - Interrupt on fault detection
- Can be used with DMA and can trigger DMA transactions

36.3 Block Diagram

Figure 36-1. Timer/Counter for Control Applications - Block Diagram



36.4 Signal Description

Pin Name	Type	Description
TCCx/WO[0]	Digital output	Compare channel 0 waveform output
TCCx/WO[1]	Digital output	Compare channel 1 waveform output

Pin Name	Type	Description
…	...	...
TCCx/WO[WO_NUM-1]	Digital output	Compare channel n waveform output

Refer to *I/O Multiplexing and Considerations* for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

I/O Multiplexing and Considerations

36.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

36.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Pin Controller (PORT).

Related Links

PORT: IO Pin Controller

36.5.2 Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes.

36.5.3 Clocks

The TCC bus clock (CLK_TCCx_APB, with x instance number of the TCCx) is enabled by default, and can be enabled and disabled in the Main Clock.

A generic clock (GCLK_TCCx) is required to clock the TCC. This clock must be configured and enabled in the generic clock controller before using the TCC. Note that TCC0 and TCC1 share a peripheral clock generator.

The generic clocks (GCLK_TCCx) are asynchronous to the bus clock (CLK_TCCx_APB). Due to this asynchronicity, writing certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

Peripheral Clock Masking

GCLK - Generic Clock Controller

36.5.4 DMA

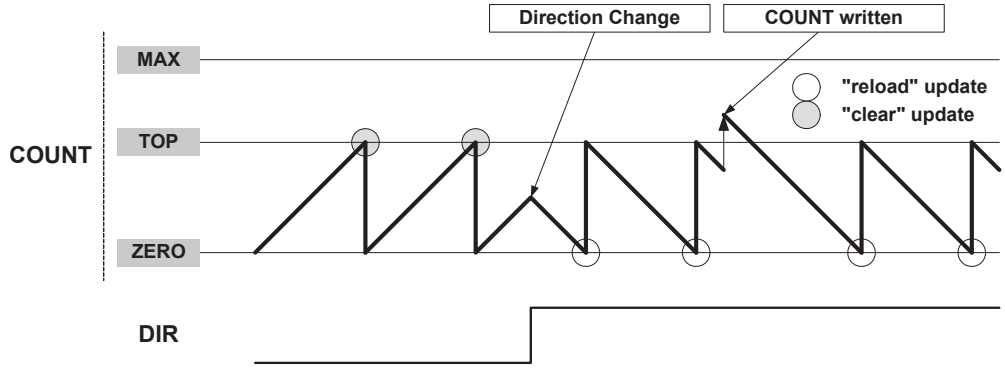
The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

DMAC – Direct Memory Access Controller

INTFLAG.OVF can be used to trigger an interrupt, a DMA request, or an event. An overflow/underflow occurrence (i.e. a compare match with TOP/ZERO) will stop counting if the One-Shot bit in the Control B register is set (CTRLBSET.ONESHOT).

Figure 36-3. Counter Operation



It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. The COUNT value will always be ZERO or TOP, depending on direction set by CTRLBSET.DIR or CTRLBCLR.DIR, when starting the TCC, unless a different value has been written to it, or the TCC has been stopped at a value other than ZERO. The write access has higher priority than count, clear, or reload. The direction of the counter can also be changed during normal operation. See also Figure 36-3.

Stop Command

A stop command can be issued from software by using TCC Command bits in Control B Set register (CTRLBSET.CMD=0x2, STOP).

Pause Event Action

A pause command can be issued when the stop event action is configured in the Input Event Action 1 bits in Event Control register (EVCTRL.EVACT1=0x3, STOP).

Re-Trigger Command and Event Action

A re-trigger command can be issued from software by using TCC Command bits in Control B Set register (CTRLBSET.CMD=0x1, RETRIGGER), or from event when the re-trigger event action is configured in the Input Event 0/1 Action bits in Event Control register (EVCTRL.EVACTn=0x1, RETRIGGER).

When the command is detected during counting operation, the counter will be reloaded or cleared, depending on the counting direction (CTRLBSET.DIR or CTRLBCLR.DIR). The Re-Trigger bit in the Interrupt Flag Status and Clear register will be set (INTFLAG.TRG). It is also possible to generate an event by writing a '1' to the Re-Trigger Event Output Enable bit in the Event Control register (EVCTRL.TRGEO). If the re-trigger command is detected when the counter is stopped, the counter will resume counting operation from the value in COUNT.

Note:
When a re-trigger event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACTn=0x1, RETRIGGER), enabling the counter will not start the counter. The counter will start on the next incoming event and restart on corresponding following event.

Start Event Action

The start action can be selected in the Event Control register (EVCTRL.EVACT0=0x3, START) and can start the counting operation when previously stopped. The event has no effect if the counter is already

Name: INTENCLR
Offset: 0x04 [ID-00001f13]
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
					OVF	WINMON	OVERRUN	RESRDY
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – OVF: Overflow Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Overflow Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The overflow interrupt is disabled.
1	The overflow interrupt is enabled, and an interrupt request will be generated when the Overflow interrupt flag is set.

Bit 2 – WINMON: Window Monitor Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Window Monitor Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The window monitor interrupt is disabled.
1	The window monitor interrupt is enabled, and an interrupt request will be generated when the Window Monitor interrupt flag is set.

Bit 1 – OVERRUN: Overrun Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Overrun Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The Overrun interrupt is disabled.
1	The Overrun interrupt is enabled, and an interrupt request will be generated when the Overrun interrupt flag is set.

Bit 0 – RESRDY: Result Ready Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Result Ready Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The Result Ready interrupt is disabled.
1	The Result Ready interrupt is enabled, and an interrupt request will be generated when the Result Ready interrupt flag is set.

Name: WINLT
Offset: 0x10 [ID-00001f13]
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	WINLT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WINLT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WINLT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – WINLT[23:0]: Window Lower Threshold
If the window monitor is enabled, these bits define the lower threshold value. This WINLT value is in two's complement format.

43.8.12 Window Monitor Upper Threshold

Name: WINUT
Offset: 0x14 [ID-00001f13]
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Symbol	Parameter	Conditions		Measurement			Unit
				Min	Typ	Max	
		Fadc = 1 Msps - R2R disabled with gain compensation	Vddana=2.7V Vref=2.0V	-	+/-0.3	+/-0.8	
			Vddana=5.0V Vref=Vddana/2	-	+/-0.1	+/-0.5	
Offset	Offset Error	Fadc = 1 Msps - R2R disabled	Vddana=5.0V Vref=Vddana	-	+/-7	+/-63	mV
			Vddana=2.7V Vref=2.0V	-	+/-7	+/-64	
SFDR		Spurious Free Dynamic Range	Fs = 1Msps / Fin = 14 kHz / Full range Input signal Vddana=5.0V Vref=Vddana	57	66	73	dB
SINAD(1)		Signal to Noise and Distortion ratio		54	59	62	
SNR at -3 db FS		Signal to Noise ratio		57	60	62	
THD		Total Harmonic Distortion		-71	-64	-56	
		Noise RMS	External Reference voltage	-	0.6	1.9	mV

1. Referred to Full Scale.

47.4.4 Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics

Table 47-8. Operating Conditions(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Res	Resolution	Differential mode	-	16	-	bits
		Single-Ended mode	-	15	-	
CLK_SDADC	Sampling Clock Speed	Chopper OFF (ANACTRL.ONCHOP = 0)	1	-	6	MHz
		Chopper ON (ANACTRL.ONCHOP = 1)	1	-	3	
CLK_SDADC_FS	Conversion rate		CLK_SDADC/4			
fs	Output Data Rate	Free running mode	CLK_SDADC_FS / OSR			
		Single conversion mode SKPCNT = N	(CLK_SDADC_FS / OSR) x (N+1)			
OSR	Oversampling ratio	Differential mode	64	256	1024	Cycles
	Input Conversion range	Differential mode Gaincorr = 0x1	- VREF	-	VREF	V
		Single-Ended mode Gaincorr = 0x1	0	-	VREF	
Vref	Reference Voltage range		1	-	5.5	V
Vcom	Common mode voltage	Differential mode	0	-	AVDD	V
Cin	Input capacitance		0.425	0.5	0.575	pF
Zin	Input impedance	Differential mode	1/(Cin x CLK_SDADC_FS)			kΩ
		Single-Ended mode	1/(Cin x CLK_SDADC_FS x 2)			
	Input anti-alias filter recommendation(2)	Rext	-	1.0	-	kΩ
		Cext	3.3	-	10	nF

1. These are based on simulation. These values are not covered by test or characterization.

Symbol	Parameter	Conditions		Typ.	Max.	Units
			VDD = 5.5V	+/-1.5	+/-3.5	
DNL	Differential non-linearity	VREF= Ext 2.0V	VDD = 2.7V	+/-0.3	+/-2.3	LSB
			VDD = 5.5V	+/-0.4	+/-2.2	
		VREF = VDDANA	VDD = 2.7V	+/-0.2	+/-2.1	
			VDD = 5.5V	+/-0.2	+/-2.1	
		VREF= 1.024V INT REF	VDD = 2.7V	+/-1.0	+/-2.5	
			VDD = 5.5V	+/-1.4	+/-3.5	
	Gain error	Ext. VREF		+/-8	+/-28	mV
	Offset error	Ext. VREF		+/-4	+/-26	mV

1. These values are based on characterization. These values are not covered by test limits in production.

47.4.6 Analog Comparator Characteristics

Table 47-15. Analog Comparator Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
PNIVR	Positive and Negative input range voltage		0	-	VDDANA	V
ICMR	Input common mode range		0	-	VDDANA	V
Off (1)(2)	Offset	Low power COMPCTRLn.SPEED = 0x0	-55	-4/+2	51	mV
		High speed COMPCTRLn.SPEED = 0x3	-22	-2/+1	20	
V_{HYS} (1)(3)	Hysteresis	High speed COMPCTRLn.SPEED = 0x3	39	106	156	mV
T_{PD} (1)	Propagation Delay Vcm=Vddana/2 Vin = ±100mV overdrive from Vcm	Low power COMPCTRLn.SPEED = 0x0	-	149	268	ns
		High speed COMPCTRLn.SPEED =0x3	-	41	73	
T_{START} (1)	Startup time	Low power COMPCTRLn.SPEED = 0x0	-	6.8	10.4	µs
		High speed COMPCTRLn.SPEED = 0x3	-	2.2	3.7	
V_{SCALE} (1)	INL		-	0.569	-	LSB
	DNL		-	0.053	-	