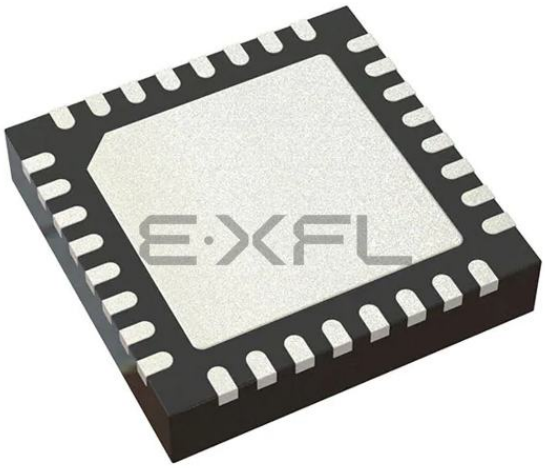


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, WDT |
| Number of I/O | 26 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-VFQFN Exposed Pad |
| Supplier Device Package | 32-VQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamc20e16a-mut |

The DCC0 and DCC1 registers are accessible when the protected state is active. When the device is protected, however, it is not possible to connect a debugger while the CPU is running (STATUSA.CRSTEXT is not writable and the CPU is held under Reset).

Two Debug Communication Channel status bits in the Status B registers (STATUS.DCCDx) indicate whether a new value has been written in DCC0 or DCC1. These bits, DCC0D and DCC1D, are located in the STATUSB registers. They are automatically set on write and cleared on read.

**Note:** The DCC0 and DCC1 registers are shared with the on-board memory testing logic (MBIST). Accordingly, DCC0 and DCC1 must not be used while performing MBIST operations.

**Related Links**

NVMCTRL – Non-Volatile Memory Controller

Security Bit

### 13.11.5 Testing of On-Board Memories MBIST

The DSU implements a feature for automatic testing of memory also known as MBIST (memory built-in self test). This is primarily intended for production test of on-board memories. MBIST cannot be operated from the external address range when the device is protected by the NVMCTRL security bit. If an MBIST command is issued when the device is protected, a protection error is reported in the Protection Error bit in the Status A register (STATUSA.PERR).

1. Algorithm
   The algorithm used for testing is a type of March algorithm called "March LR". This algorithm is able to detect a wide range of memory defects, while still keeping a linear run time. The algorithm is:

   1.1. Write entire memory to '0', in any order.
   1.2. Bit for bit read '0', write '1', in descending order.
   1.3. Bit for bit read '1', write '0', read '0', write '1', in ascending order.
   1.4. Bit for bit read '1', write '0', in ascending order.
   1.5. Bit for bit read '0', write '1', read '1', write '0', in ascending order.
   1.6. Read '0' from entire memory, in ascending order.

   The specific implementation used has a run time which depends on the CPU clock frequency and the number of bytes tested in the RAM. The detected faults are:

   – Address decoder faults
   – Stuck-at faults
   – Transition faults
   – Coupling faults
   – Linked Coupling faults

2. Starting MBIST
   To test a memory, you need to write the start address of the memory to the ADDR.ADDR bit field, and the size of the memory into the Length register.

   For best test coverage, an entire physical memory block should be tested at once. It is possible to test only a subset of a memory, but the test coverage will then be somewhat lower.

   The actual test is started by writing a '1' to CTRL.MBIST. A running MBIST operation can be canceled by writing a '1' to CTRL.SWRST.

3. Interpreting the Results
   The tester should monitor the STATUSA register. When the operation is completed, STATUSA.DONE is set. There are two different modes:

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| ... 0x1FCB | | | | | | | | | | |
| 0x1FCC | MEMTYPE | 7:0 | | | | | | | | SMEMP |
| 0x1FCD | | 15:8 | | | | | | | | |
| 0x1FCE | | 23:16 | | | | | | | | |
| 0x1FCF | | 31:24 | | | | | | | | |
| 0x1FD0 | PID4 | 7:0 | FKBC[3:0] | | | | JEPCC[3:0] | | | |
| 0x1FD1 | | 15:8 | | | | | | | | |
| 0x1FD2 | | 23:16 | | | | | | | | |
| 0x1FD3 | | 31:24 | | | | | | | | |
| 0x1FD4 ... 0x1FDF | Reserved | | | | | | | | | |
| 0x1FE0 | PID0 | 7:0 | PARTNBL[7:0] | | | | | | | |
| 0x1FE1 | | 15:8 | | | | | | | | |
| 0x1FE2 | | 23:16 | | | | | | | | |
| 0x1FE3 | | 31:24 | | | | | | | | |
| 0x1FE4 | PID1 | 7:0 | JEPIDCL[3:0] | | | | PARTNBH[3:0] | | | |
| 0x1FE5 | | 15:8 | | | | | | | | |
| 0x1FE6 | | 23:16 | | | | | | | | |
| 0x1FE7 | | 31:24 | | | | | | | | |
| 0x1FE8 | PID2 | 7:0 | REVISION[3:0] | | | | JEPU | JEPIDCH[2:0] | | |
| 0x1FE9 | | 15:8 | | | | | | | | |
| 0x1FEA | | 23:16 | | | | | | | | |
| 0x1FEB | | 31:24 | | | | | | | | |
| 0x1FEC | PID3 | 7:0 | REVAND[3:0] | | | | CUSMOD[3:0] | | | |
| 0x1FED | | 15:8 | | | | | | | | |
| 0x1FEE | | 23:16 | | | | | | | | |
| 0x1FEF | | 31:24 | | | | | | | | |
| 0x1FF0 | CID0 | 7:0 | PREAMBLEB0[7:0] | | | | | | | |
| 0x1FF1 | | 15:8 | | | | | | | | |
| 0x1FF2 | | 23:16 | | | | | | | | |
| 0x1FF3 | | 31:24 | | | | | | | | |
| 0x1FF4 | CID1 | 7:0 | CCLASS[3:0] | | | | PREAMBLE[3:0] | | | |
| 0x1FF5 | | 15:8 | | | | | | | | |
| 0x1FF6 | | 23:16 | | | | | | | | |
| 0x1FF7 | | 31:24 | | | | | | | | |
| 0x1FF8 | CID2 | 7:0 | PREAMBLEB2[7:0] | | | | | | | |
| 0x1FF9 | | 15:8 | | | | | | | | |
| 0x1FFA | | 23:16 | | | | | | | | |
| 0x1FFB | | 31:24 | | | | | | | | |
| 0x1FFC | CID3 | 7:0 | PREAMBLEB3[7:0] | | | | | | | |
| 0x1FFD | | 15:8 | | | | | | | | |
| 0x1FFE | | 23:16 | | | | | | | | |
| 0x1FFF | | 31:24 | | | | | | | | |

| Value | Description |
|---|---|
| 0000 | 48MHz |
| 0001 | 24MHz |
| 0010 | 16MHz |
| 0011 | 12MHz |
| 0100 | 9.6MHz |
| 0101 | 8MHz |
| 0110 | 6.86MHz |
| 0111 | 6MHz |
| 1000 | 5.33MHz |
| 1001 | 4.8MHz |
| 1010 | 4.36MHz |
| 1011 | 4MHz |
| 1100 | 3.69MHz |
| 1101 | 3.43MHz |
| 1110 | 3.2MHz |
| 1111 | 3MHz |

### 20.8.10 OSC48M Startup

**Name:** OSC48MSTUP
**Offset:** 0x16 [ID-00001eee]
**Reset:** 0x07
**Property:** -

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | STARTUP[2:0] | | |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 1 | 1 | 1 |

**Bits 2:0 – STARTUP[2:0]: Oscillator Startup Delay**
These bits select the oscillator start-up delay in oscillator cycles.

**Table 20-6. Oscillator Divider Selection**

| STARTUP[2:0] | Number of OSCM48M Clock Cycles | Approximate Equivalent Time |
|---|---|---|
| 0x0 | 8 | 166ns |
| 0x1 | 16 | 333ns |
| 0x2 | 32 | 667ns |
| 0x3 | 64 | 1.333µs |
| 0x4 | 128 | 2.667µs |
| 0x5 | 256 | 5.333µs |
| 0x6 | 512 | 10.667µs |
| 0x7 | 1024 | 21.333µs |

**Related Links**

NVM Software Calibration Area Mapping

## 21.6 Functional Description

### 21.6.1 Principle of Operation

XOSC32K, OSC32K, and OSCULP32K are configured via OSC32KCTRL control registers. Through this interface, the sub-peripherals are enabled, disabled, or have their calibration values updated.

The STATUS register gathers different status signals coming from the sub-peripherals of OSC32KCTRL. The status signals can be used to generate system interrupts, and in some cases wake up the system from standby mode, provided the corresponding interrupt is enabled.

### 21.6.2 32KHz External Crystal Oscillator (XOSC32K) Operation

The XOSC32K can operate in two different modes:

- External clock, with an external clock signal connected to XIN32
- Crystal oscillator, with an external 32.768kHz crystal connected between XIN32 and XOUT32

At reset, the XOSC32K is disabled, and the XIN32/XOUT32 pins can either be used as General Purpose I/O (GPIO) pins or by other peripherals in the system.

When XOSC32K is enabled, the operating mode determines the GPIO usage. When in crystal oscillator mode, the XIN32 and XOUT32 pins are controlled by the OSC32KCTRL, and GPIO functions are overridden on both pins. When in external clock mode, the only XIN32 pin will be overridden and controlled by the OSC32KCTRL, while the XOUT32 pin can still be used as a GPIO pin.

The XOSC32K is enabled by writing a '1' to the Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.ENABLE=1). The XOSC32K is disabled by writing a '0' to the Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.ENABLE=0).

To enable the XOSC32K as a crystal oscillator, the XTALEN bit in the 32KHz External Crystal Oscillator Control register must be set (XOSC32K.XTALEN=1). If XOSC32K.XTALEN is '0', the external clock input will be enabled.

The XOSC32K 32.768kHz output is enabled by setting the 32KHz Output Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.EN32K=1). The XOSC32K also has a 1.024kHz clock output. This is enabled by setting the 1KHz Output Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.EN1K=1).

It is also possible to lock the XOSC32K configuration by setting the Write Lock bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.WRTLOCK=1). If set, the XOSC32K configuration is locked until a Power-On Reset (POR) is detected.

The XOSC32K will behave differently in different sleep modes based on the settings of XOSC32K.RUNSTDBY, XOSC32K.ONDEMAND, and XOSC32K.ENABLE. If XOSC32KCTRL.ENABLE=0, the XOSC32K will be always stopped. For XOS32KCTRL.ENABLE=1, this table is valid:

When the Run in Standby bit in the VREG register (VREG.RUNSTDBY) is written to '1', VDDCORE is supplied by the main voltage regulator. The VDDCORE level is set to the active mode voltage level.

**Related Links**

Sleep Mode Controller

### 22.6.2 Voltage Reference System Operation

The reference voltages are generated by a functional block DETREF inside of the SUPC. DETREF is providing a fixed-voltage source, BANDGAP=1V, and a variable voltage, INTREF.

#### 22.6.2.1 Initialization

The voltage reference output and the temperature sensor are disabled after any Reset.

#### 22.6.2.2 Enabling, Disabling, and Resetting

The voltage reference output is enabled/disabled by setting/clearing the Voltage Reference Output Enable bit in the Voltage Reference register (VREF.VREFOE).

The temperature sensor is enabled/disabled by setting/clearing the Temperature Sensor Enable bit in the Voltage Reference register (VREF.TSEN).

**Note:** When VREF.ONDEMAND=0, it is not recommended to enable both voltage reference output and temperature sensor at the same time - only the voltage reference output will be present at both ADC inputs.

#### 22.6.2.3 Selecting a Voltage Reference

The Voltage Reference Selection bit field in the VREF register (VREF.SEL) selects the voltage of INTREF to be applied to analog modules, e.g. the ADC.

#### 22.6.2.4 Sleep Mode Operation

The Voltage Reference output and the Temperature Sensor output behavior during sleep mode can be configured using the Run in Standby bit and the On Demand bit in the Voltage Reference register (VREF.RUNSTDBY, VREF.ONDEMAND), see the following table:

**Table 22-1. VREF Sleep Mode Operation**

| VREF.ONDEMAND | VREF.RUNSTDBY | Voltage Reference Sleep behavior |
|---|---|---|
| - | - | Disable |
| 0 | 0 | Always run in all sleep modes *except* standby sleep mode |
| 0 | 1 | Always run in all sleep modes *including* standby sleep mode |
| 1 | 0 | Only run if requested by the ADC, in all sleep modes *except* standby sleep mode |
| 1 | 1 | Only run if requested by the ADC, in all sleep modes *including* standby sleep mode |

### 22.6.3 Brown-Out Detectors

#### 22.6.3.1 Initialization

Before a Brown-Out Detector (BODVDD) is enabled, it must be configured, as outlined by the following:

- Set the BOD threshold level (BODVDD.LEVEL)
- Set the configuration in active, standby (BODVDD.ACTCDG, BODVDD.STDBYCFG)
- Set the prescaling value if the BOD will run in sampling mode (BODVDD.PSEL)
- Set the action and hysteresis (BODVDD.ACTION and BODVDD.HYST)

**Name:** INTENSET
**Offset:** 0x0A
**Reset:** 0x0000
**Property:** PAC Write-Protection

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | OVF | | | | | | | CMP0 |
| Access | R/W | | | | | | | R/W |
| Reset | 0 | | | | | | | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PERn | PERn | PERn | PERn | PERn | PERn | PERn | PERn |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 15 – OVF: Overflow Interrupt Enable**
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt.

| Value | Description |
|---|---|
| 0 | The Overflow interrupt is disabled. |
| 1 | The Overflow interrupt is enabled. |

**Bit 8 – CMP0: Compare 0 Interrupt Enable**
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Compare 0 Interrupt Enable bit, which enables the Compare 0 interrupt.

| Value | Description |
|---|---|
| 0 | The Compare 0 interrupt is disabled. |
| 1 | The Compare 0 interrupt is enabled. |

**Bits 7:0 – PERn: Periodic Interval n Interrupt Enable [n = 7..0]**
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Periodic Interval n Interrupt Enable bit, which enables the Periodic Interval n interrupt.

| Value | Description |
|---|---|
| 0 | Periodic Interval n interrupt is disabled. |
| 1 | Periodic Interval n interrupt is enabled. |

### 24.8.5 Interrupt Flag Status and Clear in COUNT32 mode (CTRLA.MODE=0)

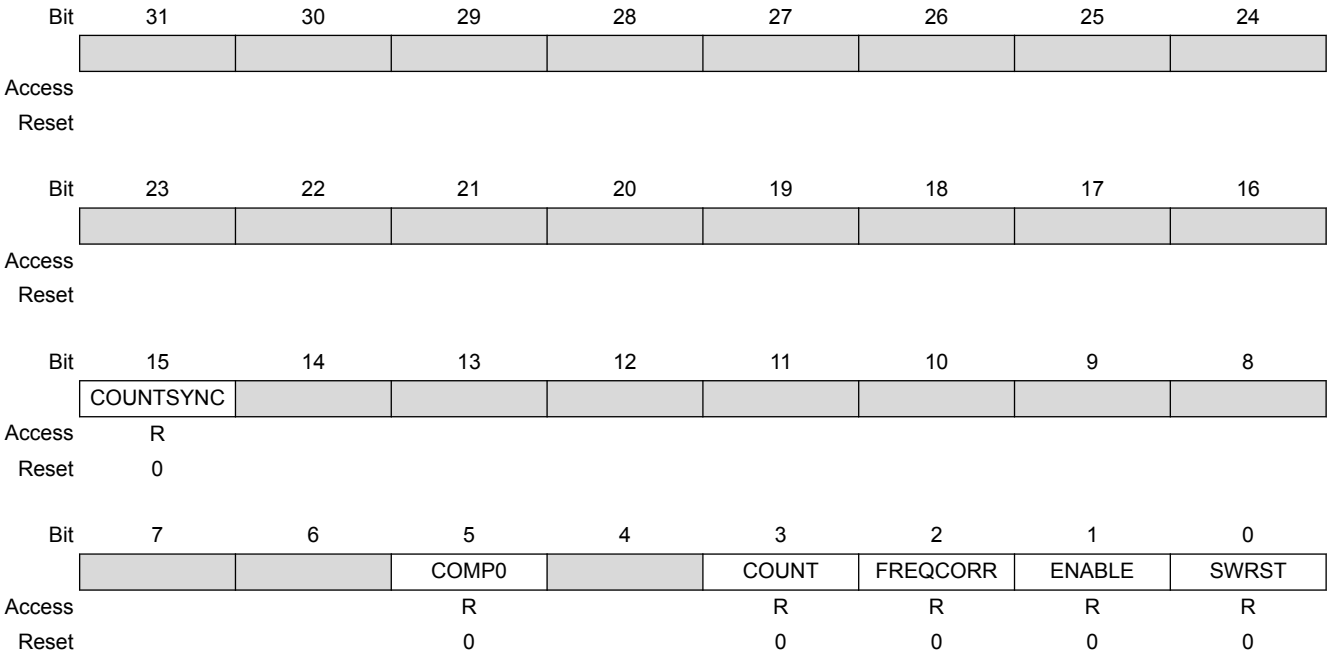
**Name:** INTFLAG
**Offset:** 0x0C
**Reset:** 0x0000
**Property:** -

This bit controls the functionality when the CPU is halted by an external debugger.

| Value | Description |
|---|---|
| 0 | The RTC is halted when the CPU is halted by an external debugger. |
| 1 | The RTC continues normal operation when the CPU is halted by an external debugger. |

### 24.8.7 Synchronization Busy in COUNT32 mode (CTRLA.MODE=0)

**Name:** SYNCBUSY
**Offset:** 0x10
**Reset:** 0x00000000
**Property:** -




**Bit 15 – COUNTSYNC: Count Read Sync Enable Synchronization Busy Status**

| Value | Description |
|---|---|
| 0 | Write synchronization for CTRLA.COUNTSYNC bit is complete. |
| 1 | Write synchronization for CTRLA.COUNTSYNC bit is ongoing. |

**Bit 5 – COMP0: Compare 0 Synchronization Busy Status**

| Value | Description |
|---|---|
| 0 | Write synchronization for COMP0 register is complete. |
| 1 | Write synchronization for COMP0 register is ongoing. |

**Bit 3 – COUNT: Count Value Synchronization Busy Status**

| Value | Description |
|---|---|
| 0 | Read/write synchronization for COUNT register is complete. |
| 1 | Read/write synchronization for COUNT register is ongoing. |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | COMP[15:8] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | COMP[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 15:0 – COMP[15:0]: Compare Value**

The 16-bit value of COMPn is continuously compared with the 16-bit COUNT value. When a match occurs, the Compare n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn) is set on the next counter cycle.

**Bits 3:2 – FQOS[1:0]: Fetch Quality of Service**
These bits define the memory priority access during the fetch operation.

| FQOS[1:0] | Name | Description |
|---|---|---|
| 0x0 | DISABLE | Background (no sensitive operation) |
| 0x1 | LOW | Sensitive Bandwidth |
| 0x2 | MEDIUM | Sensitive Latency |
| 0x3 | HIGH | Critical Latency |

**Bits 1:0 – WRBQOS[1:0]: Write-Back Quality of Service**
These bits define the memory priority access during the write-back operation.

| WRBQOS[1:0] | Name | Description |
|---|---|---|
| 0x0 | DISABLE | Background (no sensitive operation) |
| 0x1 | LOW | Sensitive Bandwidth |
| 0x2 | MEDIUM | Sensitive Latency |
| 0x3 | HIGH | Critical Latency |

**Related Links**
SRAM Quality of Service

### 25.8.8 Software Trigger Control

**Name:** SWTRIGCTRL
**Offset:** 0x10
**Reset:** 0x00000000
**Property:** PAC Write-Protection

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | IN[31:24] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | IN[23:16] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | IN[15:8] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | IN[7:0] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 31:0 – IN[31:0]: PORT Data Input Value**
These bits are cleared when the corresponding I/O pin input sampler detects a logical low level on the input pin.

These bits are set when the corresponding I/O pin input sampler detects a logical high level on the input pin.

### 28.9.10 Control

**Tip:** The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

**Name:** CTRL
**Offset:** 0x24
**Reset:** 0x00000000
**Property:** PAC Write-Protection

The DMAC can be used for debug messages functionality.

**Related Links**

DMAC – Direct Memory Access Controller

### 34.5.5 Interrupts

The interrupt request lines are connected to the interrupt controller. Using the CAN interrupts requires the interrupt controller to be configured first.

**Related Links**

Nested Vector Interrupt Controller

### 34.5.6 Events

Not applicable.

### 34.5.7 Debug Operation

Not applicable.

### 34.5.8 Register Access Protection

Not applicable.

### 34.5.9 Analog Connections

No analog connections.

## 34.6 Functional Description

### 34.6.1 Principle of Operation

The CAN performs communication according to ISO 11898-1 (identical to Bosch CAN protocol specification 2.0 part A,B). In addition the CAN supports communication according to CAN FD specification V1.0.

The message storage is intended to be a single- or dual-ported Message RAM outside the module. It is connected to the CAN via AHB.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing receive message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmit status information.

Acceptance filtering is implemented by a combination of up to 128 filter elements where each one can be configured as a range, as a bit mask, or as a dedicated ID filter.

### 34.6.2 Operating Modes

#### 34.6.2.1 Software Initialization

Software initialization is started by setting bit CCCR.INIT, either by software or by a hardware reset, when an uncorrected bit error was detected in the Message RAM, or by going Bus_Off. While CCCR.INIT is set, message transfer from and to the CAN bus is stopped, the status of the CAN bus output CAN_TX is ”recessive” (HIGH). The counters of the Error Management Logic EML are unchanged. Setting CCCR.INIT does not change any configuration register. Resetting CCCR.INIT finishes the software initialization. Afterwards the Bit Stream Processor BSP synchronizes itself to the data transfer on the CAN

**Bit 26 – WDIL: Watchdog Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 25 – BOL: Bus_Off Status Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 24 – EWL: Error Warning Status Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 23 – EPL: Error Passive Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 22 – ELOL: Error Logging Overflow Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 21 – BEUL: Bit Error Uncorrected Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 20 – BECL: Bit Error Corrected Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 19 – DRXL: Message stored to Dedicated Rx Buffer Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Bit 18 – TOOL: Timeout Occurred Interrupt Line**

| Value | Description |
|---|---|
| 0 | Interrupt assigned to CAN interrupt line 0. |
| 1 | Interrupt assigned to CAN interrupt line 1. |

**Table 34-11. Event Type**

| Value | Name | Description |
|---|---|---|
| 0x0 or 0x3 | RES | Reserved |
| 0x1 | TXE | Tx event |
| 0x2 | TXC | Transmission in spite of cancellation (always set for transmission in DAR mode) |

- E1 Bit 21 - FDF: FD Format

  0 : Standard frame format.

  1 : CAN FD frame format (new DLC-coding and CRC).
- E1 Bit 20 - BRS: Bit Rate Search

  0 : Frame received without bit rate switching.

  1 : Frame received with bit rate switching.
- E1 Bits 19:16 - DLC[3:0]: Data Length Code

  0-8 : CAN + CAN FD: received frame has 0-8 data bytes.

  9-15 : CAN: received frame has 8 data bytes.

  9-15 : CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.
- E1 Bits 15:0 - TXTS[15:0]: Tx Timestamp

  Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP.

### 34.9.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address SIDFC.FLSSA plus the index of the filter element (0 ... 127).

**Table 34-12. Standard Message ID Filter Element**

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S0 | SFT [1:0] | | SFEC [2:0] | | | SFID1[10:0] | | | | | | | | | | | | | | | | SFID2[10:0] | | | | | | | | | | |

- Bits 31:30 - SFT[1:0]: Standard Filter Type

  This field defines the standard filter type.

**Table 34-13. Standard Filter Type**

| Value | Name | Description |
|---|---|---|
| 0x0 | RANGE | Range filter from SFID1 to SFID2 (SFID2 >= SFID1) |
| 0x1 | DUAL | Dual ID filter for SFID1 or SFID2 |
| 0x2 | CLASSIC | Classic filter: SFID1 = filter, SFID2 = mask |
| 0x3 | RES | Reserved |

- Bits 29:27 - SFEC[2:0]: Standard Filter Element Configuration

**Bit 1 – LUPD: Lock Update**
This bit controls the update operation of the TCC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable updating.

| Value | Description |
|---|---|
| 0 | The CCBx, PERB, PGVB, PGOB, and SWAPBx buffer registers values *are* copied into the corresponding CCx, PER, PGV, PGO and SWAPx registers on hardware update condition. |
| 1 | The CCBx, PERB, PGVB, PGOB, and SWAPBx buffer registers values are *not* copied into the corresponding CCx, PER, PGV, PGO and SWAPx registers on hardware update condition. |

**Bit 0 – DIR: Counter Direction**
This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

| Value | Description |
|---|---|
| 0 | The timer/counter is counting up (incrementing). |
| 1 | The timer/counter is counting down (decrementing). |

### 36.8.3 Control B Set

This register allows the user to change this register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set (CTRLBCLR) register.

**Name:** CTRLBSET
**Offset:** 0x05 [ID-00002e48]
**Reset:** 0x00
**Property:** PAC Write-Protection, Write-Synchronized, Read-Synchronized

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CMD[2:0] | | | IDXCMD[1:0] | | ONESHOT | LUPD | DIR |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7:5 – CMD[2:0]: TCC Command**
These bits can be used for software control of re-triggering and stop commands of the TCC. When a command has been executed, the CMD bit field will be read back as zero. The commands are executed on the next prescaled GCLK_TCC clock cycle.

Writing zero to this bit group has no effect

Writing a valid value to this bit group will set the associated command.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

| Value | Description |
|---|---|
| 0 | There is no reset operation ongoing. |
| 1 | The reset operation is ongoing. |

### 43.8.2 Control B

**Name:** CTRLB
**Offset:** 0x01 [ID-00001f13]
**Reset:** 0x00
**Property:** –

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | START |
| Access | | | | | | | | W |
| Reset | | | | | | | | 0 |

**Bit 0 – START: Start Measurement**

| Value | Description |
|---|---|
| 0 | Writing a zero to this bit has no effect. |
| 1 | Writing a one to this bit starts a measurement |

### 43.8.3 Control C

**Name:** CTRLC
**Offset:** 0x02 [ID-00001f13]
**Reset:** 0x00
**Property:** PAC Write-Protection, Enable-protected

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | FREERUN | | WINMODE[2:0] | | |
| Access | | | | R/W | | R/W | R/W | R/W |
| Reset | | | | 0 | | 0 | 0 | 0 |

**Bit 4 – FREERUN: Free Running Measurement**

| Value | Description |
|---|---|
| 0 | TSENS operates in single measurement mode. |
| 1 | TSENS is in free running mode and a new measurement will be initiated when the previous measurement completes. |

**Bits 2:0 – WINMODE[2:0]: Window Monitor Mode**
These bits enable and define the window monitor mode.

$C_{LEXT}=2(C_L-C_{STRAY}-C_{SHUNT})$

where $C_{STRAY}$ is the capacitance of the pins and PCB and CSHUNT is the shunt capacitance of the crystal.

**Table 45-43. 32kHz Crystal Oscillator Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ (1) | Crystal oscillator frequency | | - | 32768 | - | Hz |
| $C_L$ (1) | Crystal load capacitance | | - | - | 12.5 | pF |
| $C_{SHUNT}$ (1) | Crystal shunt capacitance | | - | - | 1.75 | |
| Cm (1) | Motional capacitance | | - | 1.25 | - | fF |
| ESR | Crystal Equivalent Series Resistance - SF = 3 | F = 32.768kHz, $C_L$=12.5 pF | - | - | 79 | kΩ |
| Cxin32k | Parasitic capacitor load | | - | 2.9 | - | pF |
| Cxout32k | | | - | 3.2 | - | |
| Tstart | Startup time | F = 32.768kHz, $C_L$=12.5 pF | - | 16 | 24 | Kcycles |

1. These are based on simulation. These values are not covered by test or characterization

**Table 45-44. Power Consumption(1)**

| Symbol | Parameters | Conditions | Ta | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Current consumption | VDD = 5.0V | Max 85°C<br>Typ 25°C | 1528 | 1720 | nA |

1. These are based on characterization.

### 45.12.3 Digital Phase Locked Loop (DPLL) Characteristics

**Table 45-45. Fractional Digital Phase Locked Loop Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$(1) | Input frequency | | 32 | | 2000 | KHz |
| $f_{OUT}$(1) | Output frequency | | 48 | | 96 | MHz |
| Jp(2) | Period jitter (Peak-Peak value) | $f_{IN}$= 32 kHz, $f_{OUT}$= 48 MHz | - | 1.5 | 3.0 | % |
| | | $f_{IN}$= 32 kHz, $f_{OUT}$= 96 MHz | - | 2.7 | 8.0 | |
| | | $f_{IN}$= 2 MHz, $f_{OUT}$= 48 MHz | - | 1.8 | 4.0 | |
| | | $f_{IN}$= 2 MHz, $f_{OUT}$= 96 MHz | - | 2.5 | 6.0 | |
| $t_{LOCK}$(2) | Lock Time | After startup, time to get lock signal. $f_{IN}$= 32 kHz, $f_{OUT}$= 96 MHz | - | 1.1 | 1.5 | ms |
| | | After startup, time to get lock signal. | - | 25 | 35 | µs |

1. These are based on characterization.

### 46.6.3 Digital Phase Locked Loop (DPLL) Characteristics

**Table 46-14. Power Consumption(1)**

| Symbol | Parameters | Conditions | Ta | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Current Consumption | Ck=48MHz<br>$V_{DD}$=5.0V | Max 105°C<br>Typ 25°C | 536 | 629 | µA |
| | | Ck=96MHz<br>$V_{DD}$=5.0V | | 865 | 986 | |

1. These are based on characterization.

### 46.6.4 32.768kHz Internal Oscillator (OSC32K) Characteristics

**Table 46-15. 32 kHz RC Oscillator Electrical Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output frequency | T=25°C<br>VDDANA = 5.0V | 32.112 | 32.768 | 33.423 | kHz |
| | | T=25°C<br>Over [2.7, 5.5]V | 29.491 | 32.768 | 36.044 | kHz |
| | | Over [-40,105]°C<br>Over [2.7, 5.5]V | 25.559 | 32.768 | 37.683 | kHz |
| Tstartup | Startup time | | - | 1 | 2 | cycles |
| Duty (1) | Duty cycle | | - | 50 | - | % |

1. These are based on simulation. These values are not covered by test or characterization.

**Table 46-16. Power Consumption**

| Symbol | Parameters | Conditions | Ta | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Current consumption | VDD = 5.0V | Max 105°C<br>Typ 25°C | 0.864 | 1.116 | µA |

1. These are based on characterization.

### 46.6.5 Ultra Low Power Internal 32kHz RC Oscillator (OSCULP32K) Characteristics

**Table 46-17. Ultra Low Power Internal 32 kHz RC Oscillator Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| Fout | Output frequency | T=25°C | 30.965 | 32.768 | 34.57 | kHz |

| Mode | Conditions | Ta | Vcc | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | | 105°C | 5.0V | 6.3 | 7.1 | |
| | CPU running a CoreMark algorithm | 25°C | 3.0V | 5.2 | 5.7 | mA |
| | | 105°C | 3.0V | 5.5 | 6.6 | |
| | CPU running a CoreMark algorithm. with GCLKIN as reference | 25°C | 5.0V | 115*Freq+167 | 126*Freq+167 | µA (with freq in MHz) |
| | | 105°C | 5.0V | 118*Freq+383 | 110*Freq+1583 | |
| IDLE | | 25°C | 5.0V | 1.2 | 1.7 | mA |
| | | 105°C | 5.0V | 1.5 | 2.6 | |
| STANDBY | XOSC32K running RTC running at 1kHz | 25°C | 5.0V | 15.9 | 37.0 | µA |
| | | 105°C | 5.0V | 187.0 | 602.0 | |
| | XOSC32K and RTC stopped | 25°C | 5.0V | 14.6 | 35.0 | |
| | | 105°C | 5.0V | 185.0 | 600.0 | |

1. These are based on characterization.

## 47.4 Analog Characteristics

### 47.4.1 Power On Reset (POR) Characteristics

**Table 47-3. POR Characteristics**

| Symbol | Parameters | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{POT+}$ | Voltage threshold Level on VDDIN rising | - | 2.55 | - | V |
| $V_{POT-}$ | Voltage threshold Level on VDDIN falling | 1.77 | 1.92 | 2.04 | |

| Symbol | Parameter | Conditions | | Measurement | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| | | Fadc = 1 Msps - R2R disabled with offset compensation | Vddana=5.0V Vref=Vddana/2 | - | +/-0.01 | +/-5.6 | |
| | | | Vddana=2.7V Vref=2.0V | - | +/-0.4 | +/-4.2 | |
| SFDR | | Spurious Free Dynamic Range | Fs = 1Msps / Fin = 14 kHz / Full range Input signal Vddana=5.0V Vref=Vddana | 63 | 71 | 81 | dB |
| SINAD(1) | | Signal to Noise and Distortion ratio | | 60 | 65 | 70 | |
| SNR at -3 db FS | | Signal to Noise ratio | | 64 | 67 | 70 | |
| THD | | Total Harmonic Distortion | | 63 | -70 | 81 | |
| | | Noise RMS | External Reference voltage | - | 0.4 | 3.2 | mV |

1. Referred to Full Scale.
2. Dynamical input range is +/-6% of Full scale.

**Table 47-7. Single-Ended Mode**

| Symbol | Parameter | Conditions | | Measurement | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| ENOB(1) | Effective Number of bits | Fadc = 500 ksps - R2R disabled | Vddana=3.0V Vref=Vddana | 9.0 | 9.7 | 10.2 | bits |
| | | | Vddana=3.0V Vref=2.0V | 9.0 | 9.6 | 10.1 | |
| | | Fadc = 1 Msps - R2R disabled | Vddana=3.0V Vref=Vddana | 8.9 | 9.6 | 10.0 | |
| | | | Vddana=3.0V Vref=2.0V | 8.9 | 9.4 | 9.7 | |
| TUE | Total Unadjusted Error | Fadc = 500 ksps - R2R disabled with offset and gain compensation | Vddana=5.0V Vref=Vddana | - | +/-12.9 | +/-25.2 | LSB |
| | | | Vddana=2.7V Vref=2.0V | - | +/-25 | +/-49.6 | |
| | | Fadc = 1 Msps - R2R disabled with offset and gain compensation | Vddana=5.0V Vref=Vddana | - | +/-13.5 | +/-26.4 | |
| | | | Vddana=2.7V Vref=2.0V | - | +/-27 | +/-52 | |
| INL | Integral Non Linearity | Fadc = 500 ksps - R2R disabled | Vddana=5.0V Vref=Vddana | - | +/-3.7 | +/-6.5 | |
| | | | Vddana=2.7V Vref=2.0V | - | +/-3.4 | +/-5.9 | |
| | | Fadc = 1 Msps - R2R disabled | Vddana=5.0V Vref=Vddana | - | +/-4.2 | +/-7.4 | LSB |
| | | | Vddana=2.7V Vref=2.0V | - | +/-3.5 | +/-6.2 | |
| DNL | Differential Non Linearity | Fadc = 500 ksps - R2R disabled | Vddana=5.0V Vref=Vddana | - | -0.9/+1.2 | -1/+1.6 | |
| | | | Vddana=2.7V Vref=2.0V | - | -0.9/+1.3 | -1/+2.3 | |
| | | Fadc = 1 Msps - R2R disabled | Vddana=5.0V Vref=Vddana | - | -1/+1.1 | -1/+1.3 | |
| | | | Vddana=2.7V Vref=2.0V | - | -1/+1.4 | -1/+3.1 | |
| Gain | Gain Error | Fadc = 1 Msps - R2R disabled w/o gain compensation | Vddana=5.0V Vref=Vddana | - | +/-0.2 | +/-0.7 | % |
| | | | Vddana=2.7V Vref=2.0V | - | +/-0.3 | +/-1.4 | |
| | | | Vddana=5.0V 1V internal Ref | - | +/-1.6 | +/-6.6 | |
| | | | Vddana=5.0V Vref=Vddana/2 | - | +/-0.2 | +/-1.1 | |

**Table 48-6. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 48-7. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |